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Modelling of organic thin film transistors for technology and circuit design

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Outline

Introduction to organic electronics

PMOS project

OTFT technology

Open problems and modelling challenges

OTFT device model development

Conclusions and future work





Organic Electronics

- Fast development of organic electronics is supported by applications that require low cost electronic circuits covering mechanically flexible large areas
- These include e-skin, e-paper, e-nose, smart-fabrics, flexible displays, printed electronics or radio frequency identification tags (RFID).



• Organic electronics can be fabricated using faster and cheaper processes

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Basis of the future organic electronic circuits are organic TFTs (OTFTs).



Organic Electronics Forecast and Opportunities

- Organic electronics will be a \$30 billion business in 2015 mainly due to logic, displays and lighting.
- It will be a \$250 billion business in 2025, with major sales from logic/memory, OLED displays for electronic products, OLED billboard, signage, non-emissive organic displays, OLED lighting, batteries and photo-voltaics
- Organic lighting will severely dent sales of both incandescent and fluorescent lighting in the second decade from now.
- Organic electronics in the form of electronic billboards, posters, signage and electronic books will revolutionize the conventional printing and publishing industry.
- The future organic market will be newly created without replacing much from the inorganic semiconductors in existing electronics products.

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A Challenge for Electronic Design Automation (EDA): Organic Electronics



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- Inorganic semiconductor industry relies extensively on EDA software to support the iterative cycles of process, device and circuit technology improvements.
 - To further develop organic electronics industry, equivalent design tools are needed.
 - EDA tools essentially depend on numerical and analytical process and device models which are, in case of OSCs, not yet matured and quite sparsely implemented in commercial EDA tools.
 - **Cambridge Display Technology** (CDT) and **Silvaco** have joined forces together in a TSB funded project entitled **PMOS** to enhance EDA tools for use in the organic electronics and **to help move organic transistor technology from the lab to the shop floor**.



PMOS Project

On Physical Modelling of Organic Semiconductors

Project partners

- Cambridge Display Technology (CDT)
 - Expert in polymer light emitting diode (PLED) technologies
 - Leader in development of solution processable (printable) organic semiconductors for display fabrication
 - Expertise in development of PLED materials and deposition processes
- Silvaco
 - Leading provider of TCAD and EDA software for IC design
 - Provides established products for TCAD process and device simulation, spice parameter extraction, circuit simulation, custom IC design and verification

Project activities

- Device fabrication/measurements/testing
- TCAD model development
- Spice model development
- Measurements and modelling of device reliability and aging effects
- The **focus** is on **display device (oled) drivers** as these will be the first large scale organic semiconductor products.





OTFT Requirements for OLED Backplanes

OTFTs offer the potential to reduce cost and increase functionality of OLED backplanes.

- Device performance requirements:
 - Mobility (>0.5cm²/Vs with 10μm channel)
 - Contact resistance (<5kΩcm)
 - On/Off ratio (>10⁵)
 - Swing (<1 preferred)
 - Threshold voltage (<0)
 - Current and bias stress stability (mobility and V_{th})
- Process requirements:
 - Low cost: Development of novel solution processing and self-aligned processes
 - Thermal stability in combination with low-T processes (planarisation, OLED fabrication, etc...)
 - Air stability preferred for ease of fabrication (But: OLEDs require encapsulation)







OTFT Architectures and Peculiar Features



- OTFTs can be fabricated in different device architectures
- OTFTs are commonly realized using an **OSC** layer **without** a deliberate **doping**.
- Carriers that contribute to the charge distribution and transport in OTFTs must be injected from the metallic contacts.
- Without particular semiconductor type of the OSC layer, OTFT can operate in the electron or hole carrier accumulation mode depending on polarity of the gate voltage and capabilities of the contacts to inject particular carrier type.
- The source and drain have no junction isolation. A drain/source leakage current is limited by intrinsic OSC conductivity and contact resistance rather than reverse junction current.
- Contact resistances often dominate the OTFT performance and represent a bottleneck to achieve full potential of the intrinsic transistor effect.
- OTFTs are typically characterized with much lower intrinsic carrier mobility then their inorganic counterparts.





CDT OTFTs: Architectures/main fabrication steps

CDT explored two device architectures

Bottom gate (BG) bottom contact OTFT

- Gate created by photolithographic patterning of ITO coated glass substrate
- Spin coating of dielectric
- Thermal evaporation of gold contacts through shadow mask
- Before spin coating OSC, selfassembled monolayer treatment is performed (SAM) to ensure matching of energy levels between gold and OSC
- Device encapsulation

Evaporation of gold (Au) source-drain

Top gate (TG) bottom contact OTFT

- contacts onto the glass substrate
- Spin coating of organic semiconductor (OSC) onto the surface
- Before spin coating OSC, selfassembled monolayer treatment is performed (SAM) to ensure matching of energy levels between gold and OSC
- Spin coating of dielectric
- Gate (Au or AI) evaporation
- Device encapsulation





CDT OTFTs Device architecture: pros and cons

Bottom gate bottom contact OTFT

- (+) Wider range of solution processable dielectrics is available
- (+) Smooth dielectric/OSC interface
- (-) Low area for charge injection/extraction in bottom contacthigh contact resistance
- (-) Less manufacturable due to S/D patterning on top of dielectric or OSC

- Top gate bottom contact OTFT
- (+) Larger injection area smaller contact resistance
- (+) More manufacturable
- (+) Dielectric layer provides some level of encapsulation for the OSC
- (-) Dielectric/OSC interface may be more rough
- (-) Limited number of solution processable dielectrics available



CDT OTFTs: Top Gate Architecture and Materials

- Focus on top gate OTFT architecture
 - Avoid damage to critical OSC / dielectric interface
 - Lower R_C (greater injection area)
 - Novel process development to simplify top gate processing

Fluoropolymer Gate Dielectric (< 250nm)

- Fluorosolvent: "orthogonal" to OSC
- Good interface with OSC
- Low-k

"Encapsulates OSC"





High Throughput Testing

- CDT has applied PLED experience to develop equipment and analytical software for high-throughput automated OTFT testing
- 1" OTFT test cell has 12-20 OTFTs. >450 OTFTs measured in a single experiment
- Enables averaging of important parameters
 - Decisions based on sound judgements rather than max. data
- Spread of effective mobility primarily due to different channel lengths
 - (L 10 200 μm): Extraction of contact resistance by linear extrapolation





Organic TFTs Modelling challenges/open problems





Density of States and Carrier Concentration



Trap Limited Transport in Organic TFTs



Multiple Trapping and Thermal Release



- Dominant in well-ordered OSCs (molecular crystals)
- Thermally activated mobility
- During the transit in the delocalized band, the charge carriers interact with the shallow localized levels through trapping and thermal release
- The main reason why the standard semiconductor band model fails in OSCs is that it does not account for the **polarization**

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Variable Range Hopping (VRH): *Miller-Abrahams VRH Rate and Network*



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VRH Mobility: *Effective Transport Energy*

 $E_j = E_{tr}$ A carrier will most probably jump to a site at socalled *effective transport energy*

$$\mu_{n} = \frac{\mu_{n}}{D_{n}} D_{n} = q \frac{1}{n} \frac{\partial n}{\partial E_{F}} \left\langle v_{ij} \right\rangle \left\langle R_{ij} \right\rangle$$

$$\left\langle v_{ij} \right\rangle = \frac{v_0}{n} \int_{-\infty}^{E_{tr}} g(E) f(E, E_F) \exp\left(\frac{E - E_{tr}}{kT}\right) dE \qquad \left\langle R_{ij} \right\rangle = \left(\int_{-\infty}^{E_{tr}} g(E) dE\right)^{-1/3}$$

$$\int_{-\infty}^{E_{\rm tr}} g(E) [1 - f(E, E_F)] (E_{\rm tr} - E)^3 dE = \frac{6}{\pi} (\frac{kT}{a})^3$$



VRH Mobility: *Percolation Theory*



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VRH Mobility: *High Electric Field*

$$\mu_n(F, n, T) = \mu_n(n, T) \exp\left(\frac{\delta\sqrt{F}}{kT}\right)$$
$$F < 2 \cdot 10^6 \frac{V}{cm}$$

- Empirical model obtained fitting Monte-Carlo numerical experiments.
- For higher electric fields the mobility saturates and decrease with electric field intensity.
- In OFET modeling it is important to separate the vertical and lateral electric field components.







OTFT Model Development

Compact modelling (parametric) TCAD modelling (numerical)





Compact Modelling of Organic TFTs

- Compact models are essential for the design of driving electronic circuits in active matrix displays (or any other application) based on organic semiconductors using Spice-like circuit simulators
- Generic compact model parameters are extracted directly from measured (or simulated) device characteristics
- The models should accurately represent the static and dynamic device electrical characteristics for all possible circuit operation biases and temperatures
- Most of the existing inorganic Mosfet compact models are not suitable for organic TFTs since they:
 - do not consider the accumulation operation mode,
 - do not account for the trapped carrier charges and transport and
 - employ only the silicon specific mobility and resistance models
 - are overloaded with modelling features irrelevant for organic TFTs (junction models, short- and narrow-channel effects, ballistic transport, etc.)





Channel Sheet Charge: Surface Potential Equation



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Exponential DOS carrier concentration

$$n = n_i(T) \exp\left[\frac{q(\varphi - \varphi_n)}{kT_0}\right]$$

Accumulation operation mode

$$(V_G - V_{FB} - \varphi_s)^2 = V_{t0} \gamma^2 \cdot h \left(\frac{\varphi_s - \phi_n}{V_{t0}} \right)$$
$$\gamma = \frac{\sqrt{2q\varepsilon_s n_i(T)}}{C'_i}$$
$$h(x) = \exp(x) - x - 1$$
$$Q'_C = -C'_i (V_G - V_{FB} - \varphi_s)$$

There is an approximate analytical solution (Gildenblat, et al., IEEE J. SSC, 2004)

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Channel Sheet Charge: Unified Charge Control Model



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Sheet Channel Conductivity

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Parametric approach SOTFT - Surface potential based OTFT model

- A surface potential based compact model for organic TFTs (SOTFT) has been developed
- The model provides physical description of the currents and charges based on the accurate evaluation of electrical potential at the insulator-semiconductor interface
- It employs the physical mobility description based on exponential DOS and variable range hopping transport



Parametric approach UOTFT - Universal charge based OTFT model

- Universal OTFT (UOTFT) spice model has been developed suitable for all analogue, digital and RF circuit design.
- It uses basic principles and ideas from M Schur's universal models
- Model combines universal charge based field effect transistor modelling with OTFT specific channel charge, mobility bias, temperature dependences, and nonlinear contact resistances.
- Main model features include:
 - Suitable for all modes of device operation (static, dynamic, noise) and a large variety of OTFT device architectures, material specifications and fabrication technologies.
 - Physical temperature scaling of model parameters (based on exponential distribution of traps and the percolation theory for the conductance in disordered materials)
 - Geometry scaling
 - Universal mobility law based on variable range hopping (VRH) theory and OTFT operation in the channel accumulation mode
 - Source and drain series resistances







Parametric approach Equivalent Circuit





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Numerical approach TCAD modelling

- TCAD modelling has been used to validate the compact modeling and enhance understanding of the charge transport phenomena
- Implementation in the Silvaco's Device Simulator ATLAS includes:
 - Exponential and double Gaussian built-in DOS distributions
 - Arbitrary user defined DOS distributions
 - SHR statistical distribution of the state occupancy
 - The VRH model based on the effective transport energy
 - Poole-Frenkel electric field dependent mobility model
 - Steady-state and transient recombination models
 - Bimolecular Langevin Recombination Model







TCAD - Simulated Structure

- Fully Conformal Structure Developed in *Athena* (2D Process Simulator)
- Dimensions aligned to physical device dimensions
- TCAD Simulations focused on Top-Gate Bottom Contact devices due to improved experimental performance



Magnified Gate/Oxide/OSC/ Drain - Conformal Deposition of OSC





TCAD - Current Transport

- Electrical Characteristics and DOS profiles extracted/defined in *Atlas* (2D/3D device Simulator with dedicated organic models)
- Multiple Trapping and Release Transport type model Used
- DOS profile modeled using an exponential + Gaussian function
- 16.3 % Error achieved in comparison





TCAD - Current Voltage Characteristics



 Thus enabling pre-manufacture investigation of concepts and the effect of device geography for example

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TCAD - Current Density as a Function of Gate Bias



Parameter Extraction in UTMOST4

- UTMOST4 represents the next generation in SPICE model optimization software.
- Provides an easy to use tool for the generation of accurate, compact models and macro-models
- Family of advance global and local optimisers
- Unlimited model or macro-model complexity
- Any combination of data can be used



Compact model evaluation SOTFT and UOTFT model performance

- The performances of SOTFT model and UOTFT model are verified with measured advanced OTFT device structures and related TCAD organic simulations in ATLAS.
- UOTFT model is implemented into Simucad's model library and made accessible as a TFT model level 37.
- Equivalent circuit and external components match the existing inorganic TFT models (level 35 and 36).
- UOTFT model performance is verified on various OTFT technologies and device architectures.
- Figures in the following slides compare the simulated with the measured data from the bottom-gate bottom contact OTFT device (for both models)







Compact model evaluation SOTFT (BG)







Compact model evaluation UOTFT (BG)



Comparison between simulated (lines) and measured (circles) transfer characteristics of the OTFT in the linear operation region with Vds=-3V (blue line and circles) and saturation operation region with Vds=-30V (red line and circles)

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-0.01 -0.02₹ -0.03 £ ⊻ _0.04 000000000 -0.05 -0.06 -0.07 -40 -35 -30 -25 -20-15 -10 -5 D Vds (V)

Comparison between simulated (lines) and measured (circles) output characteristics of the OTFT for Vg=-10V, -20V, -30V and -40V.





Temperature Scaling UOTFT (TG)



Comparison between simulated (lines) and measured (circles) transfer characteristics of the OTFT in the saturation operation region at different temperatures: T=270K (dark blue) T=280K (light blue) T=300K (green) T=310K (pink) T=330K (red)





Conclusions

- EDA tools with accurate and predictive physical OTFT models are crucial for speeding up the optimisation of device performance and enable organic circuit design
- Demonstrated that application of advanced models for a charge transport and mobility behaviour in Atlas can provide accurate physical modelling of OTFT devices
- TCAD model development
 - Explores the effect of design parameters and performs optimisation procedure
 - Enables testing of a layout and all geometry, material and process related issues
- Compact model development
 - Developed compact models can provide a very good fit to the measured transfer and output device data at various temperatures







Future works

TCAD

- Investigate a computationally reasonable approach to incorporate percolation theory mobility models with arbitrary DOS distribution for TCAD device modeling
- Mixed mode simulation
- Aging

Compact modelling

- Extend a model to account for the bias dependent contact resistances, gate tunelling, effect of interface trap states
- Model a dynamic device behaviour
- Handle aging and hysteresis of the OTFT characteristics within the model and the corresponding circuit design







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