The Development of Device Lithography

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Invited Paper

Abstract—**Lithography has been the principal pacing element in the development of complex integrated circuits. Although major programs in electron-beam lithography and X-ray lithography have developed new systems with smaller feature capability, the optical systems remain the only candidates for large-volume device production. Scanning and step-and-repeat optical systems have been developed for the next generation of devices with 1-μm features. Electron beams are used for mask fabrication and direct exposure of special devices of exceptional value or for prototypes. X-ray and ion systems are being developed for future devices.**

Introduction

DEVICE LITHOGRAPHY has been the principal pacing element in the growth of very large scale integrated circuits. In spite of a tremendous development effort, the resolution, registration between levels, and defect density of the lithography have limited the device complexity. This is not to say that the lithography has not improved. The complexity of integrated circuits has almost doubled every year since the early 1960's when they were invented, so that 500 000 active components is a reasonable goal for new devices today. There is a major economic value in increased scale of integration in eliminating interconnection cost, reducing system device cost, and increasing system reliability. During the past ten years, integrated electronics systems cost has been reduced by one hundred and the reliability increased by the same factor for a given function.

This paper presents a general review of the mainstream of lithographic system developments of integrated circuit patterning. It is neither detailed nor complete but will give a general background for the papers that follow in this issue.

Integrated Circuits

Integrated circuits grew out of the previous transistor technology when a means of isolating two or more transistors on a single substrate of silicon, and interconnecting them to perform a more complex function, was developed. The planar geometry, with layers on a flat silicon surface, permits the use of device lithography to pattern the successive layers that make up the three-dimensional structure. A layer of insulator, conductor, or mask material to control the diffusion of impurities into the silicon is deposited on the surface of the wafer and covered with a radiation-sensitive resist (commonly a photoresist). After the resist is exposed with the pattern for the layer of the device, the developer solution dissolves the pattern regions leaving a mask to control etching of the layer beneath. This process is used for six or more accurately registered layers to form the discrete transistor areas, isolate them from each other, and interconnect them to form the desired circuit.

The features in early integrated circuits had minimum dimensions of five or ten thousandths of an inch (before metric) and a chip was as large as a tenth of an inch across. The pressure for more complex circuits has pushed the feature size down to a few thousandths of a milimeter and the chip to as large as 10 mm on a side. Thus the features have shrunk by a factor of ~60 in each dimension and grown by ~10 in area permitting the growth in complexity.

When the size of the features goes down and the area of the chip increases, both the defect density and the size of the defects must go down to achieve an adequate yield of good devices.

Historical Development

The history of lithographic system development contains a continuing series of bottlenecks that have limited performance. As new development has cleared each of these problems, it has moved the bottleneck to another area of the technology.

The early integrated circuits were patterned with contact printing on photoresist using printing industry techniques to prepare the mask. Each layer of the device was laid out on graph paper at between 50 and 500 times final size and then cut into a plastic material called Rubylith. A red layer on the transparent substrate was cut so it could be peeled off in the pattern areas. The pattern was then backlighted with the mercury lamps in a printing plate camera and reduced to 10 times final size on photographic glass plate. This 10X reticle was then reduced to final size in a special step-and-repeat camera that exposed an array of identical images. A 10X microscope objective was commonly used for the reduction lens in these cameras.

Contact copies of this master mask were then used in a contact printer to expose the photoresist coated wafers. The masks were pressed hard against the wafer using vacuum to even out the flatness errors in both substrates and obtain good contact. Where the mask emulsion and photoresist were pushed hard together, particles of emulsion adhered to the photoresist leaving particles on the wafer and holes in the mask that were propagated with further exposures. The probability of having a fatal defect on small chips with large features was small enough to give adequate yields. As chip size grew and defects became more critical, each mask copy was used for fewer exposures; as low as 10 wafers in critical cases.

Pattern Generators

As the device patterns increased in complexity, the layout of the devices and cutting of Rubylith became a bottleneck. Automatic plotters and coordinatographs with knives were

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developed to cut the Rubylith from data on punch cards, but the patterns still had to be peeled.

Photographic pattern generators were later developed that used an X-Y table and an adjustable rectangular aperture illuminated with a flash lamp to expose photo artwork from computer tape inputs.

Projection Printing

As the defect density and yield became a critical problem, two systems were developed to avoid contact defects. One system is proximity printing, where the spacing between the mask and wafer was increased to ~10 μm. This results in lower contrast and some distortion of features because of diffraction effects. Proximity printing was very successful on the less critical levels.

Projection printing was tried using a lens at 1–1 magnification to image a standard mask onto a small wafer. The resolution was poor and the resulting linewidth errors caused as much yield loss as the contact defect density. The best conventional lens will resolve about 10^8 pixels over its field, so that it can well resolve a single chip but not a whole wafer pattern.

Micralign System

A novel optical system was developed in 1973 that changed this resolution limit. A system of spherical mirrors was used to form a narrow ring of aberration-free imagery. The wafer was moved past an arc of this ring image while a mask was moved in synchronism at the object end. An arc of the mask was illuminated and imaged onto the wafer so that by scanning once across the wafer, the whole image was exposed. This system was extended over the years so that it would image 2-μm features over a 4-in diameter wafer at a rate of ~40 wafers/h. This is 5×10^4 linear resolutions or 25×10^8 pixels in the whole image. These Micralign systems quickly became the principal lithographic tool in the industry because of the uniformity of resolution and illumination as well as the high throughput (see Fig. 1).

With the lower defect density provided by projection printing as well as improvements in the materials and processing of the wafer, chip complexity increased to the point where many hours were consumed in producing the initial reticle pattern for the chip, and defects introduced in the photographic materials used in the many steps of this process became significant in terms of yield.

Electron-Beam Pattern Generation

Electron beams have long been considered an obvious technology for high-resolution direct wafer exposure and this will be considered later in this paper, but electron beams were first applied to the pattern generation problem (see Fig. 2).

An electron-beam system (EBES) was developed in 1972 that highlighted the speed and accuracy of electron beams for patterning a final mask in a single step with lower defects on an economical basis. The speed of deflection and blanking of the electron beam combined with the ease of coupling the electron-beam system to computers contributed to the high throughput of the system for very complex patterns.

The use of a small deflection field combined with a laser interferometer measured stage achieved the dimensional accuracy required for the more complex and smaller feature devices. A raster scan on a continuously moving stage was used to write at a 40-MHz address rate directly on the electron resist over a chrome-coated mask substrate. These electron-beam

Fig. 1. The scanning projection printer has been the principal wafer exposure tool.

Fig. 2. An electron-beam mask exposure system can generate complex patterns efficiently.

pattern generators were used to push defect density down to ~2/cm² and write most final masks in the late 1970's in ~20 min. Since that time, the machines have been upgraded to give 0.1-μm address capability in addition to the previous 0.25 or 0.5 μm and accuracies of 0.05 μm to keep up with new requirements. The larger number of 0.1-μm addresses in a 5-in mask area and the complexity of ~5 million features per chip is pushing up exposure times. Improved systems are continually being developed.

Lithography for Today

The forefront of commercial lithography today is at 2-μm minimum features on 5-mm to 1.0-cm long chips on a 4- to 6-in wafer. The older Micralign machines that have been the mainstay of the industry are pushed to the limit to meet the submicron registration required between levels. The next generation of devices will shrink to 1–1.5-μm features and will require a new generation of lithography that is now emerging.

Step-and-Repeat Optical Lithography

In anticipation of the tighter requirements, many companies have developed step-and-repeat cameras for direct wafer expo-

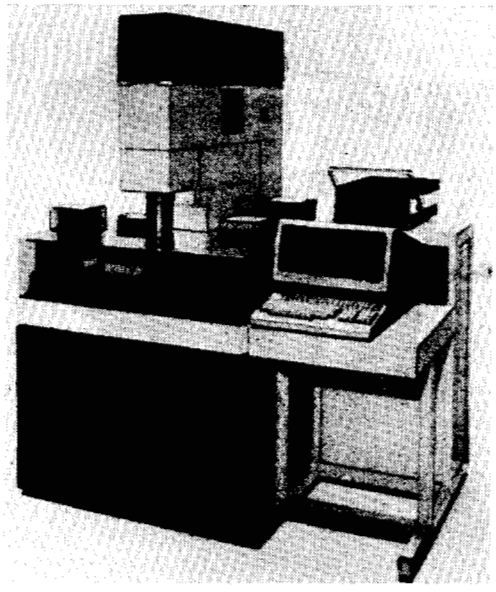

Fig. 3. A high-technology Censor Step-and-Repeat camera uses alignment on every exposure.

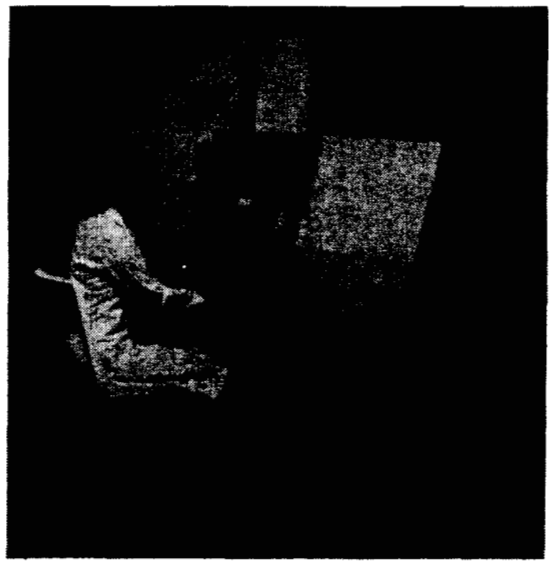

Fig. 4. A new scanning printer will expose 100 5-in wafers per hour with adjustable magnification.

sure (see Fig. 3). These systems use a very-high-quality lens to image as small as 1-μm features over a chip area of about 1 cm square at 10 times reduction. A fast stepping table with laser interferometer measurement is used to expose at rates in excess of one field per second. The high numerical aperture of the >13-element lens gives a better ultimate resolution than the Micralign systems can. Registration accuracy can be achieved using a single alignment over the wafer and dependence on the interferometer for stage position control, or alignment can be done on each chip of the wafer. The reduction ratio of the lens makes the reticle generation easier.

The problems with step and repeat are in defects and throughput. Any defect on the reticle will be printed onto every chip on the wafer. Thus if there is a particle of dirt or fatal defect on the reticle for exposure of any level of the wafer, the yield may drop to zero. Thin transparent pellicles mounted over the mask can eliminate the dirt problem. On recent systems a reduction ratio of 4 or 5 has been used so that two adjacent patterns can be written on the reticle and compared for defects in an automatic inspection system.

The throughput of step-and-repeat systems is limited because of the large number of steps required to fill the wafer. If the chip size exceeds a quarter of the area of the field, it may be necessary to expose them one at a time, pushing up the exposure time. A throughput of 30 to 40 5-in wafers per hour is about the best that can be expected in usual commercial production.

New Micralign Systems

Two new Micralign systems have been developed to meet the new requirements. The optics for the Micralign systems has been improved using phase measuring interferometry to reduce the registration tolerance to below 0.5 μm for exposure of 4-in wafers.

A new Micralign system has been developed to cover a 5-in wafer with better registration and to permit automatic adjustment of magnification in both coordinates, as part of the automatic alignment procedure. The machine uses a double optical system of the concentric spherical mirror type with some fused silica elements to obtain a wider annulus of aberration-free imagery. This reduces the exposure time so the system will expose 100 5-in wafers per hour with 0.5-μm registration tolerances (see Fig. 4). Because the numerical aperture is less than the step-and-repeat lenses, the minimum feature is 1.25 μm in visible light, but the system can be used with UV exposure for submicron features. The use of UV also results in greater depth of focus compared to visible light systems of the same resolution.

Tomorrow's Lithography

It has been assumed, since the early 1970's, that optical systems were at the limit of their performance and would be replaced within a few years. Since resolution was assumed to be the basis for that limit, shorter equivalent wavelength systems were proposed and developed. In actual practice, the limits turned out to be in registration and linewidth control. It is clear that the choice of the next generation will be between the optical step-and-repeat and scanning systems. The major problem is economic. Semiconductor manufacturers have a surplus of lithographic capacity but very little capacity for the next generation. Step-and-repeat cameras and advanced Micralign systems each cost about a million dollars with automatic alignment and loading. This is in comparison to $20k for a contact printer in the early days and $200k for a projection printer a few years ago.

Industry is being forced to commit funds to new systems because the capacity in the equipment industry will not be able to supply the demand when business turns up. At these costs, the lithography has become the most expensive part of the process. Step and repeat has somewhat more resolution in the visible, but the scanning systems have a clear edge in capacity per dollar.

Alternate Technologies

Alternate technologies have been in development for many years. Many electron-beam systems have been designed for production use including beam scanning systems, image projection, and array systems with multiple sources. X-ray sensitive resists, sources, and exposure systems have been developed along with the critical X-ray masks. Ion systems are newer but have promise.

Electron-Beam Direct Wafer Exposure

Electron beams have long been the wave of the future for wafer exposure. The high resolution of electron beams, combined with fast deflection and computer control, all favor this technology.

Experiments were done in the late 1960's using scanning electron microscopes to expose a few high-resolution devices with excellent results. The electron beam was used to sense alignment marks and registration was superior to that of any other lithography. Many groups developed systems aimed at practical commercial production of devices.

Electron optics, with deflection fields of 5 to 10 mm at high deflection speeds, were developed. Variable beam shaping systems to expose an adjustable rectangular spot at one time were devised. Vacuum stages for rapid and accurate positioning of the wafer with laser interferometer measurement were designed. Data systems to describe the device features and feed signals to the system at the required rates were constructed.

There were some limitations on the performance of these systems. LaB_6 cathodes and thermal field emission sources were developed to achieve very high writing rates, but electron interactions in the beam limit the total current that can be used. Proximity correcting computer programs were required to compensate for the scattering range of the electron in the resist and back from the substrate to avoid distortions of the features below 2 μm.

The majority of these systems write at address rates between 40 and 500 million addresses per second and will expose up to ~6 wafers per hour with ~1-μm features. The systems have been used to make special devices that have extraordinary value because of device speed, small volume custom devices, or prototype devices for design confirmation (see Figs. 5 and 6).

The cost of these systems, in the range from 1-4 million dollars, and the moderate throughput limits their ability to economically produce catalog circuits. Further, there would not be enough capacity to produce such systems or capital to fund such systems to meet a significant fraction of the device production capacity in the foreseeable future.

Some electron-beam systems attempt to form the image of a mask rather than modulate a scanned beam. ELIPS is a system using a photocathode as the patterned source with a homogeneous magnetic and electrostatic field to image the electrons onto the resist-coated wafer. The system has improved continually for over 10 years but has always missed the moving target in resolution and registration.

A number of systems have been developed that use an array of parallel beams on a wafer or an array of lenses to form multiple images of one beam to write the array of identical chips on the wafer. These systems are a possible solution for the future but many practical problems make them improbable. There is a need for more invention in this field.

X-ray Systems

X-ray lithographic systems use the beam diverging from a small X-ray source to form a shadow image of an X-ray mask onto an X-ray-sensitive resist-coated wafer. At the X-ray wavelengths, the wafer can be spaced up to 50 μm from the mask to avoid contact. Wavelengths between 4 and 20 Å are used to have sufficient transparency in the mask substrate, sufficient opacity of the mask pattern, sensitivity of the resist and, in some cases, enough transmission through a beryllium window in the X-ray tube and through a helium atmosphere to permit exposure at atmospheric pressure. Many mask materials have been used as the substrate including silicon, boron nitride,

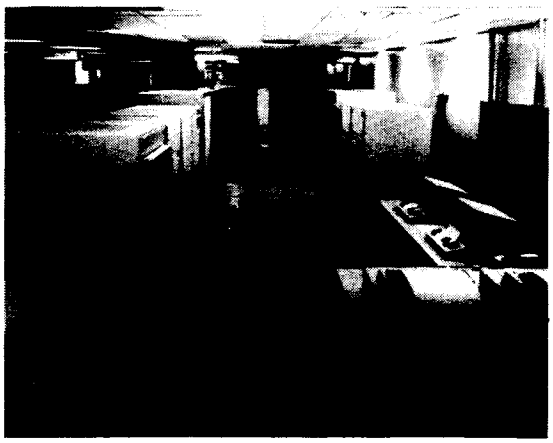

Fig. 5. The IBM EL-3 system is used for fast turnaround in electron-beam patterning of prototype devices.

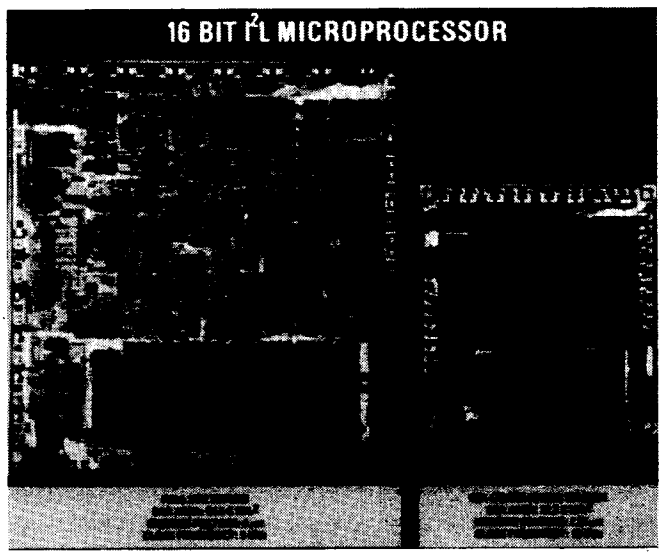

Fig. 6. Texas Instruments uses electron-beam exposure to achieve smaller features, more chips per wafer, and faster device operation.

and other polycrystaline films, metal films, and plastic films. Most substrates are only a few microns thick and must support a 1-μm-thick pattern of gold or other metal.

Some X-ray masks are transparent in the visible so optical alignment techniques can be used. The scattering range of the X-ray-generated photoelectron in the resist is only ~500 Å so resolution can be higher than electron lithography.

The major problem has been in devising a sensitive enough resist combined with a reliable bright source to give exposures of less than a minute. Also, small uncontrolled distortions in the mask substrate during and after patterning have caused significant distortions in the pattern.

X-ray systems have been used to make many devices with 2-μm features and a few in the 1-μm range. As the resolution and registration tolerances have tightened to keep ahead of the growing optical technology, the X-ray mask distortions for full field exposure have improved, but have continued to be a problem. With current registration tolerances in the 0.1-0.2-μm range, smaller X-ray masks with step-and-repeat exposures of large wafers are being studied.

The use of step and repeat will complicate the X-ray system and increase its cost compared to that of other lithographic systems.

Ion Exposure Systems

Ion beams can be used to expose resists in both the scanned beam system, comparable to electron beams, and in mask exposure systems, using crystaline substrates as in the X-ray systems. The critical question is the flux of ion beam and the sensitivity of the resist. Ions should have a shorter range in the resist and not suffer from the proximity effects as much as electron beams.

There is the possibility to use ion beams of desired materials for direct implanting of impurities in the silicon substrate. With existing beam intensities, this would be limited to a small fraction of the area to be economical. Ion systems are in a very active stage of development and results are awaited with great interest.

Future Directions

Once again the next lithography will depend on optical systems because the alternate systems are not ready. At some point, the optical resolution will be insufficient and other technologies will be required. The VHSIC military program supporting electron and X-ray lithography for making large, complex, fast processors for military applications may bring these technologies to the point of successful commercial application and extend the lithography once again.

Resists for Fine-Line Lithography

MICHAEL HATZAKIS

Invited Paper

Abstract—**Resists are radiation-sensitive materials used in the fabrication of integrated circuits (VLSI) for imaging the desired pattern onto the silicon wafer. Most resists in use today consist of polymeric solutions that are spin-coated onto the silicon wafer, exposed in a lithographic tool, developed, and completely removed after the pattern has been transferred to the substrate. This paper presents a historical development of resist materials, present uses of resists, and future requirements, dictated primarily by developments in lithographic tools.**

Introduction

THE NEED for decreasing the device dimensions in memory and logic circuits has been emphasized already in numerous papers, including papers in this issue. This need is driven by two primary factors; decrease in cost by increasing the number of devices per chip and/or the number of chips per silicon wafer, and improvements in circuit performance by reducing the device capacitance and shortening propagation delay time. One of the primary limitations in the manufacturing of smaller devices has always been lithography, which includes lithographic tools and resists and processes. Since lithographic tools are quite adequately covered in a separate paper in this issue, I will attempt to cover the development of resists and processes that have contributed significantly to micrometer and submicrometer device fabrication. Although large-scale fabrication of micrometer-size device circuits is not yet a reality, resists and processes are being extended to submicrometer device dimensions and the limitations today lie in economic factors, lithographic tools and masks, and device design optimization.

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Resist Definitions

Resists are temporary layers applied onto the workpiece only for imaging purposes. After pattern transferring onto the active layer (insulator or semiconductor material), the resist is removed (stripped) in a solvent or an oxidizing solution. The most common resists are organic solutions applied on the workpiece (wafer) by spinning and dried by baking at a suitable temperature, referred to as "prebake temperature." The thickness of the dried resist layer depends largely on the concentration of solids in the solution and on the spinning speed.

After baking of the resist-coated wafer, the desired pattern is exposed in a lithographic tool, and the resist is developed. The most important distinction between resists concerns the

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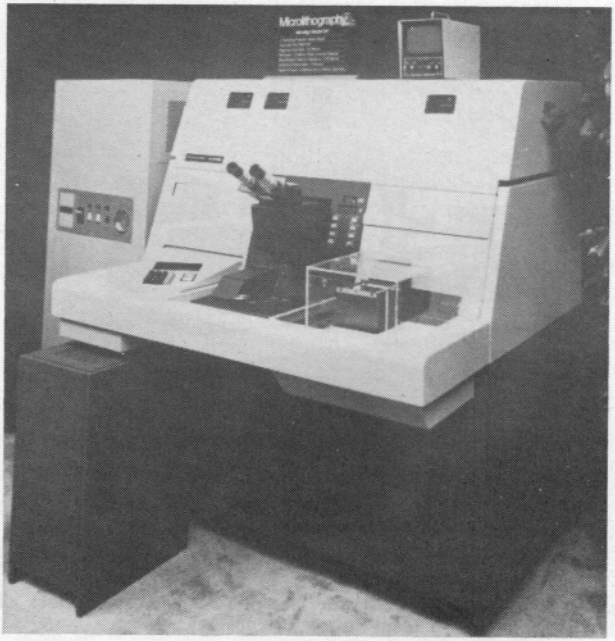

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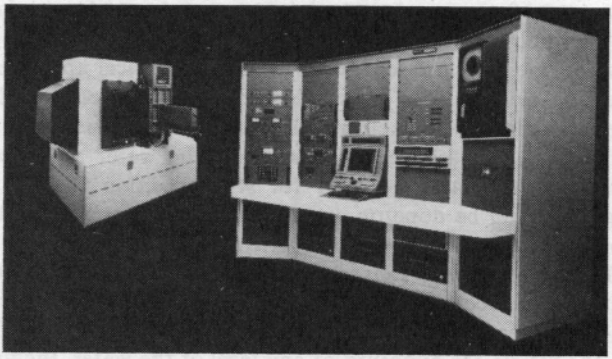


Fig. 2. An electron-beam mask exposure system can generate complex patterns efficiently.

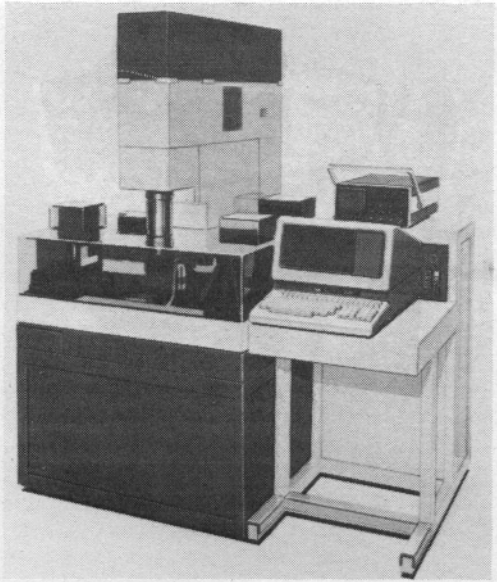
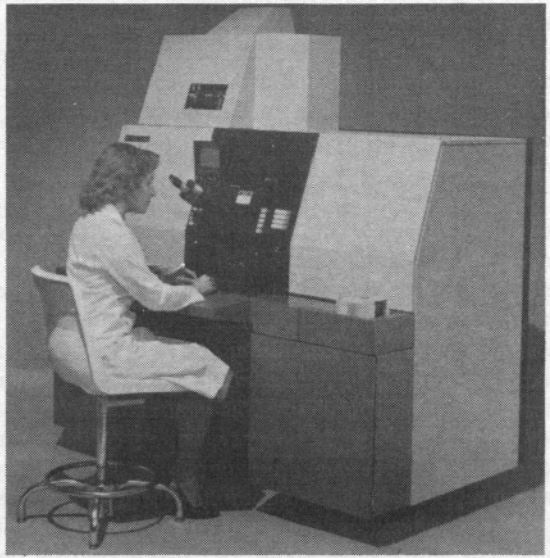


Fig. 3. A high-technology Censor Step-and-Repeat camera uses alignment on every exposure.



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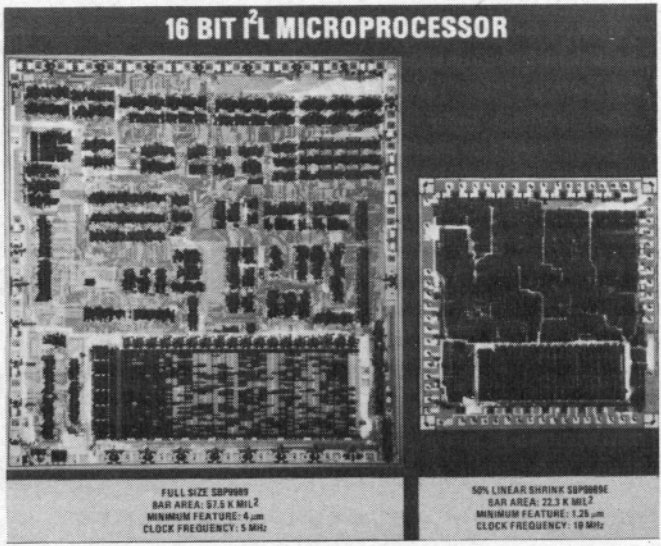

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