MEMS Infrastructure: The Multi-User MEMS Processes (MUMPs)

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ABSTRACT

In order to help provide access to advanced MEMS technologies, and lower the barriers for both industry and academia, MCNC and ARPA have developed a program which works to provide users with access to both MEMS processes and advanced integration techniques. The two distinct aspects of this program, the MUMPs and Smart MEMS, will be described in this paper. The Multi-User MEMS Processes (MUMPs) is an ARPA-supported program created to provide inexpensive access to MEMS technology in a multi-user environment. MUMPs is a proof-of-concept and educational tool to aid the development of MEMS in the domestic community. MUMPs technologies currently include a 3-layer polysilicon surface micromachining process and LIGA processes that provide reasonable design flexibility within set guidelines. Smart MEMS is the development of advanced electronics integration techniques for MEMS through the application of flip chip technology.

Keywords: MEMS, infrastructure, MUMPs, Smart MEMS, electronics integration, LIGA, cell library

2. INTRODUCTION

Over the last decade silicon process technology, synonymous with integrated circuit processing, has been increasingly applied to the field of micromechanics, leading to the emerging field of MEMS (microelectromechanical systems). The extensive characterization of silicon processes by the IC industry, integrated with silicon's high Young's modulus and yield-strength, high thermal conductivity and low thermal expansion coefficient makes it one of the best understood and well suited materials available for coupled electronic and mechanical applications.

MEMS is an enabling technology, which partially accounts for the projections of 10 - 20% annual growth and the potential of a greater than $8 billion market by the year 2000[1]. Current market estimates of approximately $800 million (1992/3) are possibly low since MEMS are already being incorporated into much more complex systems. Due to the enabling nature of MEMS and because of the significant impact they can play on both the commercial and defense markets, the federal government has taken special interest in nurturing growth in this field. One of the many ways this is being accomplished is through the MCNC MEMS Infrastructure program, supported by the Advanced Research Projects Agency (ARPA).

The MEMS Infrastructure program was established in 1993 to provide low-cost, easy access to advanced MEMS technologies. By lowering the barriers to accessing the technology, it is hoped that the cost (both time and dollars) of developing and incorporating MEMS into new applications will be significantly reduced. There are 3 key components to the Infrastructure program; the Multi-user MEMS processes (MUMPs), a publicly-accessible standard element MEMS library and the generation of Smart MEMS through the use of flip chip technology. The MUMPs and Smart MEMS activities are described below. The standard Element Library is analogous to the standard cell libraries that have been so important in aiding the advancement of the VLSI field. More information on the element library is available through the world-wide-web (URL listed in title header) or through email to camel@mcnc.org.

3. THE MULTI-USER MEMS PROCESSES (MUMPS)

As with integrated circuits, the cost of MEMS devices benefits from the leveraging of batch fabrication. Even so, the cost of micron-scale silicon processing is enormous. Building, maintaining and operating a cleanroom with knowledgeable workers can

0-8194-2005-0/95/$6.00

out price most universities as well as small and medium-sized companies with interest in developing and/or commercializing MEMS technology. Commercial prototyping services are available but the cost of developing a full prototype can easily exceed $250K. As is often the case, MEMS fabrication is too costly for individuals interested in experimenting with this technology. The result—broad dissemination of MEMS is difficult, limiting the pool of creativity contributing to new and potentially lucrative products. It is these access and cost barriers to MEMS development which prompted the establishment of the multi-user MEMS processes (MUMPs) program.

By providing an inexpensive route to MEMS fabrication technologies, the MUMPs program has filled two important niches. First, MUMPs provides cost effective proof-of-concept fabrication. This is particularly important for small (and even large) companies where R&D funds are limited and providing some kind of physical evidence beyond the "idea stage" is a prerequisite to further project funding. Once ideas have been displayed through the MUMPs process, users may wish to take their ideas further to the prototyping stage.

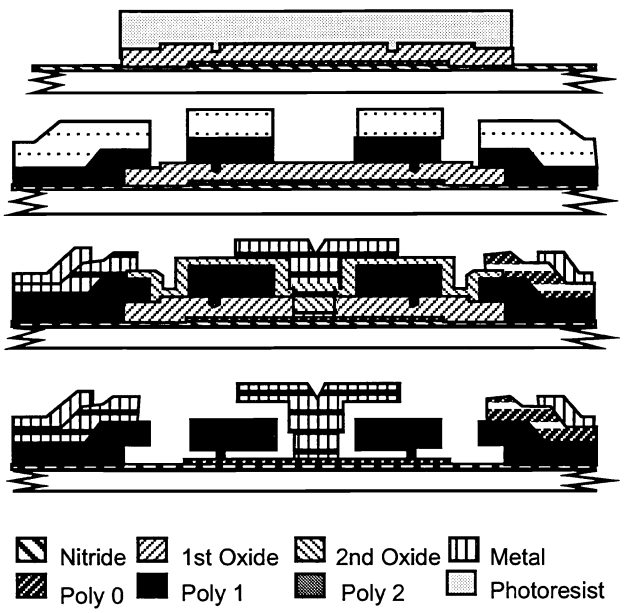
Second, MUMPs provides an excellent, low-cost, educational tool. Since MEMS is, in many ways, still in its infancy, there is plenty of room for growth. Many universities around the country are developing programs in MEMS. MUMPs allows the university to offer a course in MEMS without the financial burden of running a cleanroom facility. Small companies and government agencies interested in MEMS can benefit as well. No longer relegated to reading journals but never testing their knowledge, the low cost of MUMPs gives these individuals the opportunity to learn and experience more about MEMS technology before making the fiscal committment to a production run.

3.1 MUMPs Description

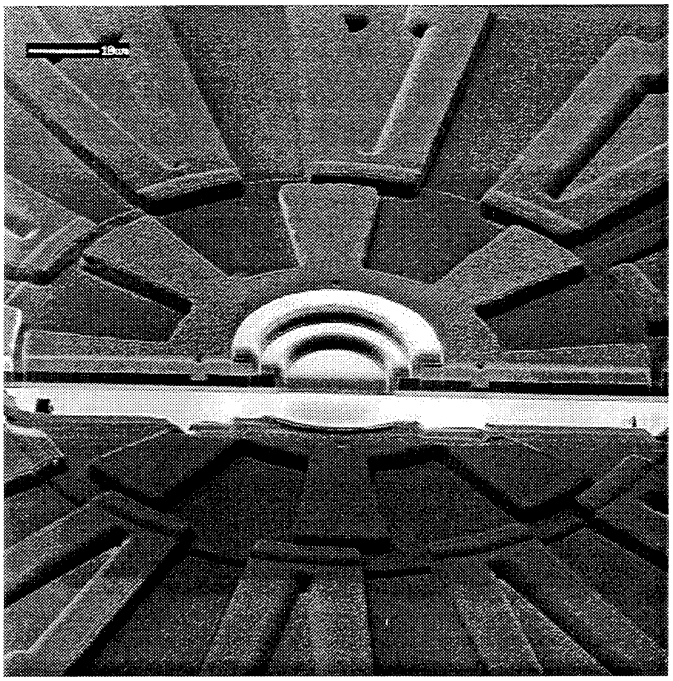
The MUMPs program currently offers access to two distinct MEMS technologies: polysilicon surface micromachining and LIGA (hereafter referred to as LIGAMUMPs), which is provided in conjunction with the University of Wisconsin. Polysilicon surface micromachining encompasses many of the same fabrication techniques as traditional silicon IC fabrication; layers of CVD films are deposited and subsequently patterned using photolithography and plasma etch techniques. Alternating layers of silicon dioxide and polysilicon are deposited so when all the layers have been patterned, the silicon dioxide can be etched away with hydrofluoric acid leaving only the polysilicon structures behind. The chief benefit to this process is the ability to fabricate moving parts on a silicon substrate. The MUMPs process provides two layers of structural polysilicon and a third layer of thin polysilicon that serves as an electrical ground plane or electrode. Devices fabricated in this way are typically several microns in thickness. With in-plane dimensions of greater than 500 μm, these devices can take on a two-dimensional appearance. Nevertheless, the mechanical strength of polysilicon films makes such structures surprisingly robust. The MUMPs process provides seven different films (layers) with which to build structures. These films are silicon nitride, poly 0, first oxide, poly 1, second oxide, poly 2 and metal. The purpose of the oxide and polysilicon films has been described above. The silicon nitride film is a blanket layer that serves to isolate all structures electrically from the substrate. The metal layer serves two purposes, it provides electrical contact to the polysilicon simplifying wire bonding and a reflective surface for optical applications. The process specifications and parameters are outlined in Table 1, while Figure 1 illustrates the progression of layers used to build a micromotor.

Table 1: MUMPs (polysilicon) process specifications

Mask Level	Nominal Size (μm)	Material	Comments
Poly 0	3.0	0.5 μm poly	Ground plane, low stress poly
Dimple	3.0	-	0.75 μm dimple into first oxide
Anchor 1	3.0	2.0 μm PSG	Creates poly 1 anchors
Poly 1	3.0	2.0 μm poly	Low stress, doped polysilicon, first structural layer
Poly1_Poly2 Via	3.0	0.5 μm PSG (2nd oxide)	Creates vias between poly 1 and poly 2
Anchor 2	3.0	2.5 μm PSG (1st & 2nd oxide)	Creates anchor for poly 2
Poly 2	3.0	1.5 μm poly	Second structural layer
Metal	3.0	0.5 μm metal	Au with Cr adhesion layer



(a)



(b)

Figure 1: a) MUMPs 3-layer polysilicon process flow cross-section (schematic represenation of micromotor) b) Focus Ion Beam cross-section of MUMPs fabricated micromotor (courtesy of NCSU AIF)

3.2 LIGAMUMPs

LIGA, a German acronym which translates to Lithography, Electroforming and Injection Molding, was developed in Germany in the 1980's and has slowly gained wide-spread interest. There are two key factors to LIGA's attractiveness - the ability to mass-replicate high aspect ratio structures out of metals, polymers and ceramics, and the ability to fabricate structures which can be assembled with a high degree of precision. LIGA requires the use of an extremely energetic, highly collimated photon source, which restricts its practice to those facilities with access to x-ray synchrotrons. This further exacerbates the access and cost issues mentioned above. The processes offered include releasable single level metal and plastic structures. As our experience with the technology increases, so too will the processes available as part of the MUMPs.

4. CONSOLIDATED MICROMECHANICAL ELEMENT LIBRARY

The Consolidated Micromechanical Element Library (CaMEL) is a library of MEMS cells and is similar to standard cell libraries that proliferate in VLSI design. The CaMEL library consists of two independent parts; the nonparameterized cell database and the parameterized micromechanical element library. The aim is to provide MEMS cell libraries that are useful for novice MEMS designers, as well as experienced ones. Both libraries are intended to *assist* the user in the design and layout of MEMS devices and it is assumed that the user will modify and customize these elements using a suitable mask layout editor.

The nonparameterized cell library is a database of MEMS designs in various process technologies contributed by different sources. It is a resource of working MEMS devices and structures. The library browser, DBRead, permits the user to peruse brief descriptions of the cells and select desired ones. The selected cells can then be retrieved from the database in either Caltech Intermediate Form (CIF) or CALMA GDS II format. A companion program, DBSubmit, allows designers to submit MEMS designs for inclusion in the database along with the accompanying process information. Both programs are written in the Practical Extraction and Report Language, PERL. Cells currently available in the library include designs for MUMPs, UCB 2 poly, and LIGA processes.

The parameterized micromechanical element (PME) library is a set of generators that allow users to create customized versions of commonly used elements in a quick and easy manner. The PME library also provides a framework for writing cell generators. It enables the generators to be relatively process independent and allows limited cell hierarchy. Designs can be generated in CIF, GDS II, or PostScript output formats. Technology dependent design rules are read in from an environment specified technology file. The library provides various geometric primitives and a set of available generators. Various types of elements are available, including active micromechanical elements, passive micromechanical elements, test mechanical structures, and electrical elements.

Rectangle, circle, sector, polygon, and wire drawing primitives are available in the PME library. Primitives can be generated with etch holes if they are parts of structures that will be released from the substrate. These primitives will generate the appropriate layout for the output format selected. Currently, these primitives are not directly accessible to the user and are only used within the library of generators.

The generators available in the PME library assume a two layer surface micromachined process . The process is assumed to have two structural layers, two sacrificial layers, and two electrical interconnect layers. Process specific mask levels and layer names are specified via a process file and compiled into the library. Technology specific design rules are specified in a separate technology file and accessed by the program at execution time. The generators have been written to conform to the technology specific design rules. However, all layouts generated by the library should be checked using an external design rule checker.
The PME input is provided in an ASCII text file and defines cells by calling generators with desired parameter values and then placing instances of defined cells at chosen locations within the top level cell. Instances of defined cells can be reflected, translated, or rotated through arbitrary rotation angles. The following examples illustrate typical use of elements available in the library.

The following example generates a linear comb resonator on the first structural layer (poly 1 in the MUMPs process) using the **lcomb1** linear comb drive and **lfbs1** linear folded beam suspension. The fingers in the comb drive are 4 μm wide with an airgap of 3 μm, and beams in the suspensions are chosen to 150 μm long and 4 μm wide. Figure 2 shows an input file and the layout generated by the PME library.

```
/* Linear comb resonator */
PME p1,p2;
/* Create comb and suspension */
p1=lcomb1(98,12,14,60,4,3,30,
        comb);
p2=lfbs1(150,4,50,12,30,25,12,
       98,suspension);
/* Place cells for resonator */
instance(p1,'*',0,0,75);
instance(p1,'*',0,0,-75);
instance(p2,'*',0,0,0);
```

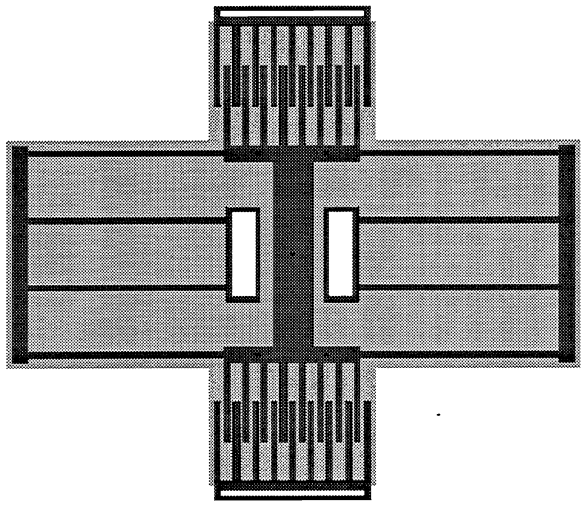


Figure 2. Linear comb resonator generated by the PME library using the input provided. The two comb drives are instances of the *cell* comb and the folded beam suspension is an instance of the cell *suspension*.

5. SMART MEMS: ELECTRONICS INTEGRATION FOR MEMS

There has been a growing interest in placing electronics closer to sensors and actuators to improve their performance. Among the several approaches that have been demonstrated are hybrids and embedded electronics. The hybrid approach, in which the different chips including electronics, sensors and actuators are placed in a single package and connected by wire bonding, has long been the industry standard. This approach is very flexible; there are few restrictions on the types of usable electronics and substrates. However, hybrids are not batch fabricated, can suffer from system performance degradation due to stray or large capacitance and also result in increased size of the integrated system[2]. A recent approach[3,4] has been to build MEMS sensors and actuators on top of underlying electronics on the same substrate. This embedded approach is suitable for batch processing and results in significant improvement of performance. However, it involves a fairly large number of processing steps resulting in increased processing complexity and reduced yield, which drives up the costs of production.

Flip chip MEMS combines the advantages of the hybrid and embedded approach. The electronics and the MEMS are fabricated on different substrates and are then connected using solder bumping. Flip chip has been successfully used to connect IC chips to printed circuits or substrate carriers for almost 20 years. In conventional flip chip attach, the IC chip is turned upside-down, i.e. *flip chip*, and an array of solder bumps on the chip are joined to a matching array of solder wettable pads on the substrate. This conventional approach has been modified to facilitate the connection of the MEMS chip to the electronics chip, taking into account the mechanical or 'released' nature of MEMS chips.

MCNC is a world leader in the development of flip chip process technology for MCM's, and is the site of the ARPA-supported Flip Chip Technology Center. As part of the MEMS Infrastructure program we are investigating the various issues involved in bump attaching both surface and bulk micromachined devices to different types of substrates, including silicon, quartz, Pyrex and GaAs. Methodologies for the handling of released MEMS structures and design rules are being developed to allow the MEMS community to access this advanced integration technique for the production of Smart MEMS systems.

5. 1 Flip Chip MEMS

A flip chip test chip has been designed and fabricated to start addressing the various issues involved in using flip chip attach for MEMS. The first test run includes a set of fabricated MEMS chips which have been flip chip attached to a corresponding set of substrate chips. On this first run the substrate die do not include electronics, since the issues of flip chip attach for IC's are well known; rather, the substrate die include standard pad arrays on the outside boundary for probing. These pad arrays are to be connected to the various pads of interest on the MEMS die through the solder bumps that join the substrate and the MEMS chip. Using these connections the MEMS devices can be electrically tested. Figure 3 shows a schematic view of how a MEMS die will be attached to a corresponding substrate die. In addition to providing bumps for electrical connection, dummy bumps have been provided to increase the mechanical strength of the joined chips. The MEMS die for this study are 1 cm x 1 cm, while the substrate die are 1.2 cm x 1.2 cm.

For the characterization run two MEMS processes have been used in order to include a wide variety of MEMS devices, providing the testing of flip chip bonded MEMS devices under different loading and handling conditions that are required by the type of MEMS device. One is a basic surface micromachining process similar to the MUMPs process up to first polysilicon, utilizing one structural layer of polysilicon and one sacrificial layer of PSG. Various stress and strain gauges, resonant structures, and other test structures have been designed using this process.

The second MEMS process combines surface micromachining with bulk micromachining. It uses one polysilicon structural layer, a PSG sacrificial layer and a bulk etch from the back. This combined surface and bulk micromachining process is being used to fabricate diaphragms and devices such as pressure and acceleration sensors. In addition, numerous substrate materials including silicon, Pyrex, quartz and GaAs are being investigated.

Issues that were investigated on this test run include 1) metallurgy for the MEMS devices compatible with the release process and with the solder bump attach process required for the flip chip joining, 2) influence of the bonding process on the released structures, 3) measurement and identification of performance variations of MEMS devices due to bumping, 4) direct measurement of the stresses induced by the bumping process, 5) die-to-die spacing (gap) accuracy achieved by varying the solder bump volumes, and 6) the effect of the two different substrates of interest, silicon and Pyrex, on the MEMS devices.

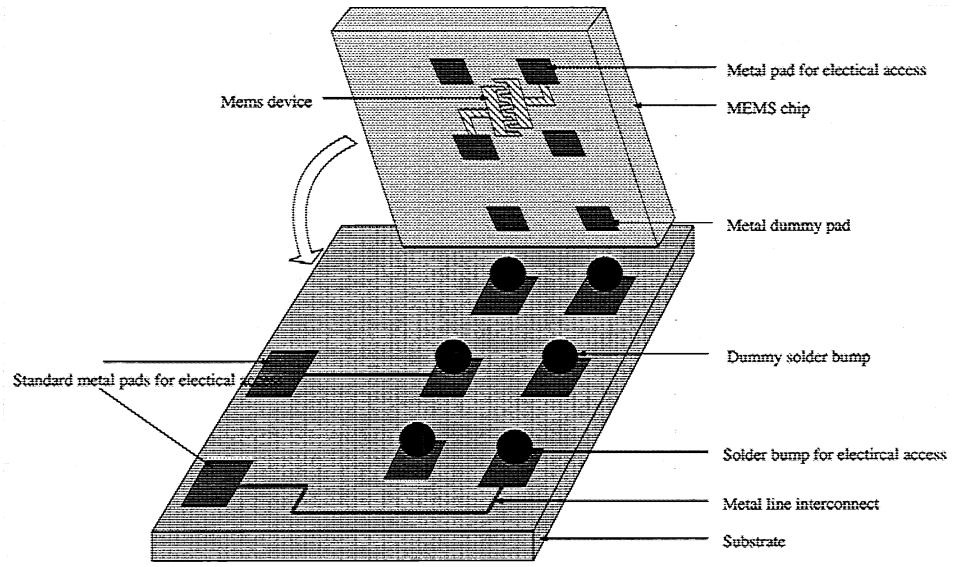


Figure 3: Schematic of flip chipped MEMS and substrate die

Figure 4 shows the cross-sectional schematic of the process flow for substrate fabrication. Two substrates, silicon and Pyrex, are being used. In the case of silicon, an insulation layer of thermal oxide is grown and a metal layer is then evaporated and patterned using lift-off. This forms the electrodes, internal interconnections, and external interconnections from the electrodes to the standard (probe or bond) pad arrays at the boundary of the chip. Next, the substrates are coated with a passivation layer of polyimide, and the polyimide is patterned to open vias to the pads requiring bumps. The under bump metallurgy (UBM) is then evaporated sequentially, in our case a combination of Cr and Cu. Next, a solder dam layer, also consisting of Cr and Cu, is sequentially evaporated and patterned using lift-off. A thick layer of photoresist is applied using multiple coats and patterned to form the template for the through-hole electroplating of the solder. Solder (high lead) is plated, the solder template is removed, and the copper on the solder dam is etched. Finally the solder is reflowed and the UBM is etched. After this step, the substrate is ready for alignment and attachment to the MEMS chip. Table 2 lists the parameters for MCNC's standard wafer bumping process.

Two methods are available for joining the two die after the substrate has been bumped. In the first method, flux is used to help in the joining of the bumps to the solder wettable pads on the MEMS chip. This involves application of flux to the substrate, alignment of the MEMS die to the substrate die and passage of the aligned pair through a heat cycle to reflow the bumps and join them to the opposing pads. A xylene clean is then performed to remove the excess flux. Since surface micromachined devices are released before they are joined, the use of the flux and xylene may cause the suspended structures to stick to the substrate after the joining process. This may cause great difficulty in achieving a process which yields both good die-attach and non-stictioned MEMS devices. The second method uses fluxless soldering, in which case the bumps are fluorine plasma-treated prior to their joining to the solder wettable pads on the MEMS side. The plasma treatment precludes the use of flux, and eliminates the need for the post-join solvent clean. MCNC has patented the technology for the fluxless soldering[5,6], which is used in our work to join the MEMS chips to the substrates.

Table 2: MCNC standard wafer bumping parameters

Solder composition:	High lead or Eutectic
Typical reflow temp:	355°C peak (high lead) 210°C peak (eutectic)
UBM diameter:	125μm (typ.), 50μm (min.)*
Bump pitch:	250 μm (typ.), 100μm (min.)*
Reflowed bump height:	84 μm
Dimensional tolerances:	
UBM diameter:	+/- 1 μm
Reflowed height:	~10%
Ave. tensile strength/bump:	~32 MPa
Ave. shearing force/bump:	~39 gmf

* Smaller bump diameters/pitches are being investigated for MEMS specific activities

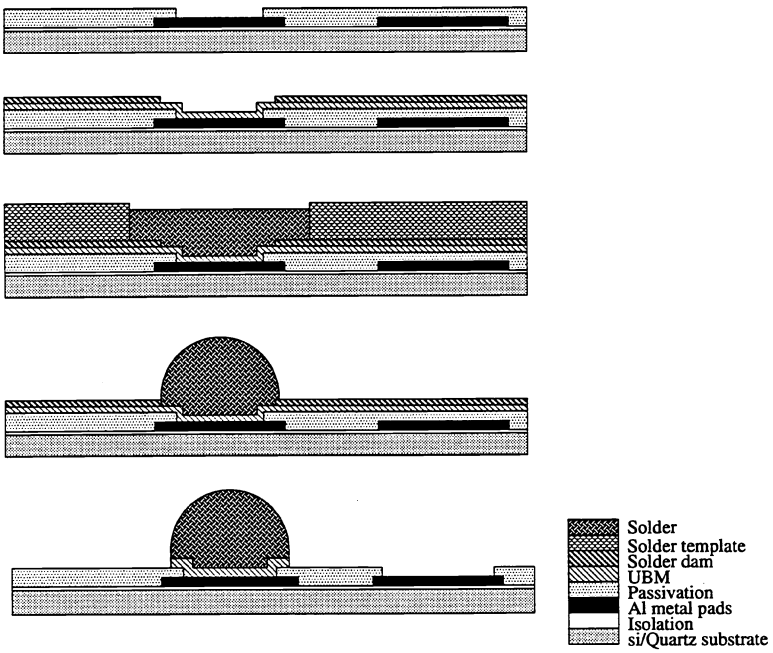


Figure 6: Cross-sectional schematic of substrate fabrication flow

Figure 4: Cross section of substrate fabrication flow

5.2 Characterization Results

Both surface and bulk micromachined devices were successfully joined to the corresponding substrates (including both silicon and quartz). Characterization tests both electrical and mechanical as appropriate were conducted on devices like resonant structures, doubly supported beam arrays, pressure sensors and diaphragms. The performace before and after flip chip joining was compared. Results from testing of some of the devices are described below.

Resonant structures with stress relieving mechanisms, such as folded beam anchors, showed no change in the resonant frequency due to flip chip joining.

Bulk micromachined diaphragms were used for measuring the stress induced due to flip chip joining. The diaphragms used for this measurement consist of single crystal silicon, PSG and polysilicon. Load (pressure) versus deflection measurements are done before and after joining of the MEMS chip to the Pyrex substrate. Pyrex substrate is necessary in this experiment to be able to measure the deflection optically after joining. Figure 5 shows the comparison of the load versus deflection data for the two cases. A custom built setup and a pneumatic chuck were used to apply the desired pressure to the diaphragm, the applied pressure was measured using a commercial pressure sensor. The deflections were measured optically and hence the accuracy of the measurements is within a micron. The equation below describes the relationship between the center deflection of a square diaphragm and the applied pressure.

$$P = 4.5E(\frac{t}{a})^4(\frac{w}{t}) + 3\sigma(\frac{t}{a})^2(\frac{w}{t}) + 1.8E(\frac{t}{a})^4(\frac{w}{t})^3$$

Where P is the load applied in Pascals, W is the maximum deflection (at the center of the diaphragm), t is the thickness of the diaphragm, 2a is the length of the side of the diaphragm, E is Young's modulus and σ is the residual stress. For the diaphragm used here the diaphragm thickness, t, is 22 microns and the size of the diaphragm, 2a, is 2590 microns.

In the above equation the Young's modulus and the residual stress values are treated as unknown parameters and are extracted by fitting the equation to the experimental load-deflection data. The values of Young's modulus and residual stress before flip-chip joining are 202.45 GPa and 20.66 MPa respectively. The value of Young's modulus obtained from the model fit before joining is used as a known parameter for model fitting for the after joining case and a residual stress value of 15.14 MPa is obtained. The results indicate that the residual stress decreases after joining indicating that the joining is introducing some compressive stress.

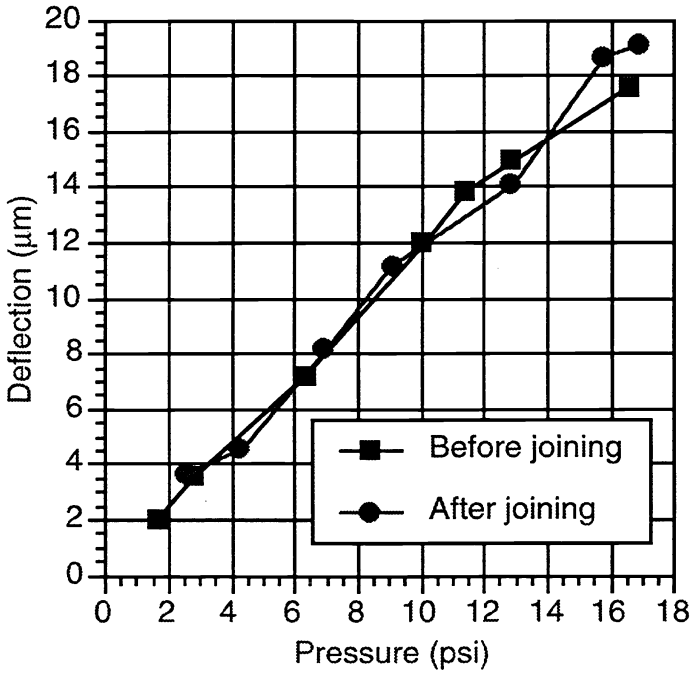


Figure 5: Deflection variation as a function of applied pressure for before and after flip-chip joining

The piezoresistive sensors fabricated using combined surface and bulk micromachining were tested to compare their performance before and after flip chip joining. A single crystal diaphragm was fabricated by bulk etching from the back side, the piezoresistors were fabricated from doped polysilicon. The resistors were electrically isolated from the single crystal silicon using the PSG, resulting in the diaphragm being a composite of silicon and PSG. Load versus peizoresistance measurements were taken before flip-chip joining for the two resistors, R1 nad R2, placed at opposing edges of the diaphragm. The pressure sensors were then flip chip joined to the corresponding Pyrex substrates. To make electrical measurements the joined chips were placed in a ceramic package and wire bonded. Then the packaged chip was used to measure the variation of the piezoresistance

as a function of the applied pressure. Figures 6 and 7 show the resistance variation of R1 and R2 before and after joining. For resistor R1 the joining resulted in increased tensile stress and therefore, an increased resistance value. For resistor R2, the joining introduced a compressive stress which decreased the resistance value after joining. These results, consistant over several tested die, indicate that the joining induced stress varies depending on the location of the structure on the chip. By proper placement of the devices the effect of the joining induced stress can be minimized or used to advantage.

This characterization run has successfully demonstrated the feasibility of flip chip integration for MEMS. The results indicate, at times, a minor influence of the flip chip joining on device performance. Design rules for the design and handling of flip chip MEMS are currently under development and will be publicly available to help facilitate the use of flip chip integration for Smart MEMS systems.

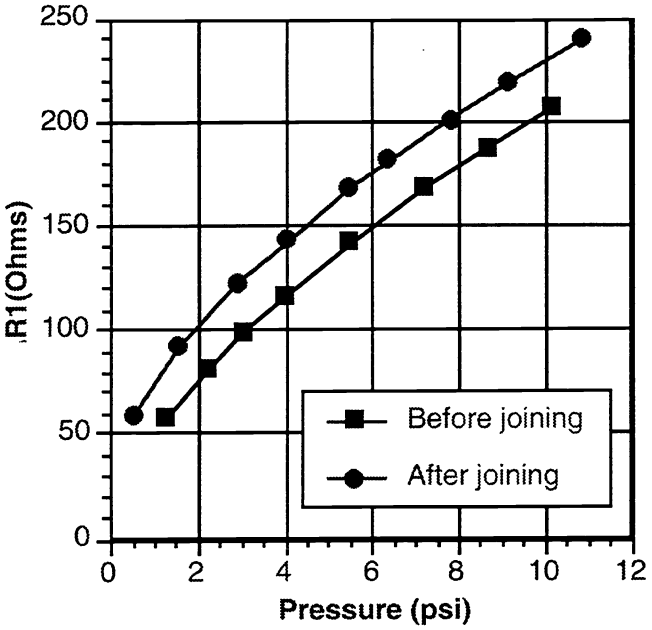


Figure 6: Piezoresistance variation for the resistor R1 before and after joining

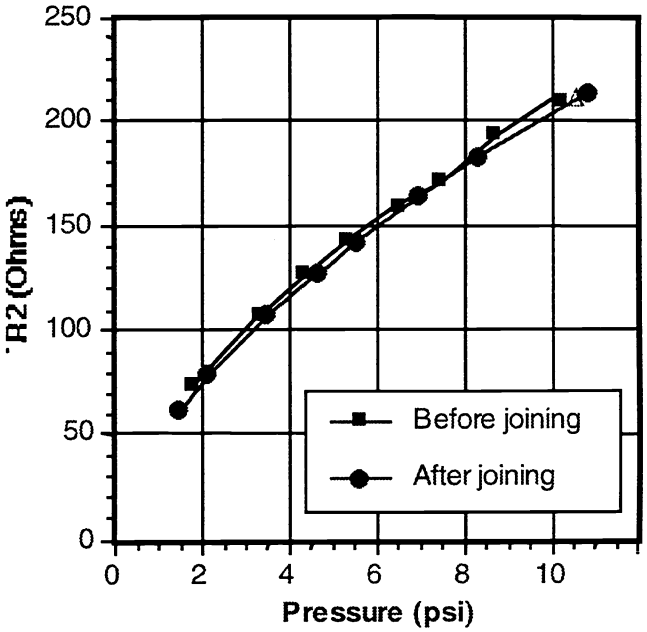


Figure 7: Piezoresistance variation for the resistor R2 before and after joining

6. ELECTROMECHANICAL CONTROL SYSTEM

The Electromechanical Control System (ECOSYS) is a program to facilitate the fabrication of MEMS systems including the electronics. A standardized IC controller with various functional blocks is currently in the design phase. The aim is to allow users to connect blocks and attach them to a MEMS device via flip-chip attachment to a MEMS die to implement a system incorporating sensing, feedback, and control. A limited degree of user programmability will be provided via external RC components to tailor the response of the blocks for the application. Interconnections to the MEMS elements will be via solder bumps and the parasitics introduced by the solder bump and pad will be accounted for in the design of the blocks.

Functional blocks currently being designed include preamplifier, capacitance measurement circuit, current/voltage references, PID control block, and buffer amplifiers. We plan to add additional functions like A/D and D/A converters and resistance measurement circuits at a later date. A simple digital circuit block is also under consideration.

7. CONCLUSIONS

Both the MUMPs and the Smart MEMS processes described have been developed and implemented at MCNC in cooperation with ARPA, as part of an ongoing program of MEMS Infrastructure development. It is hoped that by lowering the barriers to accessing MEMS technology, both cost and availability, the domestic user community will be able to implement their ideas and take advantage of the revolution in technology that MEMS can afford. Further information on the MUMPs program and the Smart MEMS activities can be obtained by contacting the authors at (919) 248-1800 or mems@mcnc.org.

8. ACKNOWLEDGMENTS

The authors would like to thank the fabrication facility staff at MCNC for their hard work and dedication in helping make the MUMPs program a success. We would also like to thank the members of the Advanced Packaging and Interconnection Group for their support and technical advice in implementing the Smart MEMS. We would also like to thank Dr. Kaigham Gabriel, ARPA MEMS Program Manager for his faith and advocacy in making MEMS infrastructure a reality. This work is supported under ARPA contract DABT63-93-C-0051.

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