Backend Wafer Processing Technology

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OUTLINE

Introduction
Vacuum & Pumping Systems
Physical Vapor Deposition
Chemical Vapor Deposition
Chemical Mechanical Polishing
Multilayer Metal Processes

INTRODUCTION

Front End - Well Formation
Isolation Technology
Transistor Formation

Back End - Local Interconnect and Contacts
Multilayer Metal and Passivation

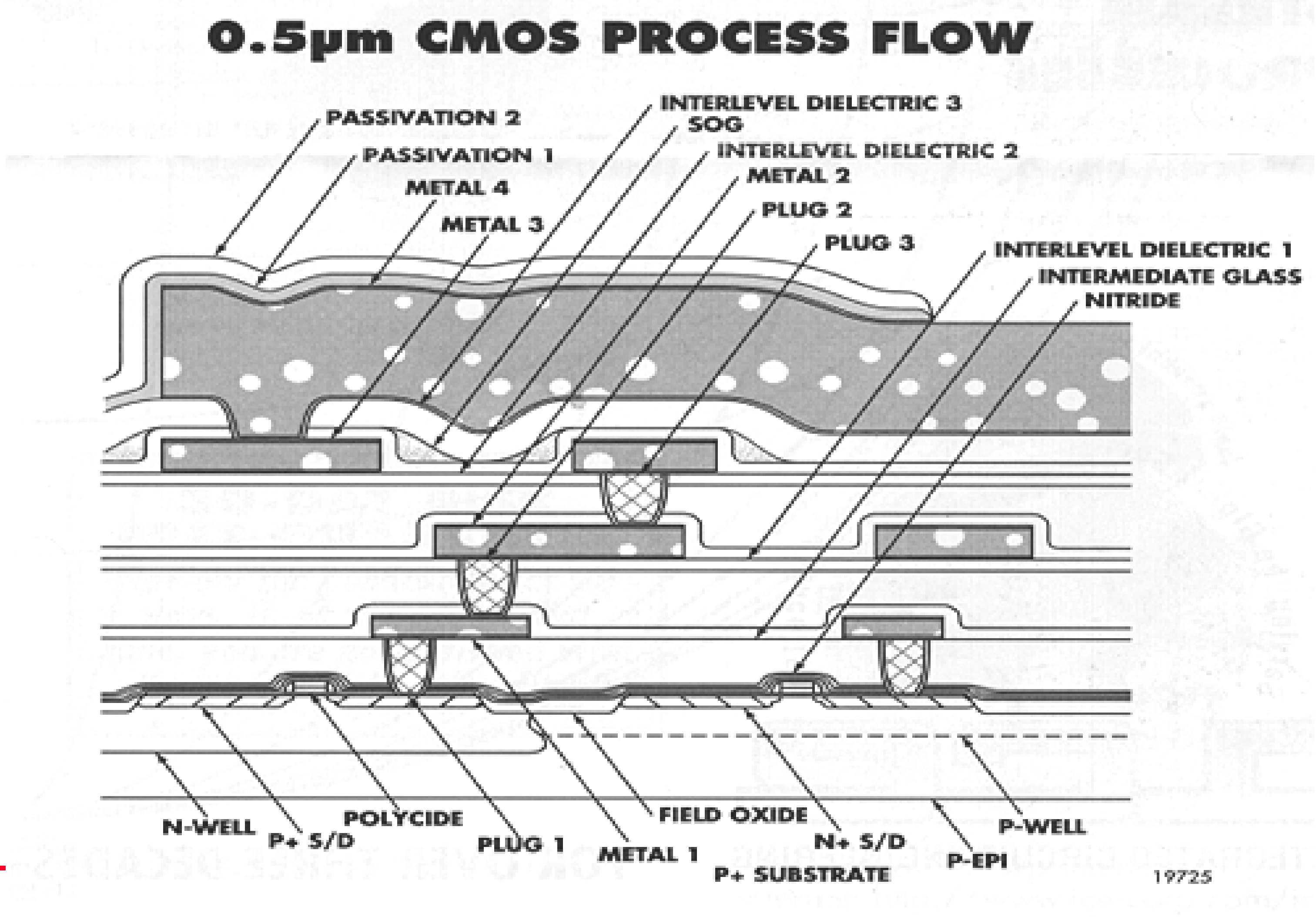
Back End Processes - Physical Vapor Deposition (PVD, Sputtering,etc.)
Chemical Vapor Deposition (CVD, LPCVD, etc.)
Chemical Mechanical Polishing
Lithography and Plasma Etching (for these films)

INDUSTRY ROADMAP

	1995	**1998**	**2001**	**2004**	**2007**	**2010**
Polysilicon CD µm	0.35	0.25	0.18	0.13	0.10	0.07
Contact/Via CD µm	0.04	0.28	.020	0.14	0.11	0.08
Min Interconnect CD µm	0.40	0.30	0.22	0.15	0.11	0.08
Metal height/width aspect ratio	1.5:1	2:1	2.5:1	3:1	3.5:1	4:1
Number of metal levels						
DRAM	2	2-3	3	3	3	3
Microprocessor	4-5	5	5-6	6	6-7	7-8
Interconnection Length m	380	840	2100	4100	6300	10,000
Reliability FITs/meter	0.016	0.0047	0.0011	0.0005	0.0004	0.0002
Cost \$/cm^2/level	0.29	0.23	0.23	0.18	0.18	0.14

1 mile = 1625 meters

CROSSECTION SHOWING INTERCONNECT



NEED FOR VACUUM PROCESSING

Atoms, Ions, Molecules, Electrons need a long Mean Free Path:

$$\text{MFP} = KT / (2 \pi \sigma^2 P)^{0.5}$$

where K is Boltzman's constant
T is Temperature
σ is collision crossection
P is pressure

as pressure goes down, MFP goes up. At 10-5 Torr MFP is > 300 cm

Vacuum also gives **control of the chemicals in the process**. For example if we do not want oxygen in the process we must remove all the room air from the process. One way is to pump out all the air and refill with the desired gas (such as Argon) and then do the process (Sputter)

VACUUM LEVELS

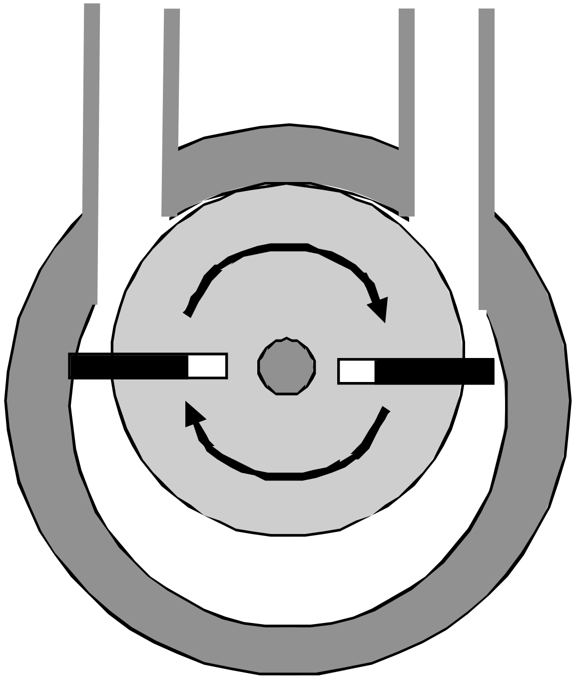
Atmospheric Pressure ~ 14.7 lbs/sq inch = 760 mm Hg
1 Torr is approximately 1 mm of Hg = 1/760 Atmosphere

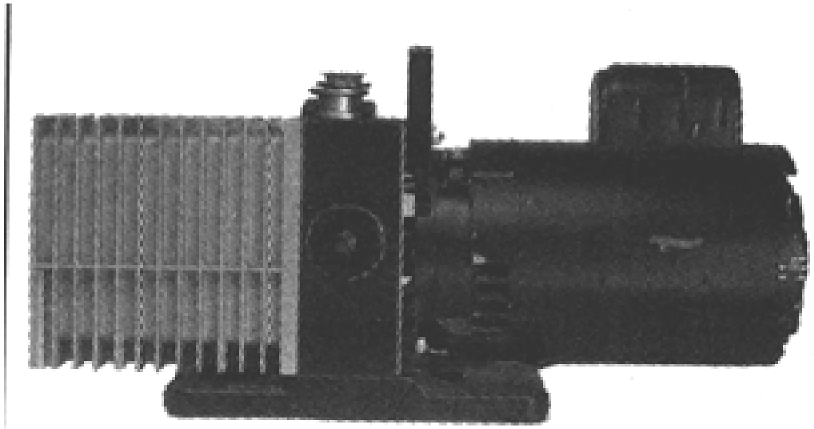
Low vacuum	700 to 25 Torr	Hold spinning wafers
Medium vacuum	25 to 10-3 Torr	LPCVD, Plasma Etch
High vacuum	10-3 to 10-6 Torr	Sputter
Very high vacuum	10-6 to 10-9 Torr	Evaporation Ion Implant Base pressure prior to Sputter, Etch SEM
Ultrahigh vacuum	below 10-9 Torr	MBE

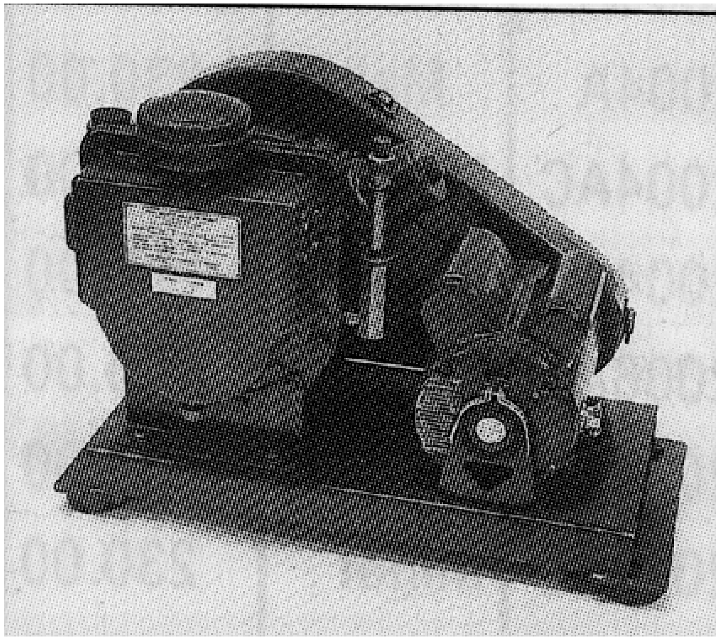
VACUM PUMPS

	Range Torr	Speed liters/s	Cost $
Pumps That Exhaust to Outside			
Rotary Mechanical Pumps	ATM to10-3	high	low
Roots Blower	10-1 to 10-4	high	medium
Turbomolecular	10-2 to 10-6	high	high
Oil Diffusion Pump	10-2 to 10-6	high	low
Pumps That Trap Gas Inside			
Ion Pump	10-4 to 10-9	low	high
Sublimation	10-2 to 10-4	low	low
Cryogenic	10-2 to 10-7	medium	high

VANE TYPE ROTARY OIL PUMP





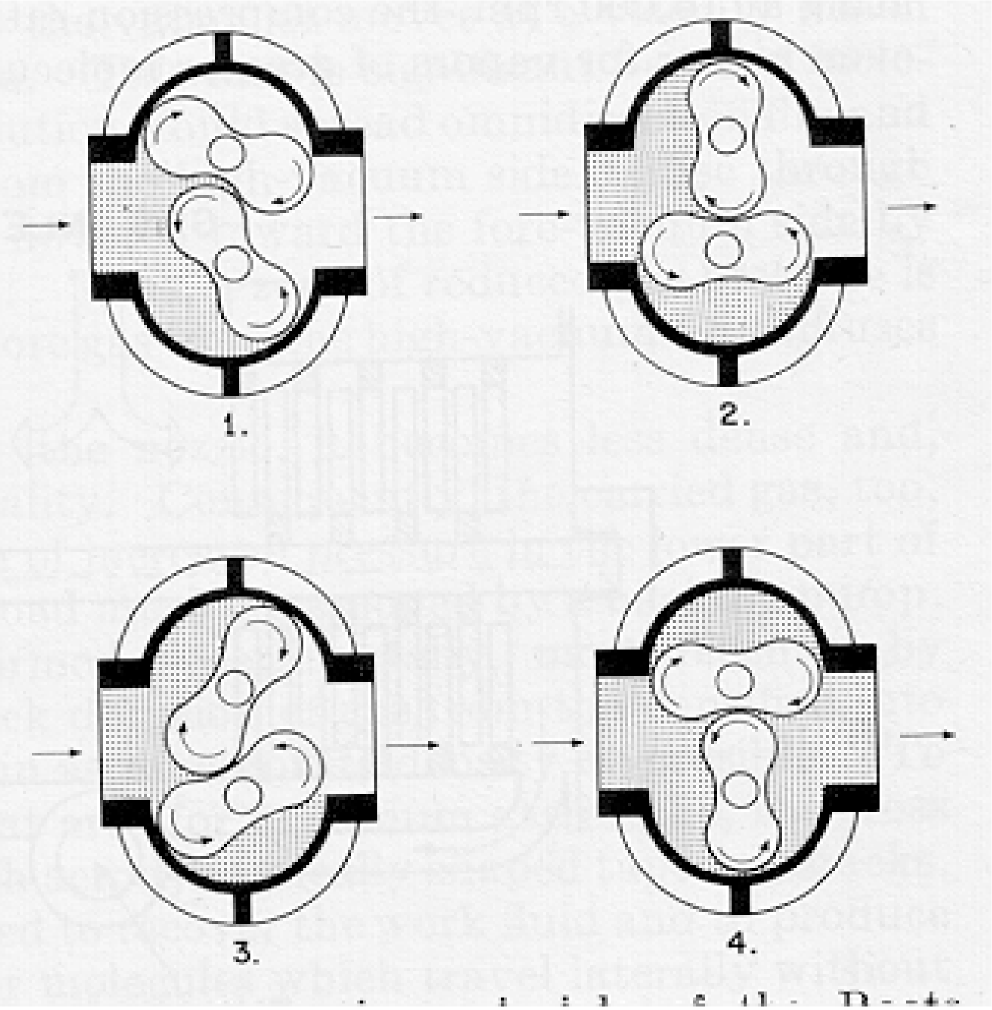


Atmosphere to medium vacuum levels
High Volume

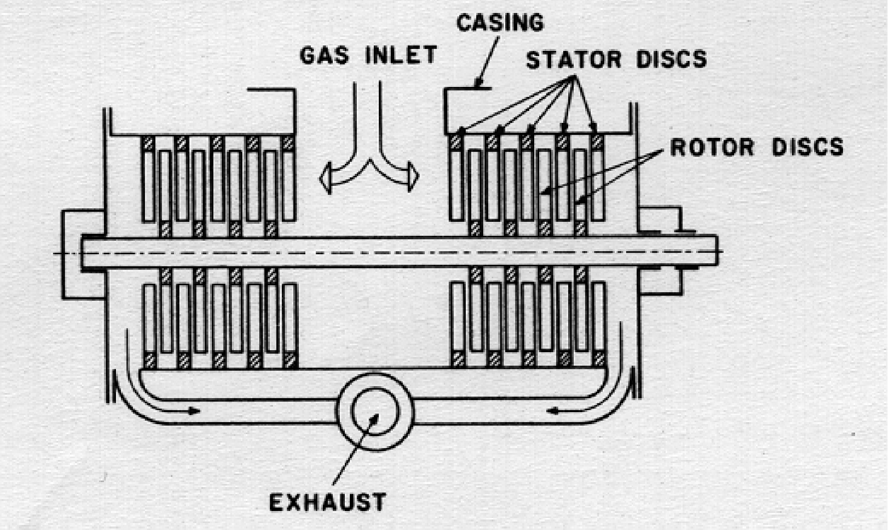
ROOTS PUMP

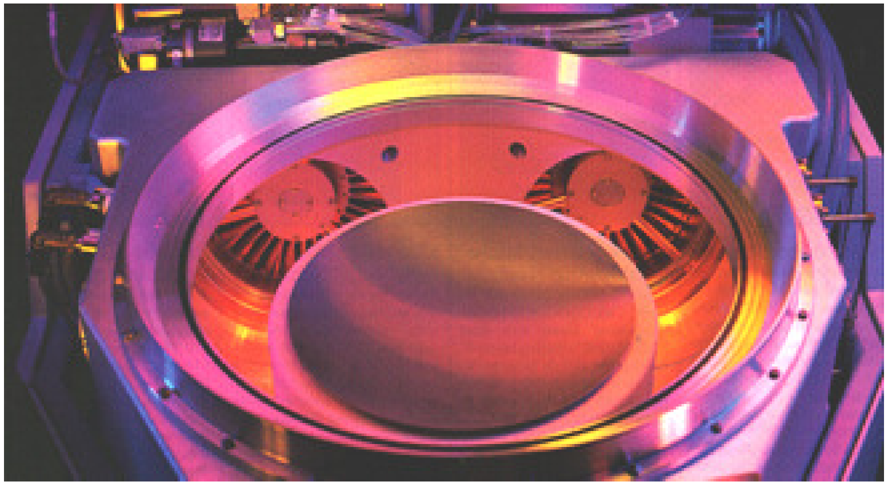
High Volume

10-1 to 10-4 Torr



TURBOMOLECULAR PUMPS

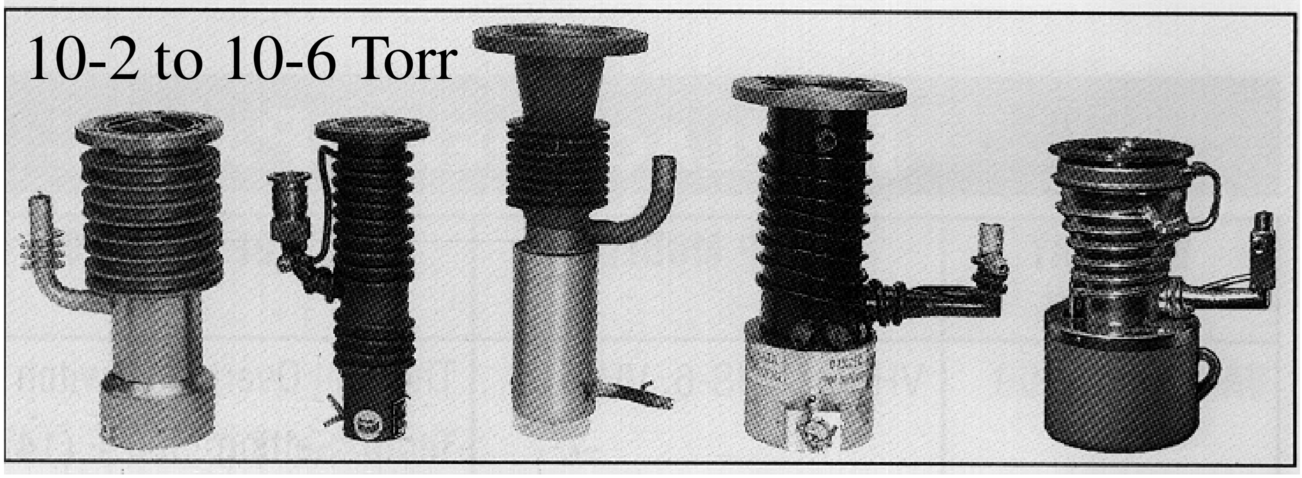




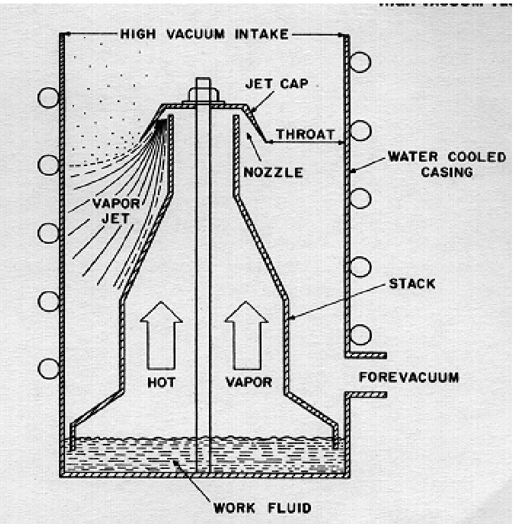
High Volume
10-2 to 10-6 Torr

Magnetically levitated turbomolecular pumps on HDPCVD system

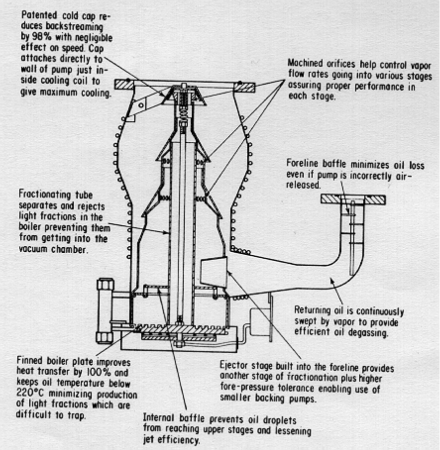
OIL DIFFUSION PUMP



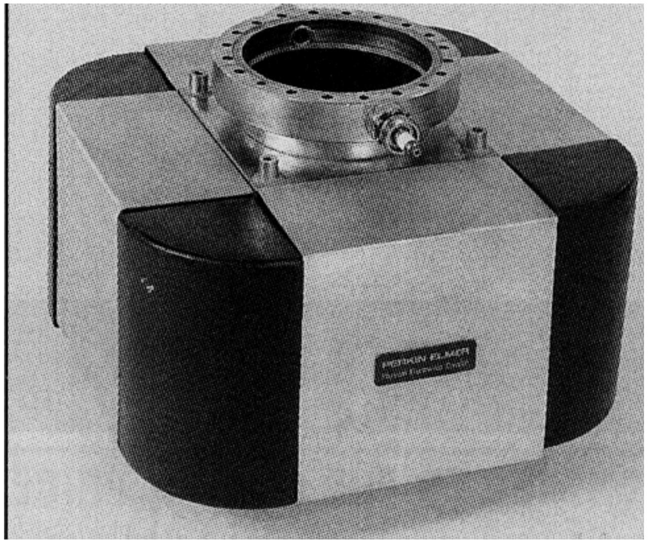
10-2 to 10-6 Torr

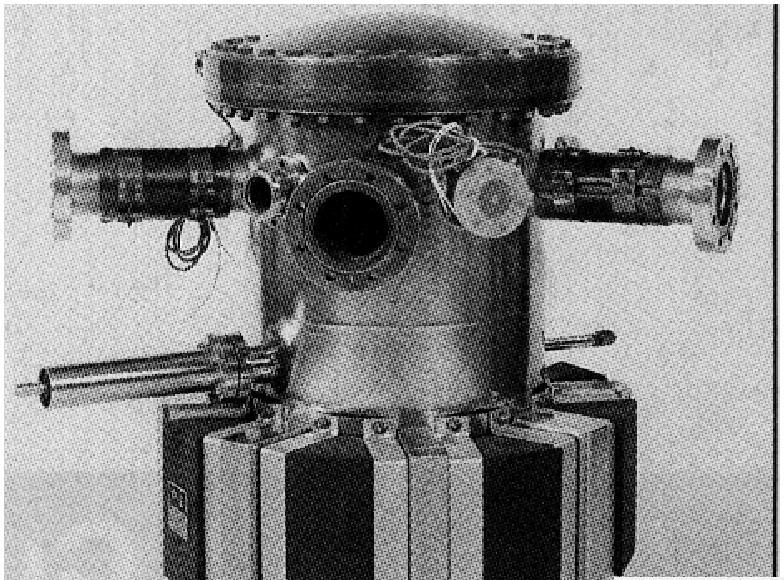


A low boiling point, high molecular weight hydrocarbon pump fluid is heated in the bottom of the pump. The higher pressure inside the boiler and jet assembly forces the vapor molecules through downward directed nozzles at very high speeds. This downward motion of the vapor molecules is also imparted to gas molecules, which collide with the heavier vapor molecules. The gas molecules create a region of increased pressure in the lower part of the pump which are removed by a roughing pump. Baffles and liquid nitrogen cold traps are used to help prevent oil molecules from reaching the chamber.

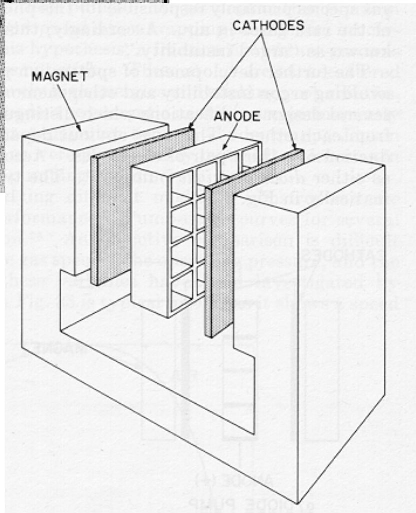


ION PUMP

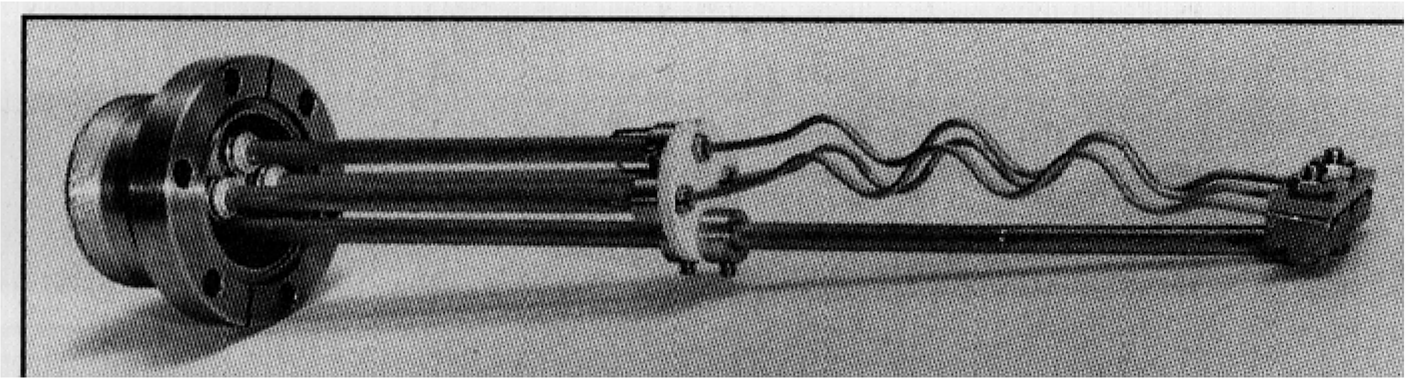




High electric field and magnetic field. Ionizes gas molecules and accelerates ions into the cathode where they remain.



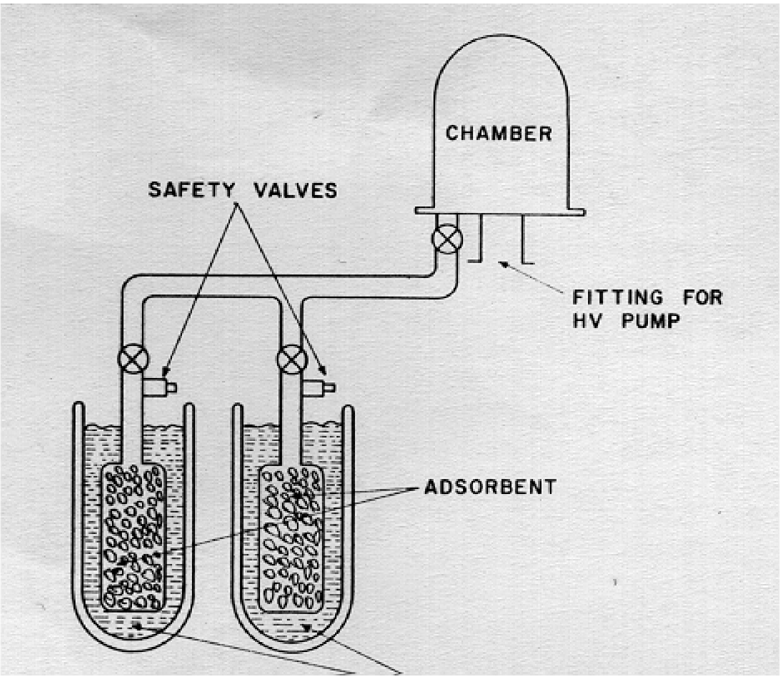
SUBLIMATION PUMP



Titanium wire when heated sublimes and covers up molecules adhered to the chamber walls. This creates a new surface which adsorbes more molecules.

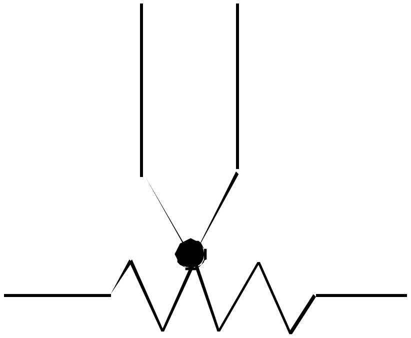
CRYO PUMP

Cryo pumps use extremely cold surfaces to trap molecules and thus pump the system. Self contained refrigeration units and liquid nitrogen cooled pumps are available. Regeneration involves heating the system to drive off trapped gases, pumping the system down to medium vacuum levels and then cooling to -200 °C

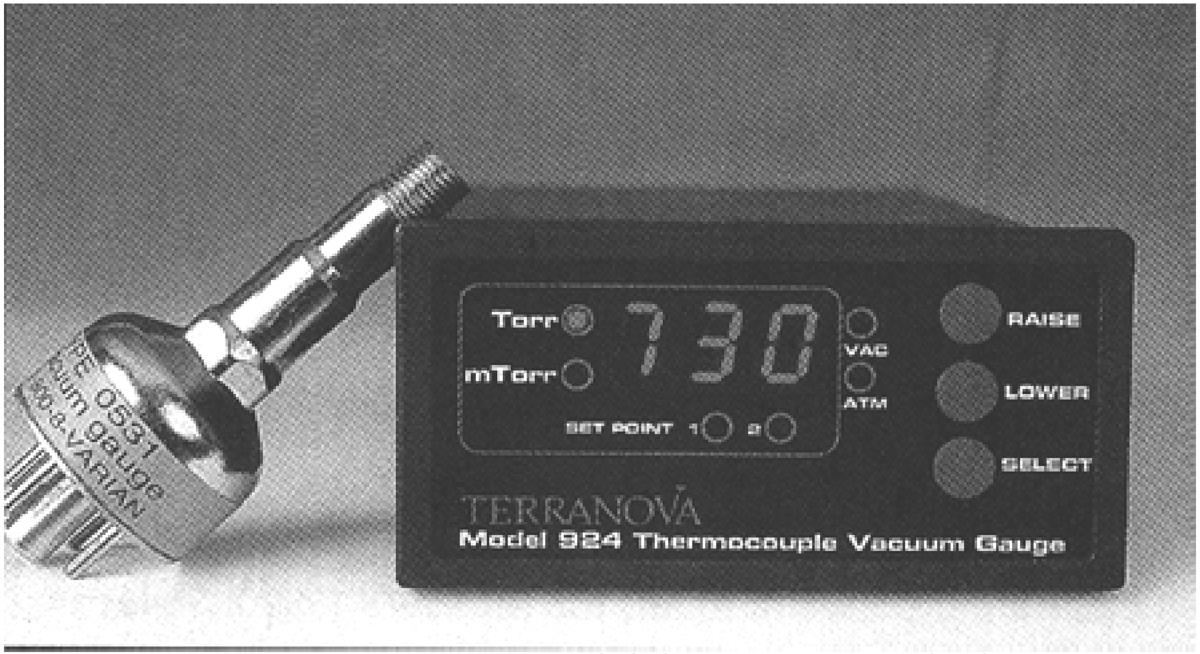


THERMOCOUPLE GAGE

Thermocouple



Constant Power
Input to Heater

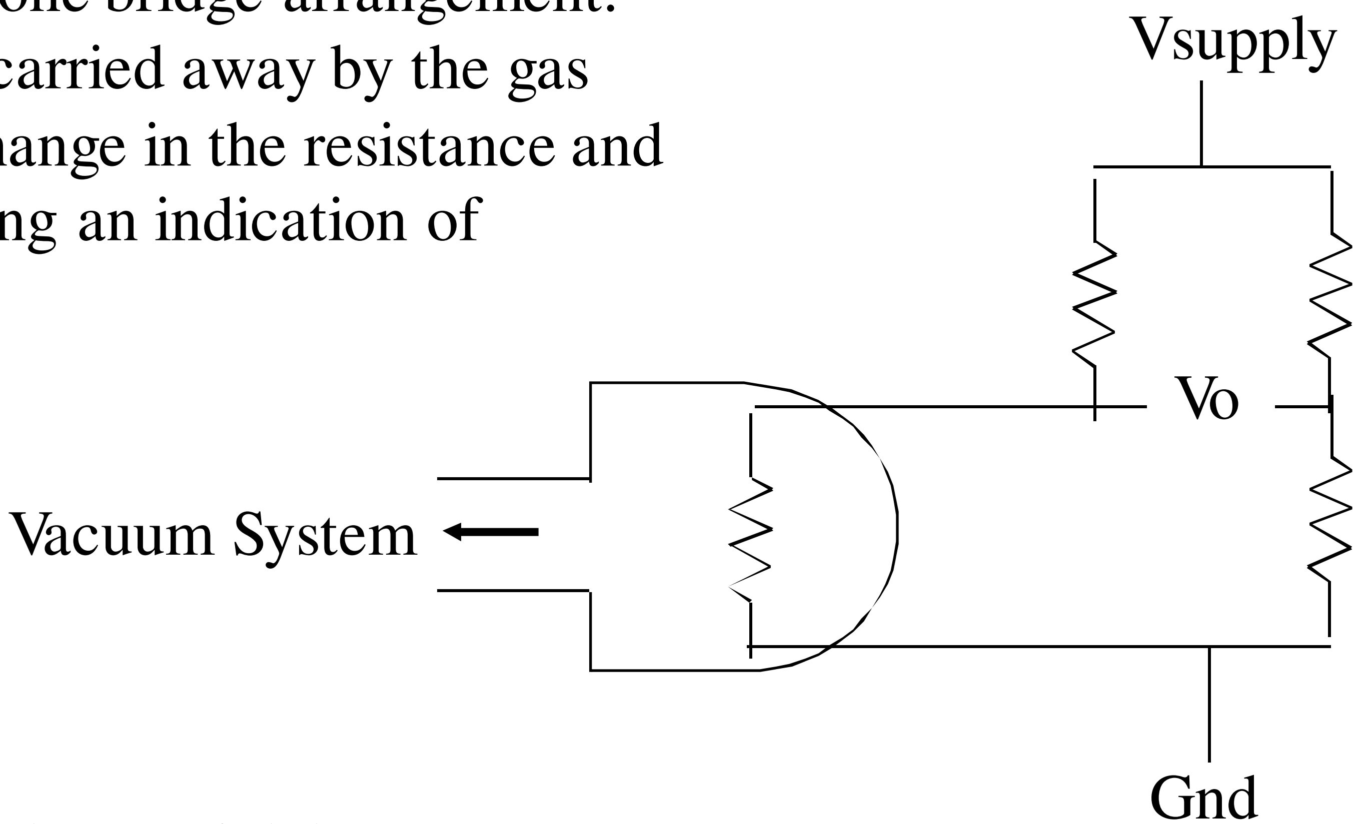


1000 Torr to 10-3 Torr

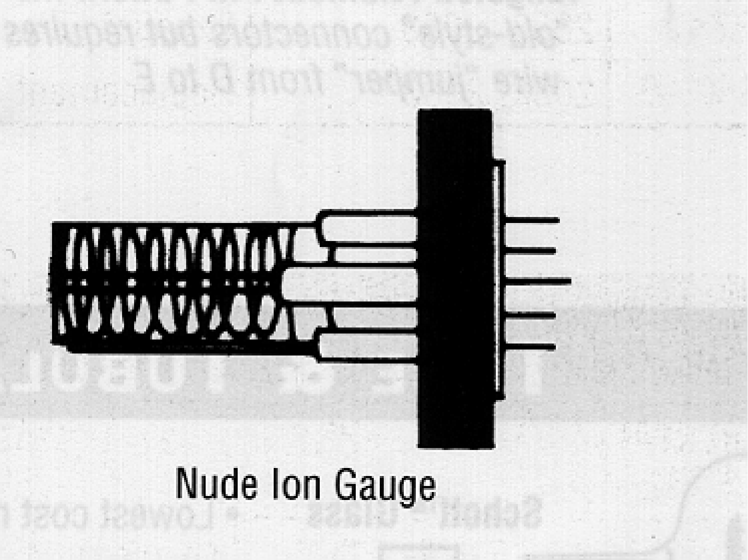
Thermocouple Readout - Temperature of the Heater is Inversely Proportional to Pressure

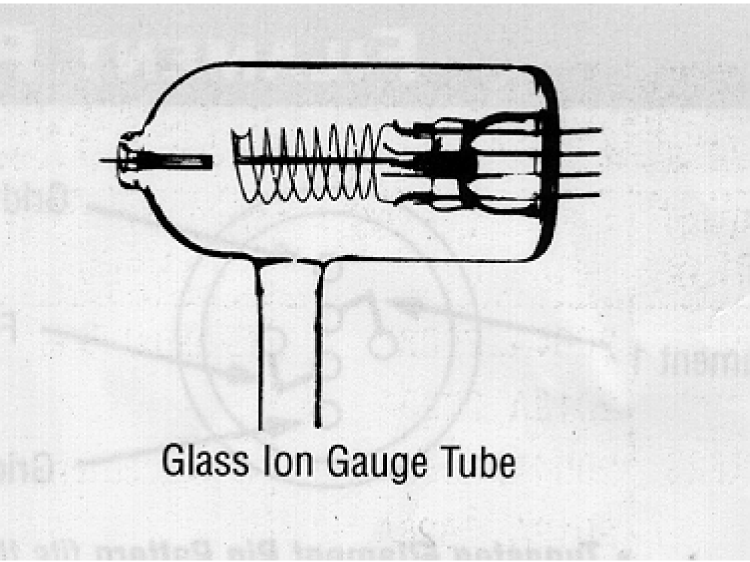
PIRANI GAGE

The pirani gage uses a resistance wire in a wheatstone bridge arrangement. The heat is carried away by the gas causing a change in the resistance and thus providing an indication of pressure.



IONIZATION GAGE

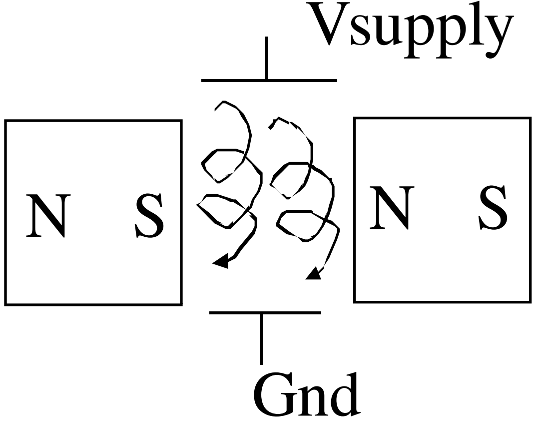

Nude Ion Gauge


Glass Ion Gauge Tube

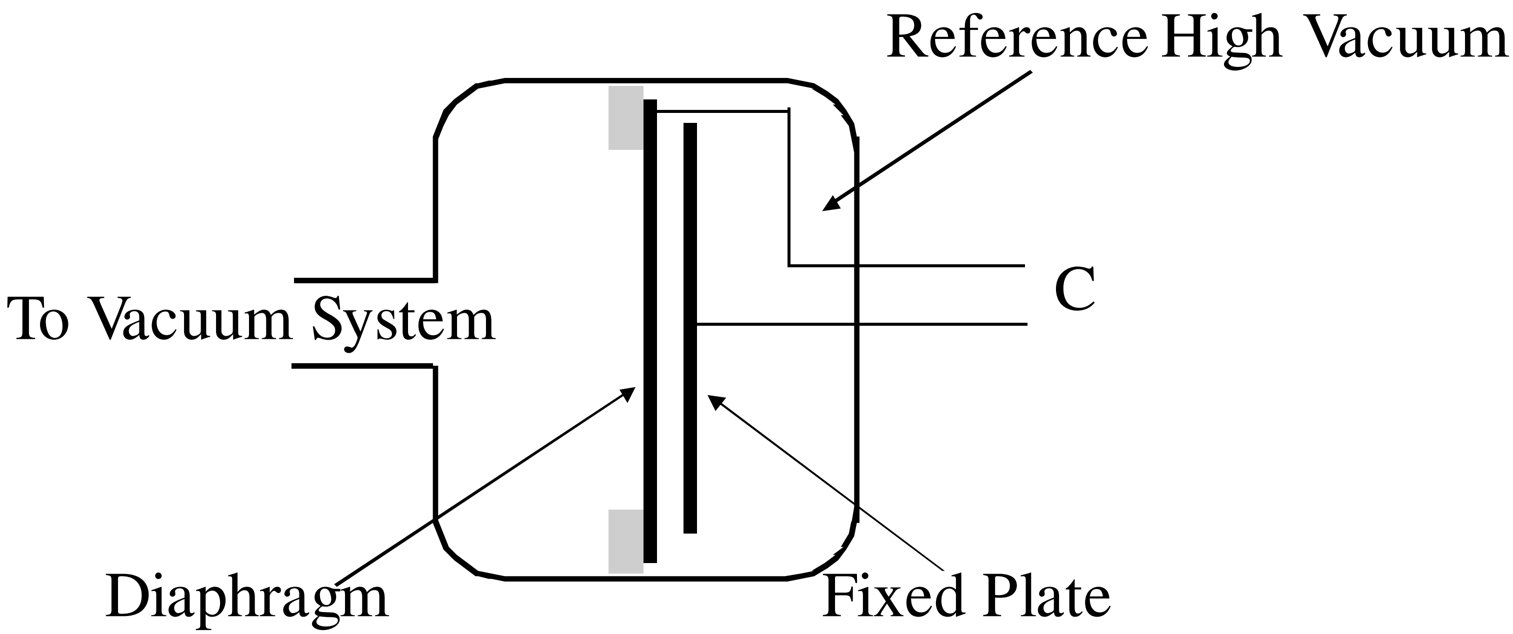
High Voltage and a hot filament ionizes gas molecules. The current is proportional to the pressure.

PENNING GAUGE

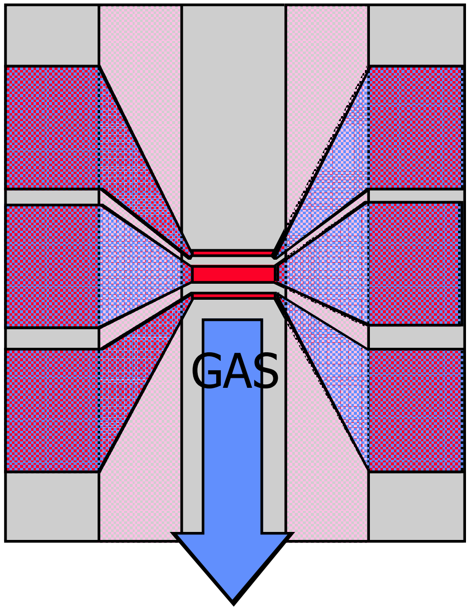
Essentially a cold cathode ionization gauge. This gage uses about 2000 volts between the anode and cathode which are placed between two permanent magnets. The magnetic field causes ions and electrons to travel in long spiral paths enroute to the cathode and anode respectively thus increasing the probability of causing an ionizing collision which in turn sustains the process. The current measured is proportional to the pressure.



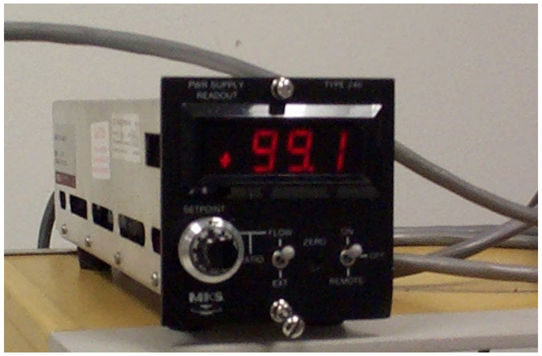
CAPACITANCE MANOMETER GAUGE

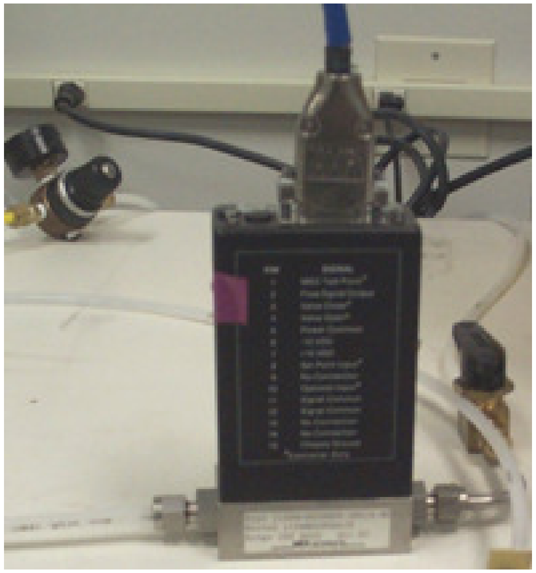


MASS FLOW CONTROLLER



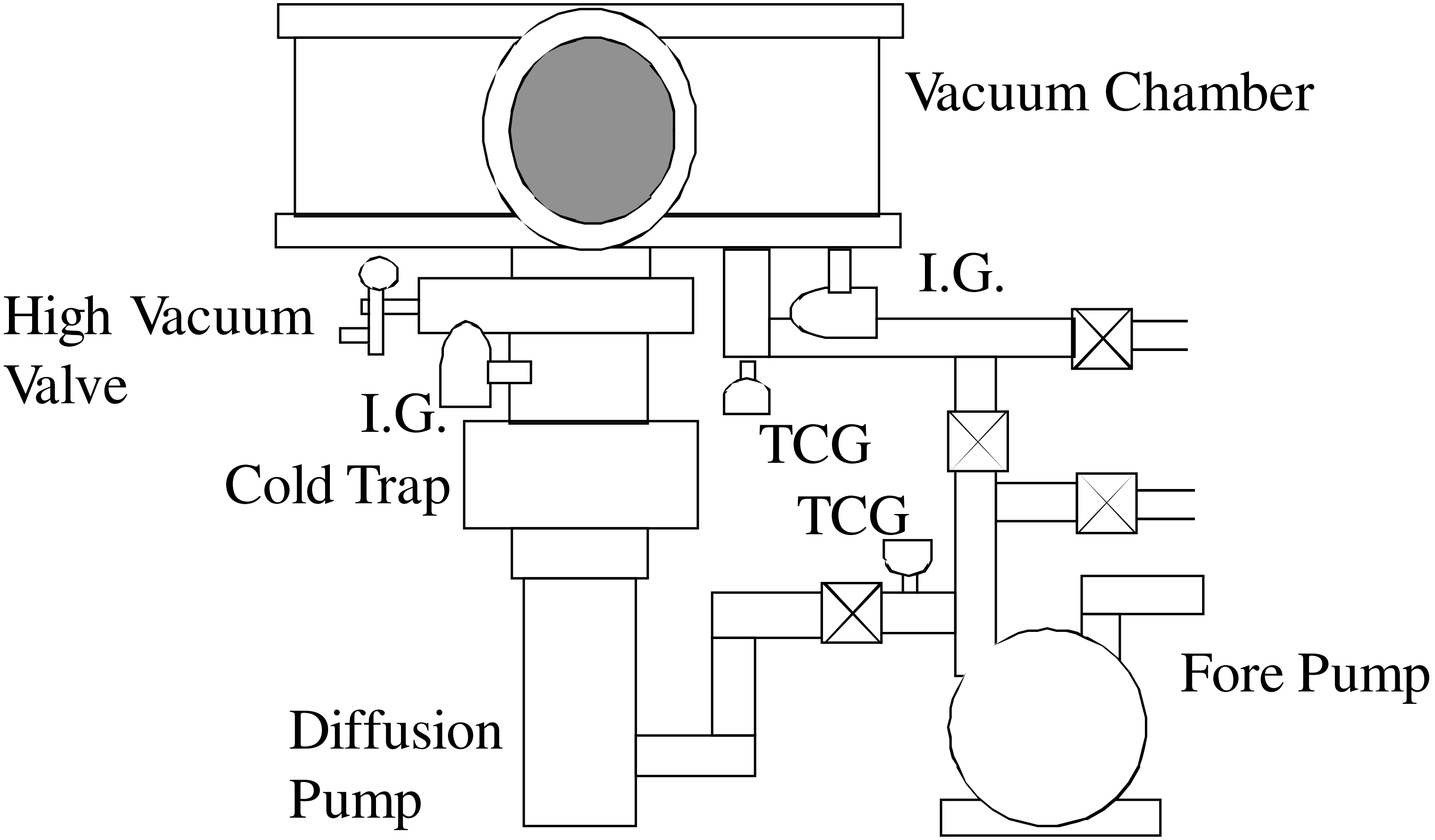
Gas Flow in Water Movie





Constant heat (input power in watts) heater and two temperature measurement resistors, one upstream, one downstream. At zero flow both sensors will be at the same temperature. Flow will cause the upstream sensor to be at a lower temperature than the down stream sensor.

DIFFUSION PUMP VACUUM SYSTEM



VACUUM SYSTEM FOR MEDIUM VACUUM LEVELS

Rotary Vane Mechanical Pump
Roots Blower or Turbomolecular Pump

VACUUM SYSTEM FOR HIGH VACUUM LEVELS

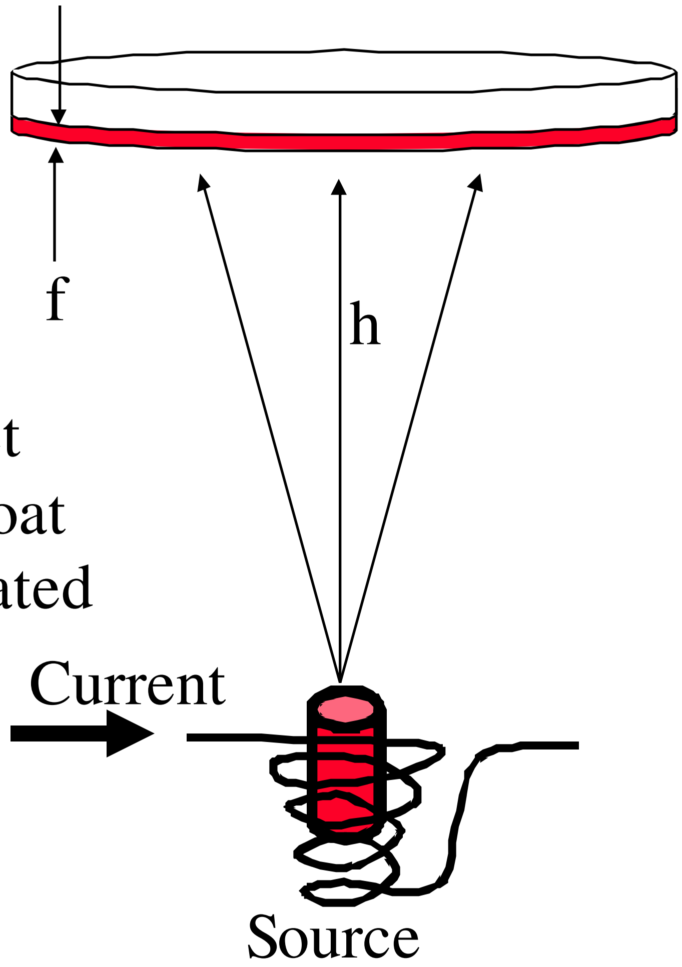
Rotary Vane Mehanical Pump
Cryo Pump
Ion Pump

PHYSICAL VAPOR DEPOSITION

- Thermal Evaporation
  - Resistance Heating
  - Electron Gun Heating

- Sputtering
  - DC
  - RF
  - RF Magnetron

EVAPORATION



Sources :

Resistance Heated

- Wire Basket
- Dimpled Boat

Electron Beam Heated

$$f = \frac{m}{4d\,\pi\,h^2}$$

f = film thickness

d = density

h = height

m = mass

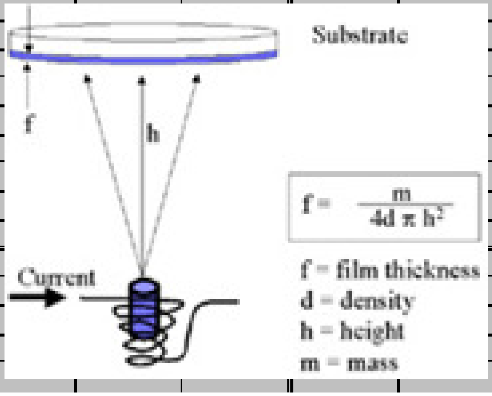
EVAPORATION CALCULATION

Rochester Institute of Technology — March 19, 2006
Microelectronic Engineering — Dr. Lynn Fuller

Evaporation in this model assumes that the mass evaporated is spread out over the inside surface of a sphere with radius equal to the distance from the evaporation source to the substrate. The surface area is 4 pi h^2 when multiplied by film thickness gives volume of material needed which is multiplied by the density to give the mass needed. Divide the mass by 2 if a dimpled boat is used allowing coating over a hemisphere instead of a sphere.

m = the mass that needs to be evaporated = 4 pi h^2 f d	m =	3.88	gm
f = the desired film thickness	f =	0.1	µm
d = the density of the material being evaporated	d =	19.3	
h = the height between the filament and the substrate	h =	40	cm
mass in troy oz is found = 0.3215 x mass (g)	m =	0.12	Troy Oz

Denisty of some materials		Select only one =1, others = 0
Aluminum	2.7	0
Gold	19.3	1
Copper	8.96	0
Tin	7.3	0
Lead	11.4	0



Dimpled Boat

EVAPORATION DATA

Material	Formula	Melt pt.	Temp °C @ Vapor Pressure		
		°C	1E-8	1E-6	1E-4
Aluminum	Al	660	677	812	1010
Alumina	Al_2O_3	2045	1045	1210	1325
Antimony	Sb	630	279	345	425
Arsenic	As	814	107	152	210
Beryllium	Be	1278	710	878	1000
Boron	B	2100	1278	1548	1797
Cadmium	Cd	321	64	120	180
Cadmium Sulfide	CdS	1750			550
Chromium	Cr	1890	837	977	1177
Cobalt	Co	1495	850	990	1200
Gallium	Ga	30	619	742	907
Germanium	Ge	937	812	957	1167

MRC Co., "Evaporation and Sputtering Data Book," Orangeburg, NY
http://www.epimbe.com/pages/vp

EVAPORATION DATA

Material	Formula	Melt pt. °C	Temp °C @ Vapor Pressure 1E-8	1E-6	1E-4
Gold	Au	1062	807	947	1132
Hafnium Oxide	HfO2	2812			2500
Nickel	Ni	1453	927	987	1262
Palladium	Pd	1550	842	992	1192
Platinum	Pt	1769	1292	1492	1747
Selenium	Se	217	89	125	170
Silicon	Si	1410	992	1147	1337
Silicon Dioxide	SiO2	1800			1025
Silicon Nitride	Si3N4				800
Silver	Ag	961	574	617	684
Tantalum	Ta	2966	1960	2240	2590
Titanium	Ti	1668	1067	1235	1453
Tungsten	W	3410	2117	2407	2757
Zirconium	Zr	1852	1477	1702	1987

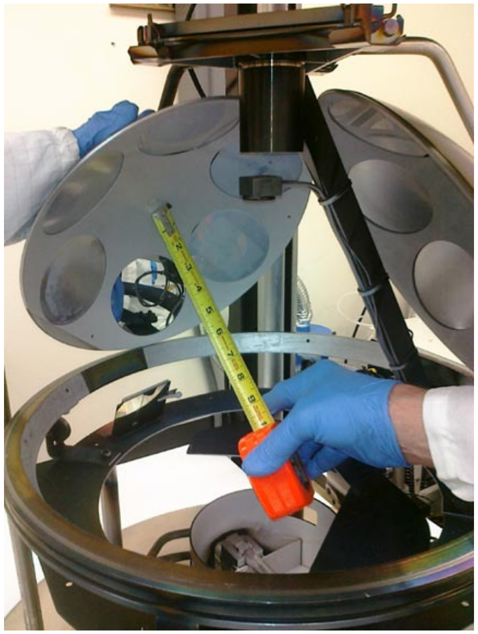
MRC Co., “Evaporation and Sputtering Data Book,” Orangeburg, NY
http://www.epimbe.com/pages/vp

EVAPORATION TOOLS

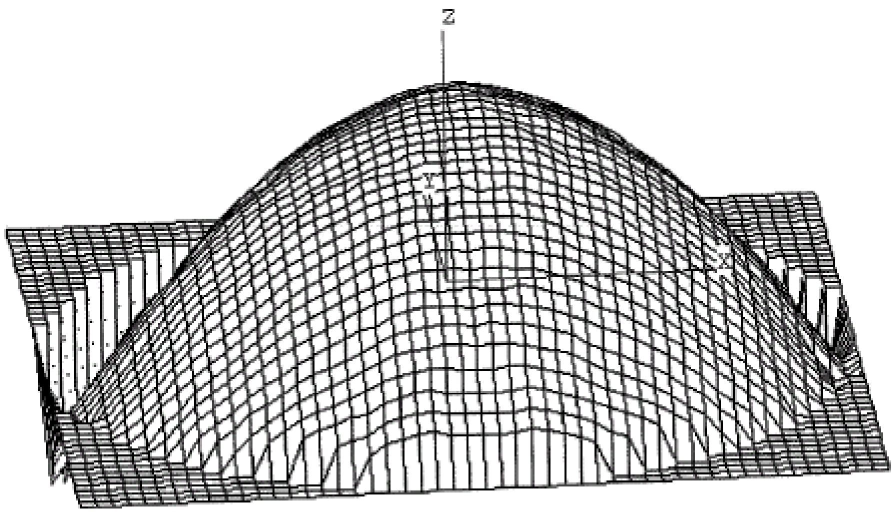
CHA Electron Beam Evaporator

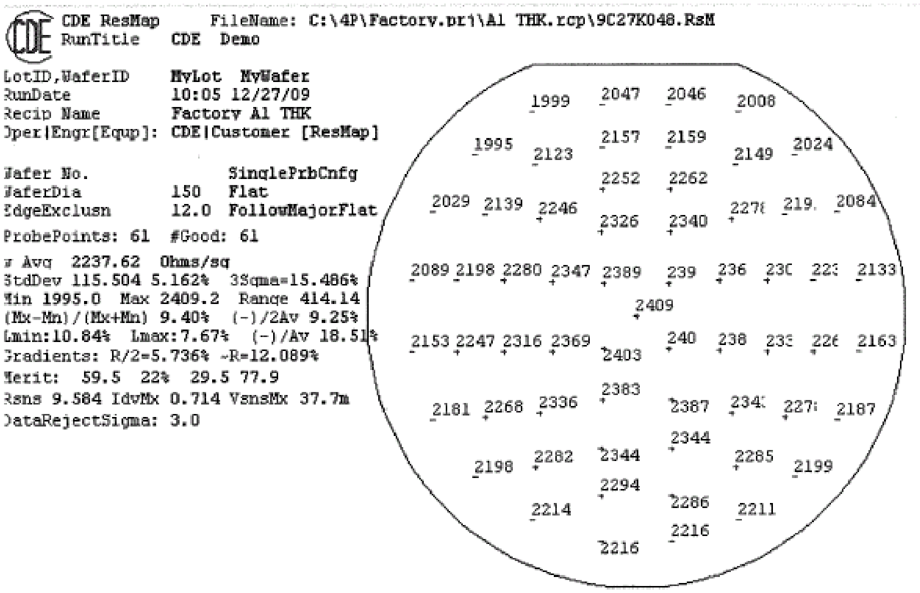
CVC Thermal Evaporator

CHA FLASH EVAPORATOR



FLASH EVAPORATOR THICKNESS UNIFORMITY





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RunTitle    CDE  Demo

LotID,WaferID      MyLot  MyWafer
RunDate            10:05 12/27/09
Recip Name         Factory Al THK
Oper|Engr[Equp]:   CDE|Customer [ResMap]

Wafer No.               SinglePrbCnfg
WaferDia           150  Flat
EdgeExclusn        12.0 FollowMajorFlat
ProbePoints: 61  #Good: 61
  Avg  2237.62  Ohms/sq
StdDev 115.504 5.162%  3Sgma=15.486%
Min 1995.0  Max 2409.2  Range 414.14
(Mx-Mn)/(Mx+Mn) 9.40%  (-)/2Av 9.25%
Lmin:10.84%  Lmax:7.67%  (-)/Av 18.51%
Gradients: R/2=5.736% ~R=12.089%
Merit:  59.5  22%  29.5 77.9
Rsns 9.584 IdvMx 0.714 VsnsMx 37.7m
DataRejectSigma: 3.0
```

```
LDE RunTitle   CDE  Demo

otID,WaferID      MyLot  MyWa
unDate            10:05 12/27/09
ecip Name         Factory Al THK
per|Engr[Equp]:   CDE|Customer [ResMap]

afer No.               SinglePrbCnfg
aferDia           150  Flat
dgeExclusn        12.0 FollowMajorFlat
robePoints: 61  #Good: 61
 Avg  2237.62  Ohms/sq
tdDev 115.504 5.162%  3Sgma=15.486%
in 1995.0  Max 2409.2  Range 414.14
Mx-Mn)/(Mx+Mn) 9.40%  (-)/2Av 9.25%
min:10.84%  Lmax:7.67%  (-)/Av 18.51%
radients: R/2=5.736% ~R=12.089%
erit:  59.5  22%  29.5 77.9
sns 9.584 IdvMx 0.714 VsnsMx 37.7m
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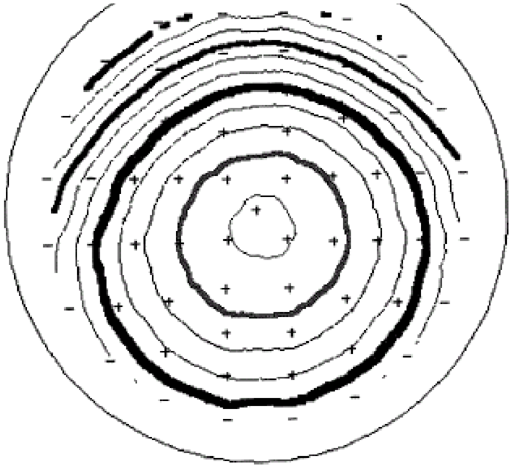
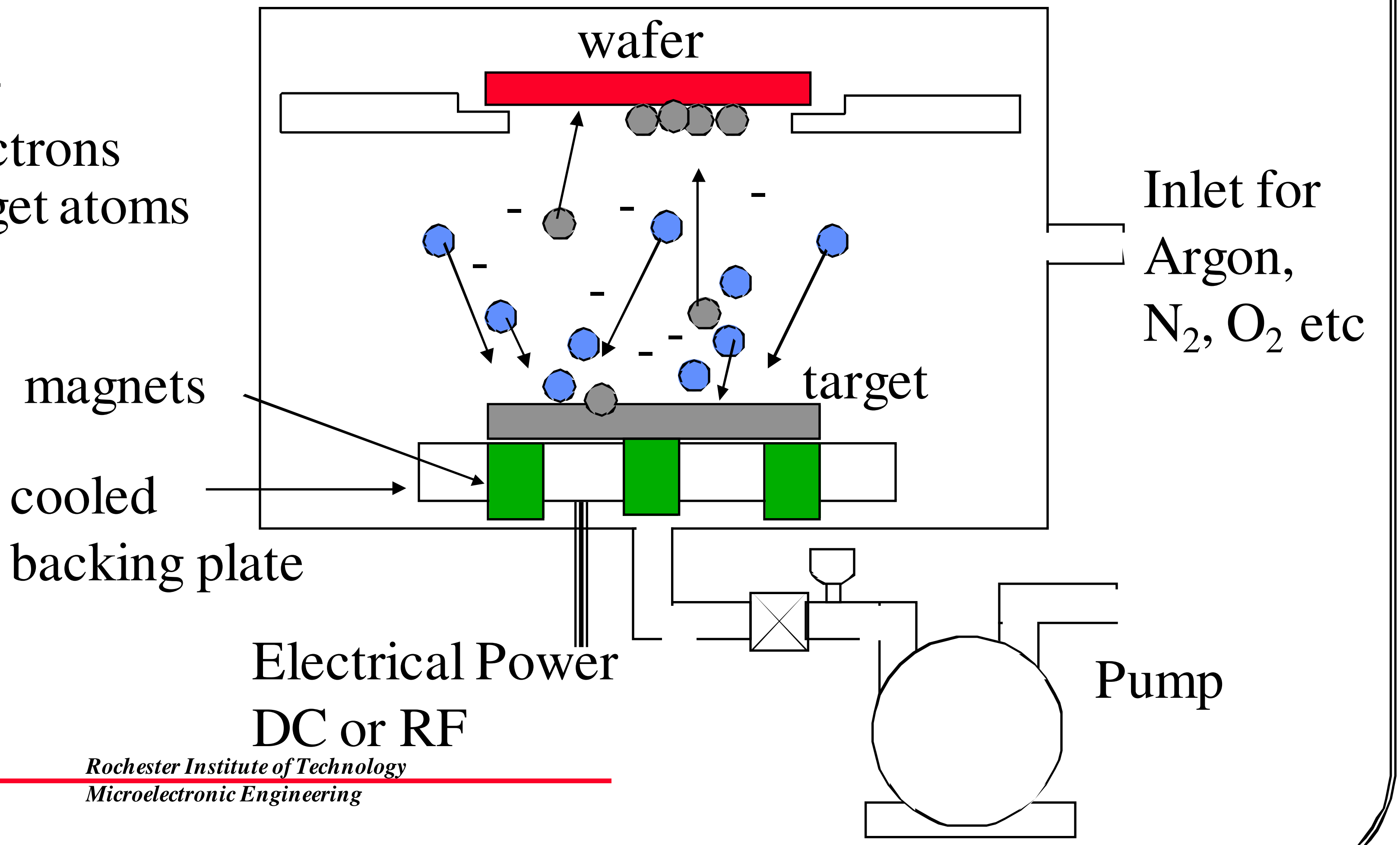


Ave = 2.03K
Min = 1.90K
Max = 2.18K
Non Uniformity = 6.95%

SPUTTERING

● Ar+
- electrons
● target atoms



wafer

Inlet for Argon, N_2, O_2 etc

target

magnets

cooled backing plate

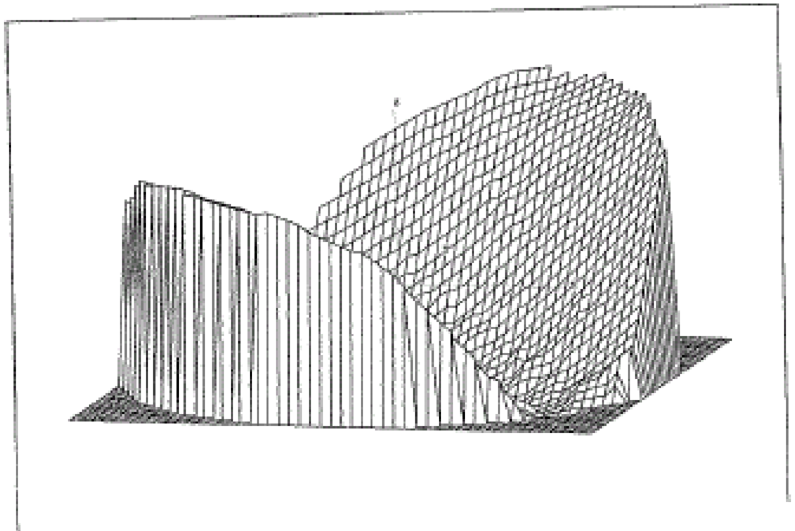
Electrical Power DC or RF

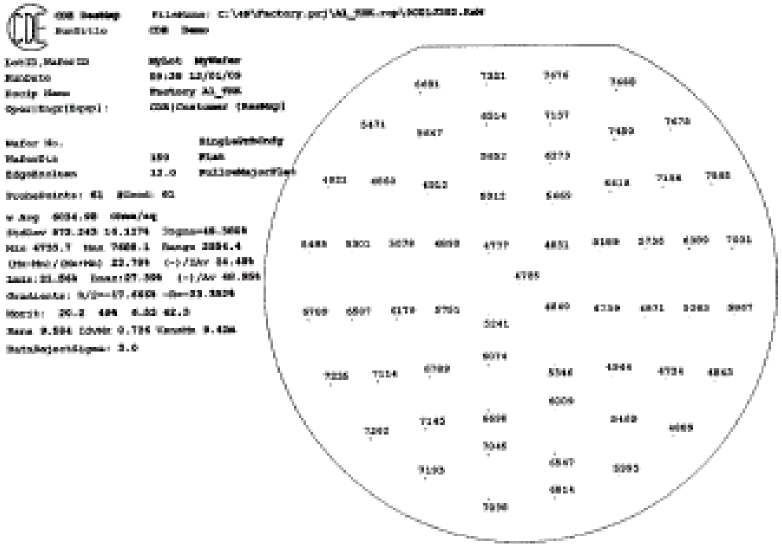
Pump

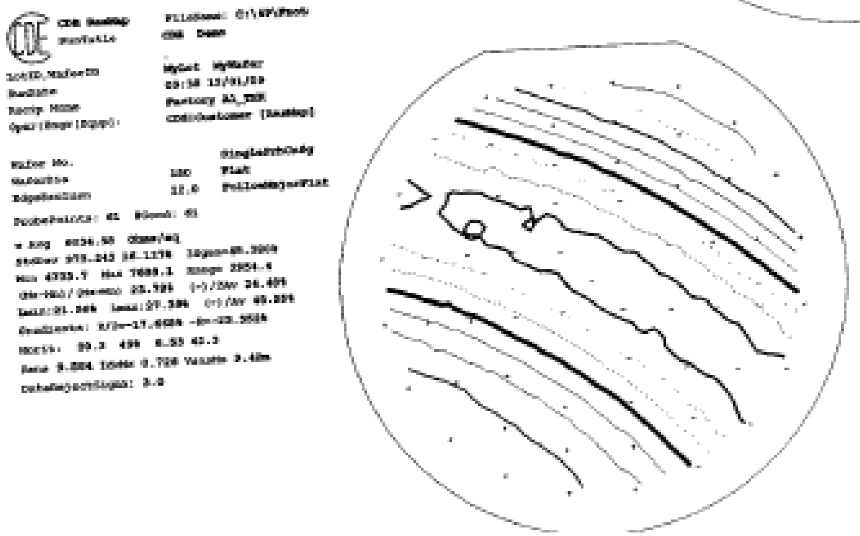
CVC 601 SPUTTER TOOL

CVC 601 Sputter Tool
Loading 6 inch wafers

CVC601 THICKNESS UNIFORMITY

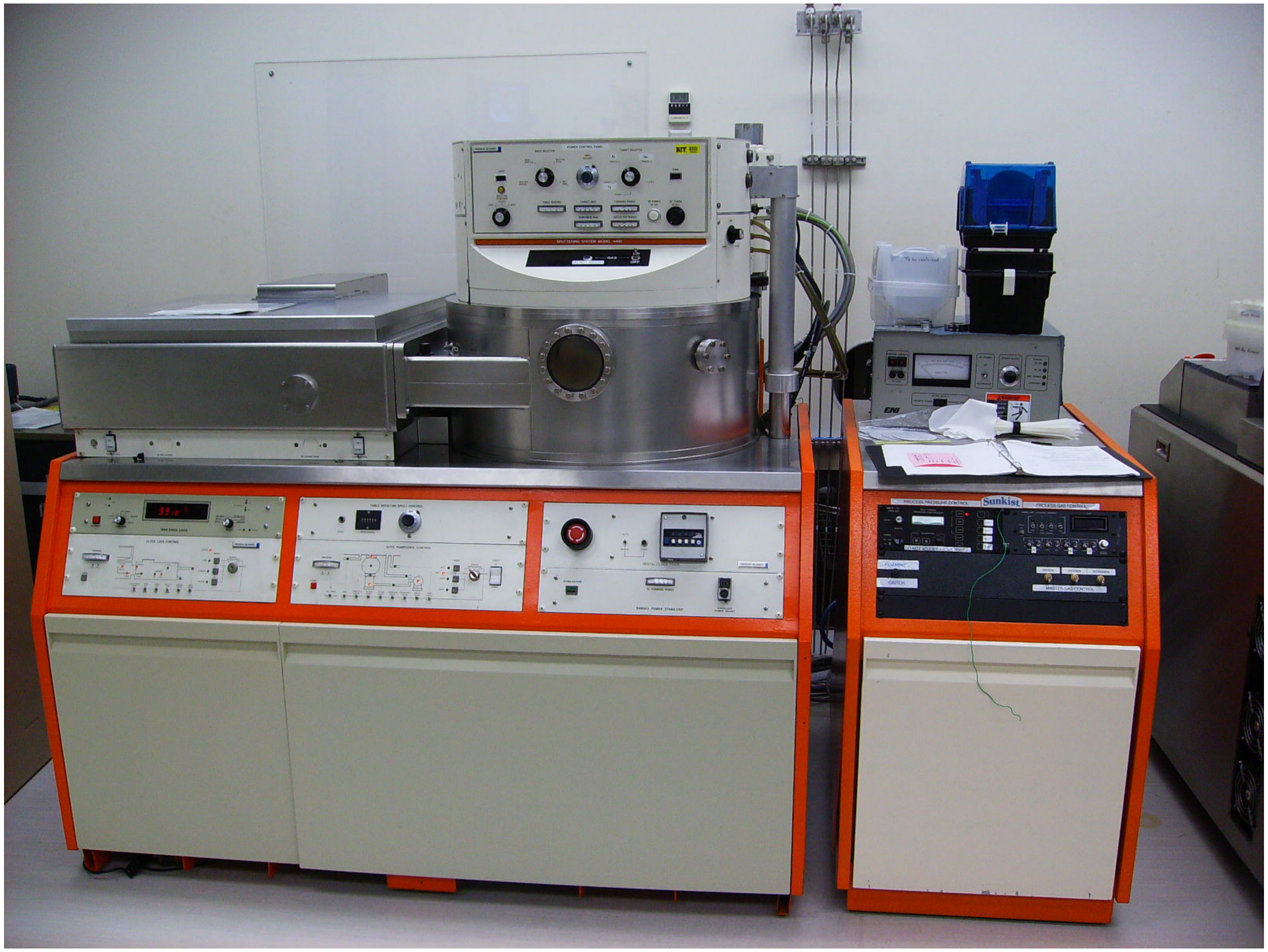




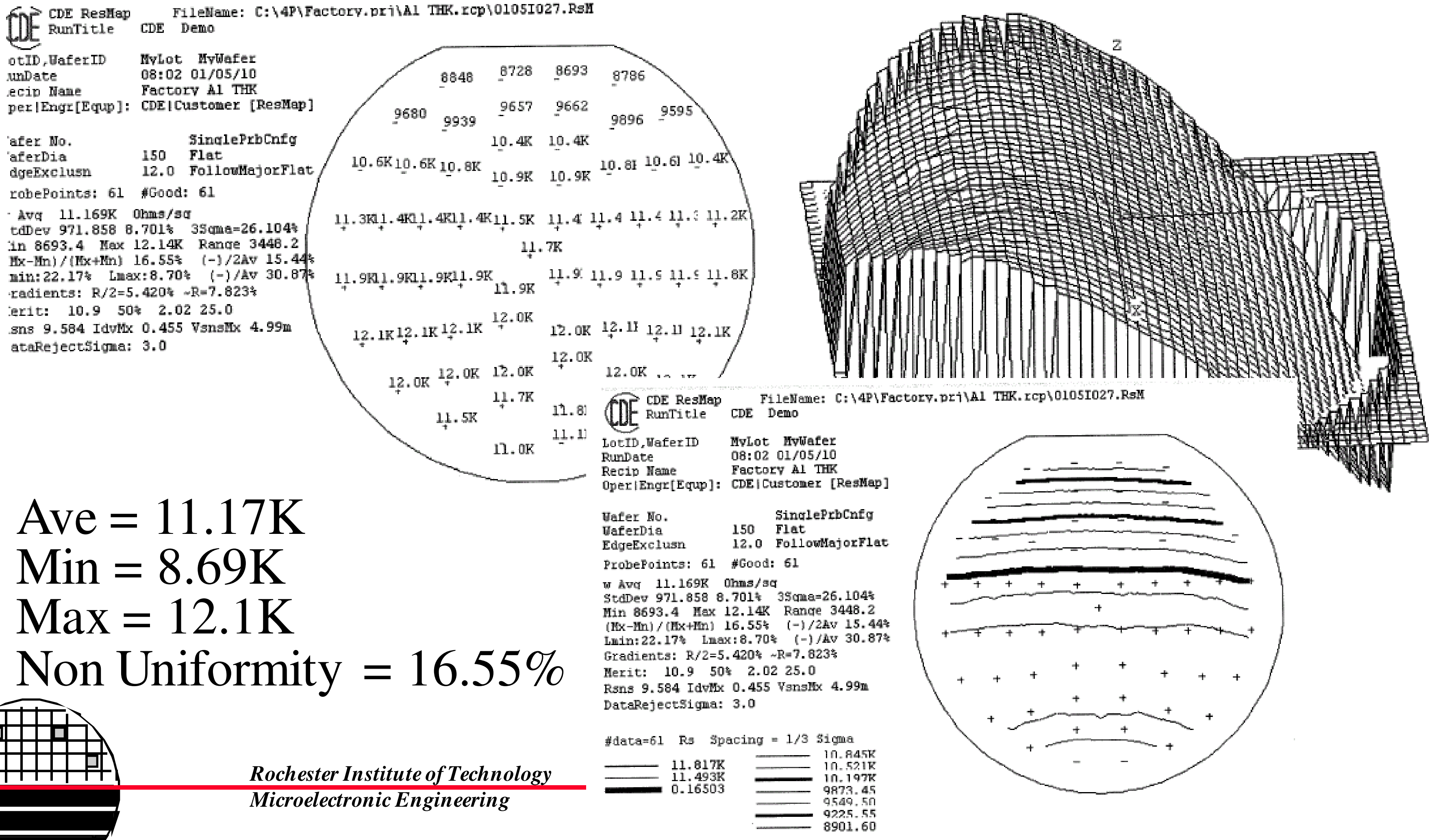


Ave = 6.03K
Min = 4.73K
Max = 7.68K
Non Uniformity = 23.78%

PE4400 SPUTTER TOOL



PE4400 – AL THICKNESS NON UNIFORMITY



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unDate             08:02 01/05/10
ecip Name          Factory Al THK
per|Engr[Equp]:    CDE|Customer [ResMap]

afer No.                  SinglePrbCnfg
aferDia            150    Flat
dgeExclusn         12.0   FollowMajorFlat
robePoints: 61    #Good: 61
 Avg   11.169K   Ohms/sq
tdDev 971.858 8.701%   3Sgma=26.104%
in 8693.4  Max 12.14K  Range 3448.2
Mx-Mn)/(Mx+Mn) 16.55%  (-)/2Av 15.44%
min:22.17%  Lmax:8.70%  (-)/Av 30.87%
radients: R/2=5.420% ~R=7.823%
erit:   10.9   50%   2.02 25.0
sns 9.584 IdvMx 0.455 VsnsMx 4.99m
ataRejectSigma: 3.0
```

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CDE ResMap      FileName: C:\4P\Factory.pri\Al THK.rcp\0105I027.RsM
RunTitle     CDE  Demo

LotID,WaferID       MyLot  MyWafer
RunDate             08:02 01/05/10
Recip Name          Factory Al THK
Oper|Engr[Equp]:    CDE|Customer [ResMap]

Wafer No.                  SinglePrbCnfg
WaferDia            150    Flat
EdgeExclusn         12.0   FollowMajorFlat
ProbePoints: 61    #Good: 61
w Avg   11.169K   Ohms/sq
StdDev 971.858 8.701%   3Sgma=26.104%
Min 8693.4  Max 12.14K  Range 3448.2
(Mx-Mn)/(Mx+Mn) 16.55%  (-)/2Av 15.44%
Lmin:22.17%  Lmax:8.70%  (-)/Av 30.87%
Gradients: R/2=5.420% ~R=7.823%
Merit:   10.9   50%   2.02 25.0
Rsns 9.584 IdvMx 0.455 VsnsMx 4.99m
DataRejectSigma: 3.0

#data=61  Rs  Spacing = 1/3 Sigma
                          ________  10.845K
________  11.817K         ________  10.521K
________  11.493K         ████████  10.197K
████████  0.16503         ________  9873.45
                          ________  9549.50
                          ████████  9225.55
                          ________  8901.60
```

Ave = 11.17K
Min = 8.69K
Max = 12.1K
Non Uniformity = 16.55%

Rochester Institute of Technology
Microelectronic Engineering

SPUTTERING

DC Sputtering - Sputtering can be achieved by applying large (~2000) DC voltages to the target (cathode). A plasma discharge will be established and the Ar+ ions will be attracted to and impact the target sputtering off target atoms. In DC sputtering the target must be electrically conductive otherwise the target surface will charge up with the collection of Ar+ ions and repel other argon ions, halting the process.

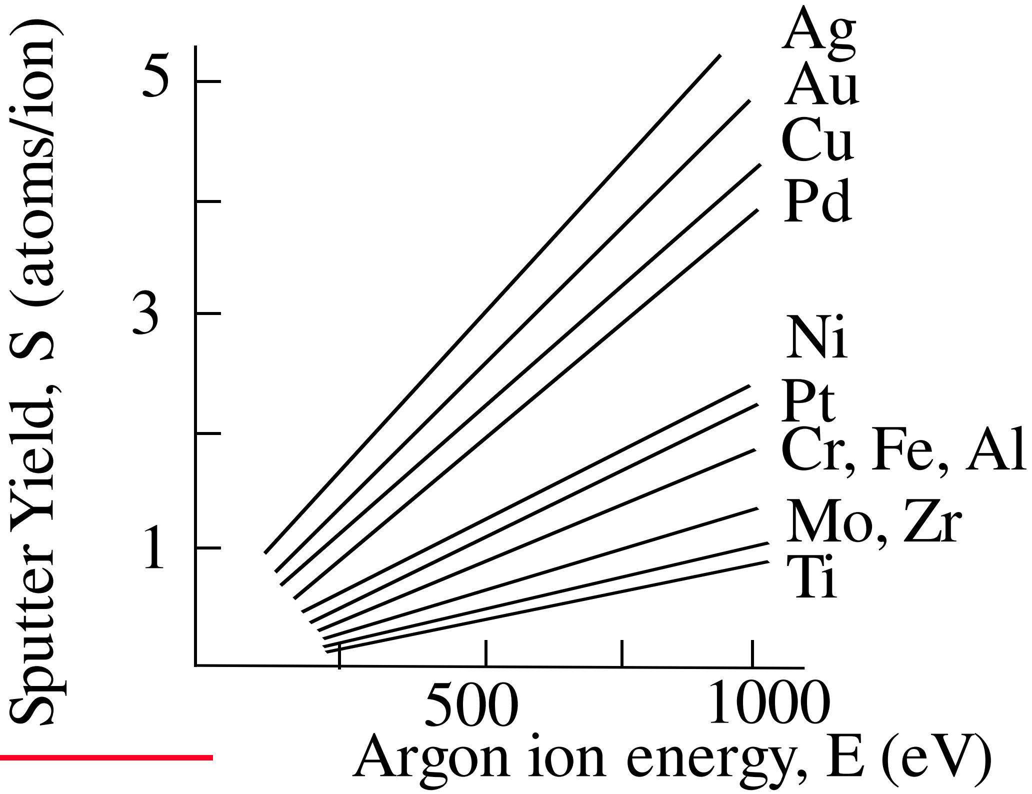
RF Sputtering - Radio Frequency (RF) sputtering will allow the sputtering of targets that are electrical insulators (SiO2, etc). The target attracts Argon ions during one half of the cycle and electrons during the other half cycle. The electrons are more mobile and build up a negative charge called self bias that aids in attracting the Argon ions which does the sputtering.

SPUTTERING

Magnetron Sputtering - Magnets buried in the baseplate under the target material cause the argon ions and electrons to concentrate in certain regions near the surface of the target. This increases the sputtering rate.

Deposition Rate ~ JSE

J is current density
S is sputter yield
E is ion energy



SPUTTER TARGETS

PE 2400 Targets

Au
Zr
SiO2 Qty2
Si Qty2
TiO2
Nb2O5
In2O5 Qty2
Permalloy
Fe
AlNi
NiFeMg
Ni
Co

Ta2O5
Cr
Ta
Mg
NiFe
CrSiO
Nb
SnO2
Al2O3
MgF2
MgO
Target Insulators 3
Backing Plates6

2” Unbonded for Denton

Gold
Palladium

CVC 601

SPUTTER TARGETS

8” Bonded for CVC-601

Aluminum 100%
Aluminum Oxide
Aluminum/1% Silicon
Chrome
Chrome Oxide
Copper
Molybdenum
Tantalum
Titanium
Titanium10%/Tungsten 90%
Silicon Dioxide
Silicon
Indium Tin Oxide

8”Unbonded for CVC-601

Molybdenum/Titanium
Titanium/Al 1%/Silicon 2%

4” Unbonded for CVC 601

Chrome
Indium 90%/Tin 10%
Nickel
Tantalum
Tin
Nickel-Chromium 80%/20%

108E-6 ohm cm, TCR 110 E-6/°C
$450- 4”x1/4” Mel Hollander, Research and PVD Materials Corp. (973) 575-4245

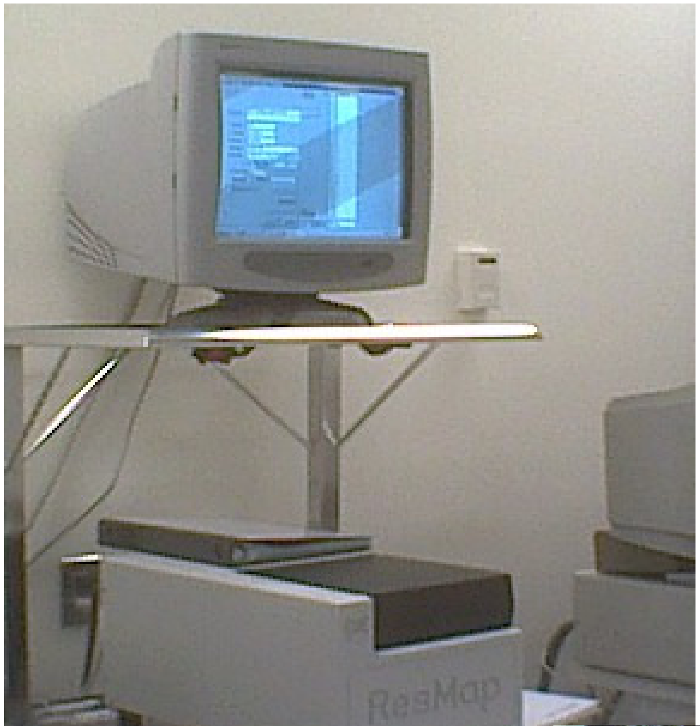
RIT SPUTTERING DATA

Material	Head	Power (watts)	Rate
Aluminum	8”	2000	240 Å/min.
Nickel	4”	500	170
Chromium	8”	1350	350
InSn + O2	4”	100	80
Copper	8”	325	110
Gold*	2”	40 mA,50mTorr	250
Tantalum	4”	500	190
Titanium	8”	1350	220
Tungsten	4”	500	100
Tungsten	8”	1000	115
Palladium#	2”	10mA, 90 mTorr	100

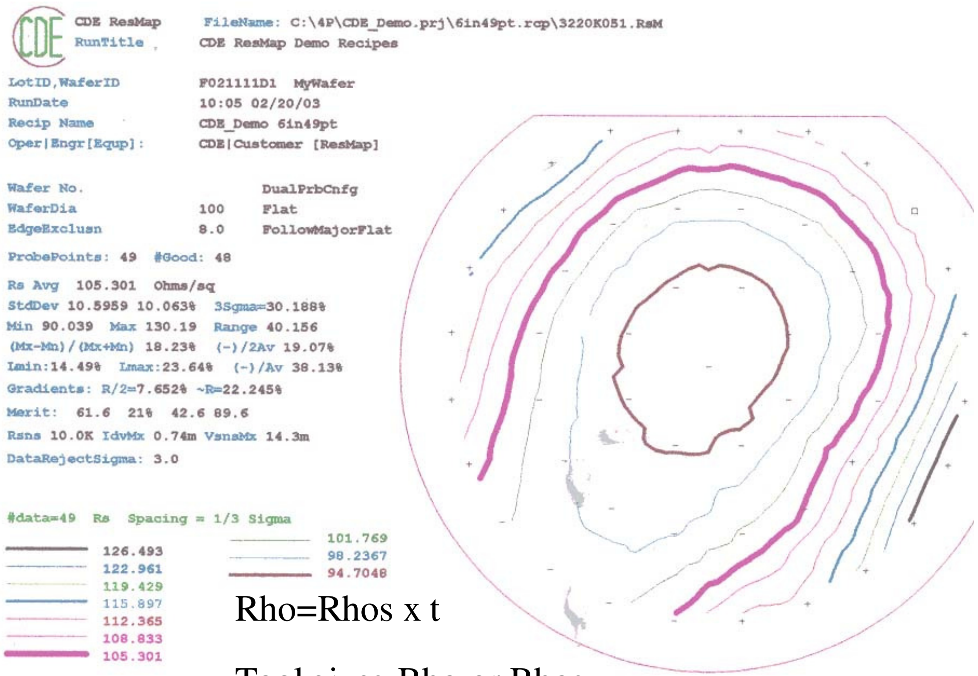
This data is for the CVC 601 Sputter System at 5 mTorr Argon Pressure, Base Pressure Prior to Sputter <1E-5

*Denton Sputter Machine

4 PT PROBE WAFER THICKNESS MEASUREMENTS



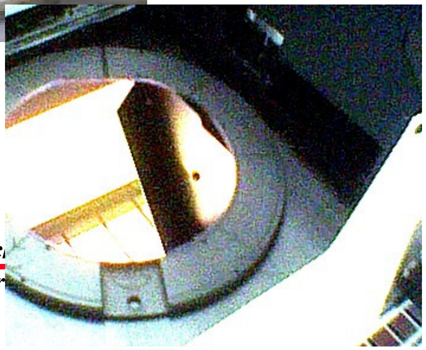
CDE Resistivity Mapper



```
CDE ResMap      FileName: C:\4P\CDE_Demo.prj\6in49pt.rcp\3220K051.RsM
RunTitle        CDE ResMap Demo Recipes

LotID,WaferID          F021111D1  MyWafer
RunDate                10:05 02/20/03
Recip Name             CDE_Demo 6in49pt
Oper|Engr[Equp]:       CDE|Customer [ResMap]

Wafer No.                    DualPrbCnfg
WaferDia               100   Flat
EdgeExclusn            8.0   FollowMajorFlat

ProbePoints: 49  #Good: 48

Rs Avg  105.301  Ohms/sq
StdDev 10.5959 10.063%  3Sgma=30.188%
Min 90.039  Max 130.19  Range 40.156
(Mx-Mn)/(Mx+Mn) 18.23%  (-)/2Av 19.07%
Lmin:14.49%  Lmax:23.64%  (-)/Av 38.13%
Gradients: R/2=7.652% ~R=22.245%
Merit:  61.6  21%  42.6 89.6
Rsns 10.0K IdvMx 0.74m VsnsMx 14.3m
DataRejectSigma: 3.0

#data=49  Rs  Spacing = 1/3 Sigma

126.493                101.769
122.961                98.2367
119.429                94.7048
115.897
112.365
108.833
105.301
```

Rho=Rhos x t

Tool gives Rho or Rhos depending on recipe used, automatically adjusts correction factors for wafer thickness



$$\boxed{t = Rho/Rhos}$$

EQUATIONS USE BY CDE RESISTIVITY MAPPER

$$\text{Thickness} = \frac{\text{Known Bulk Resistivity}}{\text{Measured Sheet Resistance}}$$

Bulk Resistivity is assumed to be known

Measured Sheet Resistance = $(\pi/\ln 2)(V/I)$

The CDE Resistivity Mapper can be programmed to automatically convert measured V/I to thickness

$$\text{Uniformity} = (\text{Max}-\text{Min})/(\text{Max}+\text{Min})$$

MODELING OF BULK RESISTIVITY

Bulk Resistivity is assumed to have a value = $x \ \mathrm{Exp}^{(y)}$

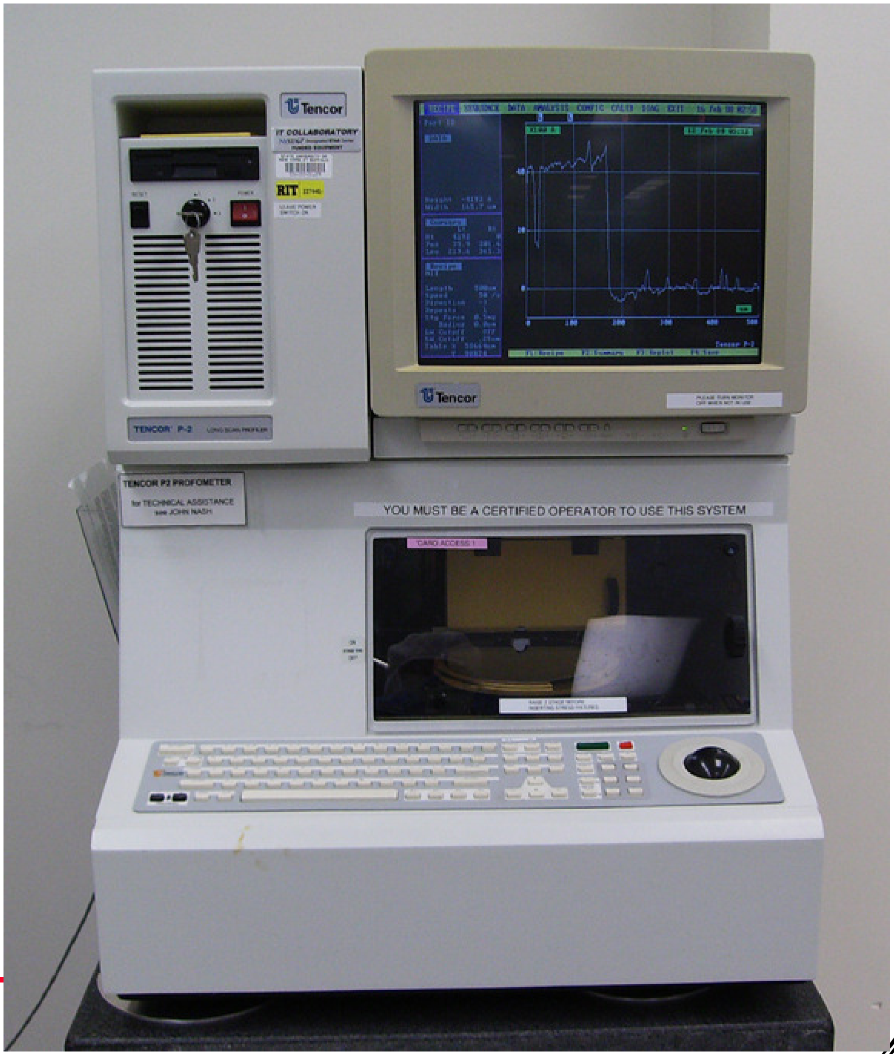
Where the pre exponential value may be different for different film deposition techniques (i.e. evaporation, RF sputtering, DC sputtering, etc.)

	x	**y**	**Rho ohm-Å**
CDE Manual	**337.17**	**-0.92401**	**133.8**
PE4400 (300watts)	**412**	**-0.92401**	**163.5**
CVC601	**540**	**-0.92401**	**214.3**
Flash Evaporator	**490**	**-0.92401**	**194.5**

Note: bulk Aluminum Rho = 270 ohm-Å

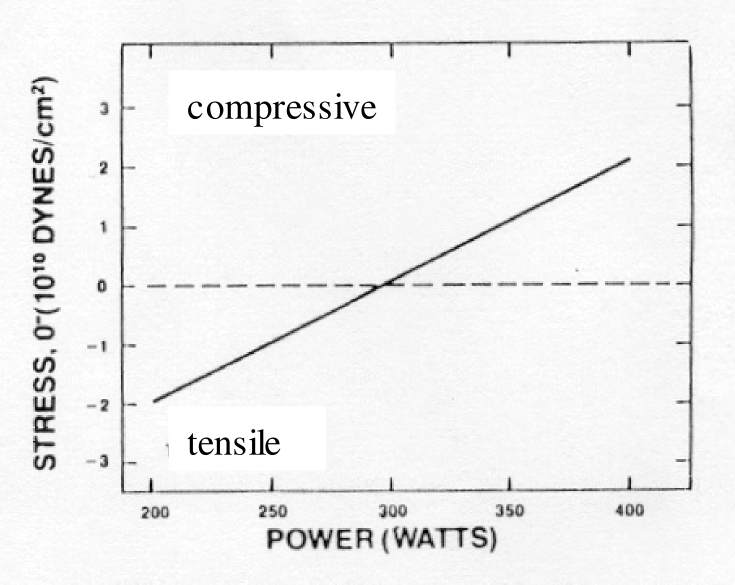
VERIFICATION USING THE TENCORE P2

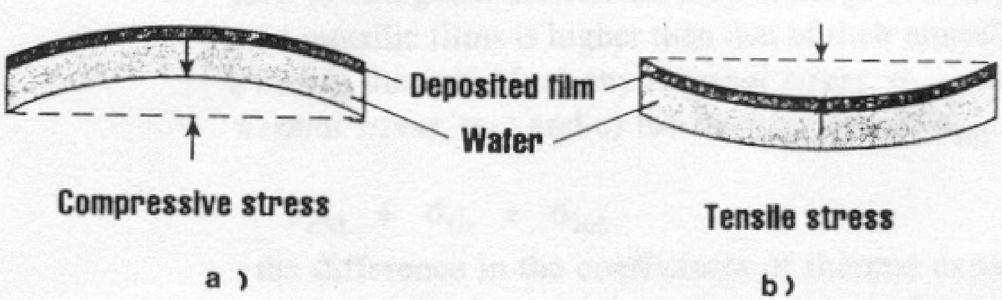
```
Part ID
DATA

Height   -4192 A
Width    165.7 um

Cursors
        Lt      Rt
Ht    4192       0
Pos   35.9   201.6
Lev  219.6   365.3

Recipe
NIT

Length       500um
Speed         50 /s
Direction       ->
Repeats          1
Sty Force    0.5mg
    Radius   0.0um
LW Cutoff      OFF
SW Cutoff    .25um
Table X    58664um
      Y      98874
```



STRESS IN SPUTTERED FILMS

Compressively stressed films would like to expand parallel to the substrate surface, and in the extreme, films in compressive stress will buckle up on the substrate. Films in tensile stress, on the other hand, would like to contract parallel to the substrate, and may crack if their elastic limits are exceeded. In general stresses in films range from 1E8 to 5E10 dynes/cm2.





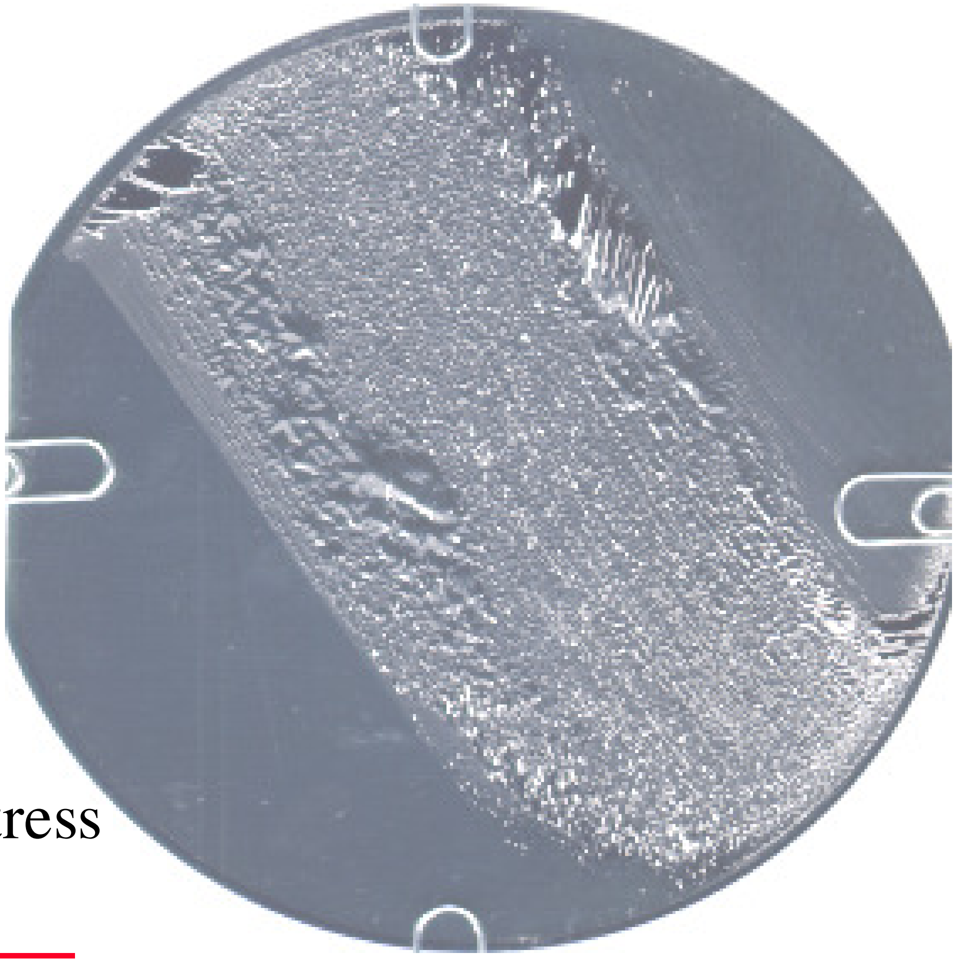
For AVT sputtered oxide films
Dr. Grande found Compressive
18MPa stress, 1-29-2000

10 dyne/cm^2 = 1 newton/m^2 = 1 Pascal

STRESS IN SPUTTERED TUNGSTEN FILMS

Tungsten

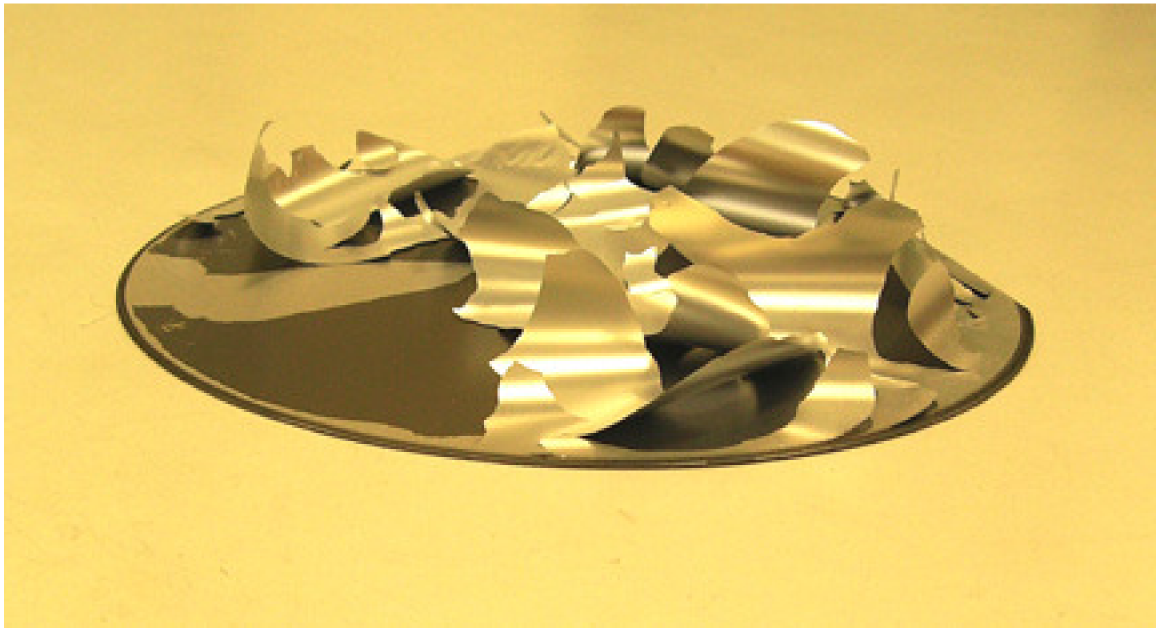
- CVC 601
- 4” Target
- 500 Watts
- 50 minutes
- 5 mTorr Argon
- Thickness ~ 0.8 µm



Compressive Stress

Picture from scanner in gowning

STRESS IN SPUTTERED ALUMINUM FILMS



Tensile Stress

REACTIVE SPUTTERING

Reactive Sputtering - introducing gases such as oxygen and nitrogen during sputtering can result in the deposition of films such as indium tin oxide (ITO) or titanium nitride TiN (other examples include AlN, Al_2O_3, AnO Ta_2O_5)

Unwanted Background Gases in Sputtering - Most Films are very reactive when deposited. Water and oxygen cause rougher films, poorer step coverage, discoloration (brown aluminum), poorer electrical properties, etc.

REACTIVE SPUTTERING PROCESSES

Deposition of Reactive Sputtered Ta2O5

CVC 601, 25% Oxygen, 75% Argon, 90 min, 500 watts, 4 inch target resulting in ~5000 Å, nanospec should use index of refraction of 2.2

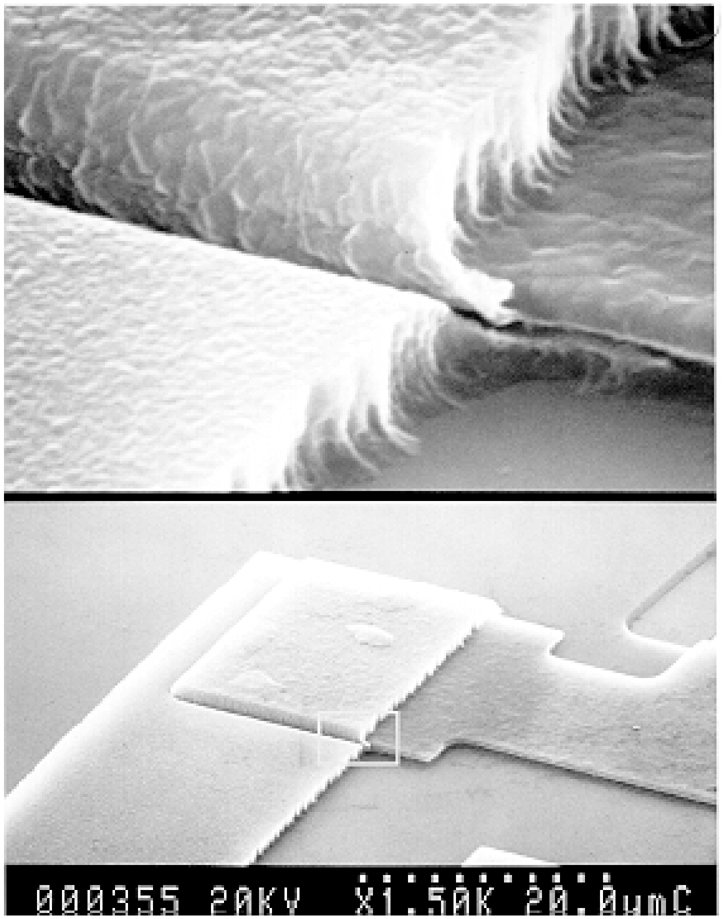
Deposition of Reactive Sputtered TaN

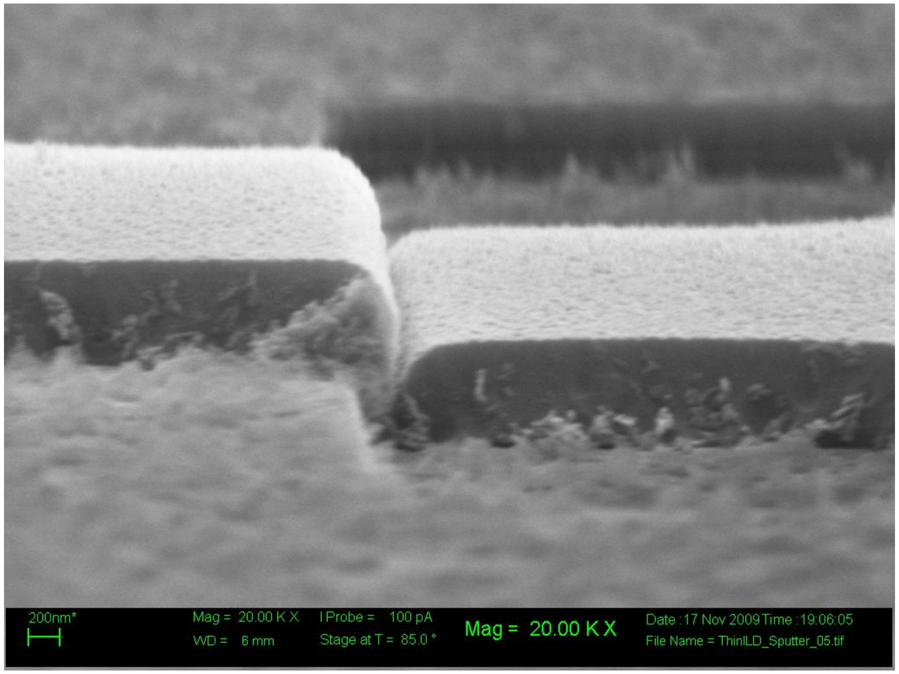
CVC 601, 8" Target of Ta, Ar 170 sccm, N2 34 sccm, Pressure = 4 mTorr, 2000 W, Rate ~900 Å/15 min

Deposition of Reactive Sputtered TaN

CVC 601, 4" Target of Ta, Ar 62 sccm, N2 34 sccm, Pressure = 6 mTorr, 500 W, Rate=157 Å/min, Rhos=228 ohms

STEP COVERAGE



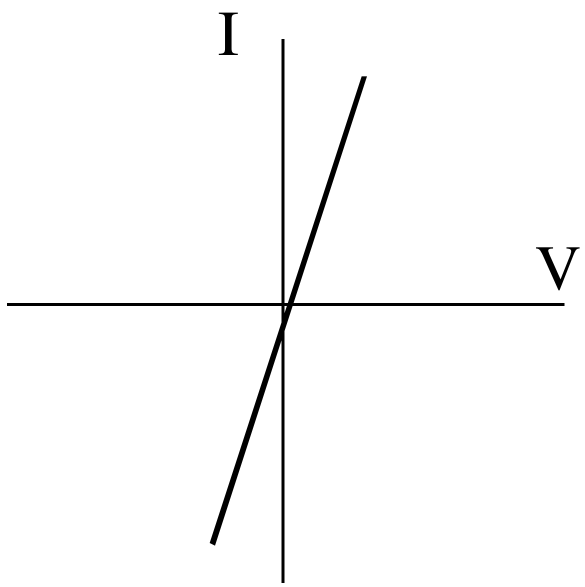


These SEM pictures show typical profiles of aluminum over steps from the CVC601.

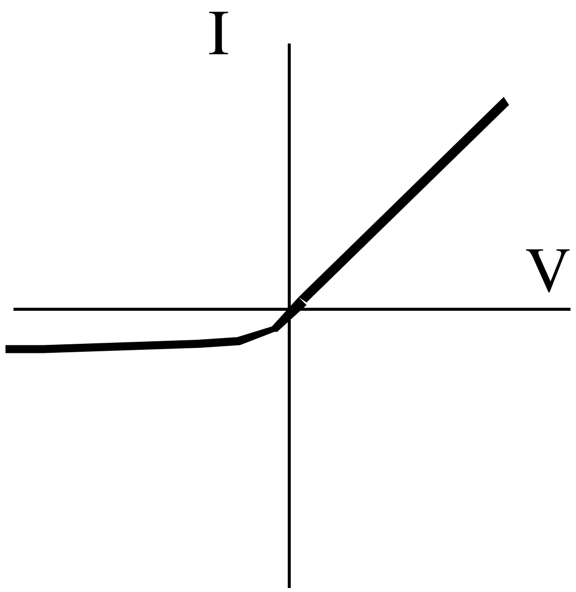
SUMMARY FOR DEPOSITION, UNIFORMITY and STEP COVERAGE

1. None of the deposition tools are that great from a thickness uniformity point of view. The best tool we investigated is the Cha Flash Evaporator.
2. The PE 4400 is the only tool that can do sputter etch prior to metal deposition. So we need to use this tool for the 2nd layer of aluminum.
3. The four point probe technique for measuring thickness is a good way to measure uniformity.
4. Step coverage can be a problem so we choose to deposit metal thickness larger than the step height. Our metal thicknesses are 0.75µm for metal one and two.

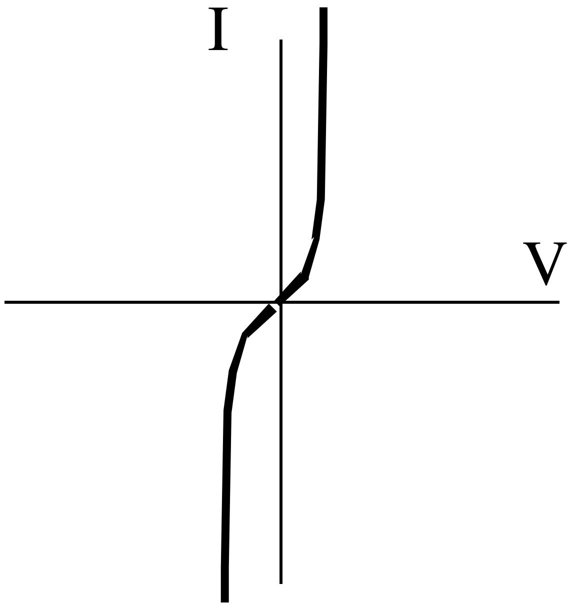
CONTACTS TO SILICON



Ideal Ohmic
Al/p-silicon



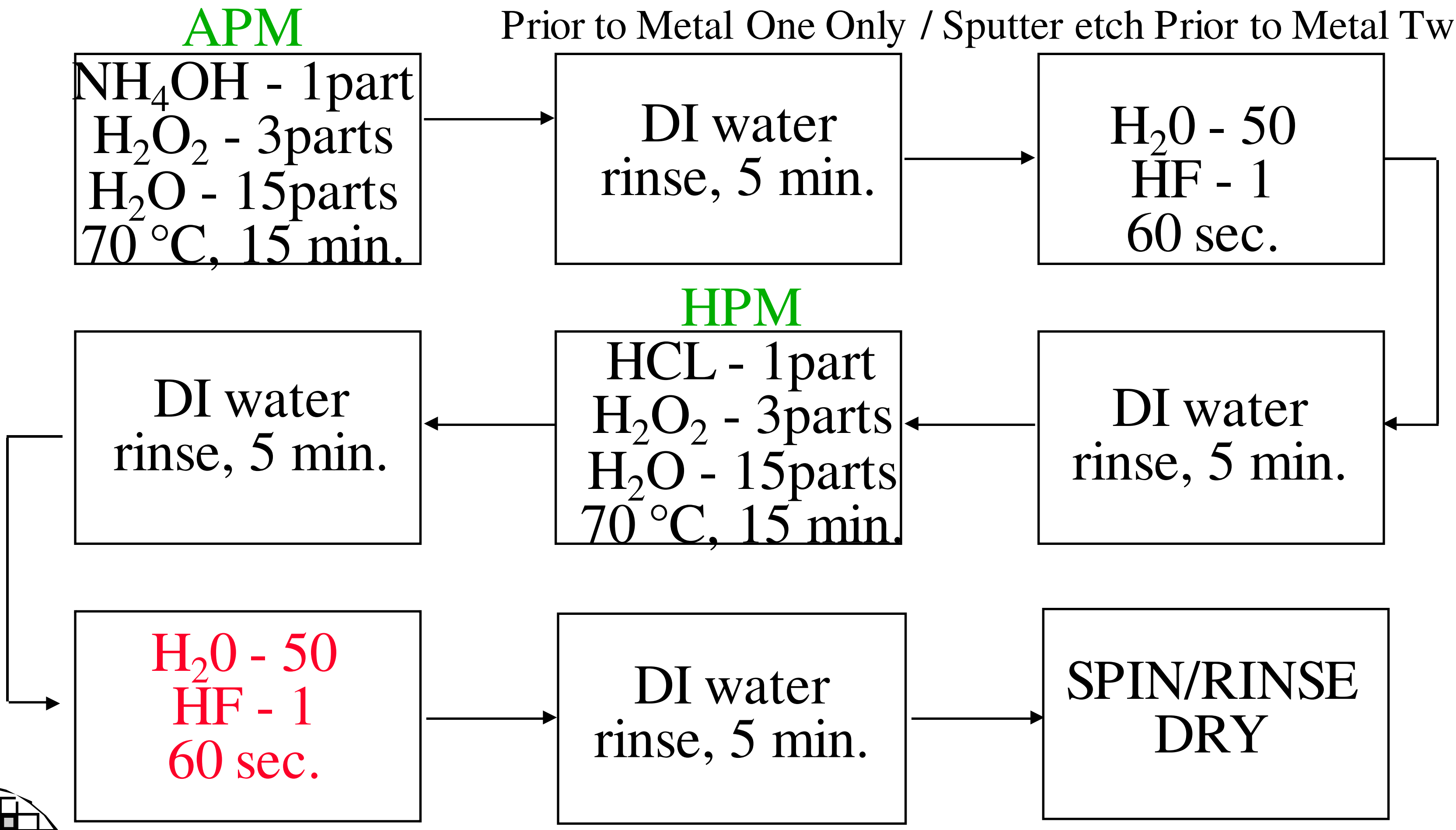
Rectifying
Al/n-silicon



Tunneling Ohmic
Al/n+-silicon

SPECIAL RCA CLEAN PRIOR TO METAL ONE

Prior to Metal One Only / Sputter etch Prior to Metal Two



APM

NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water rinse, 5 min.

H_20 - 50
HF - 1
60 sec.

DI water rinse, 5 min.

HPM

HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water rinse, 5 min.

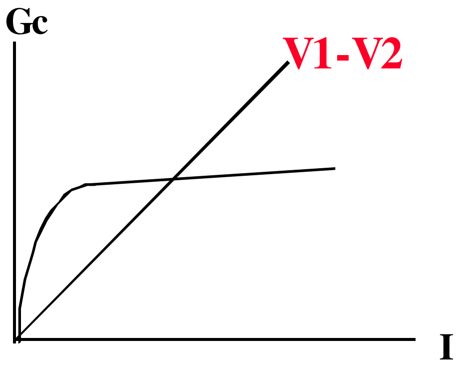
H_20 - 50
HF - 1
60 sec.

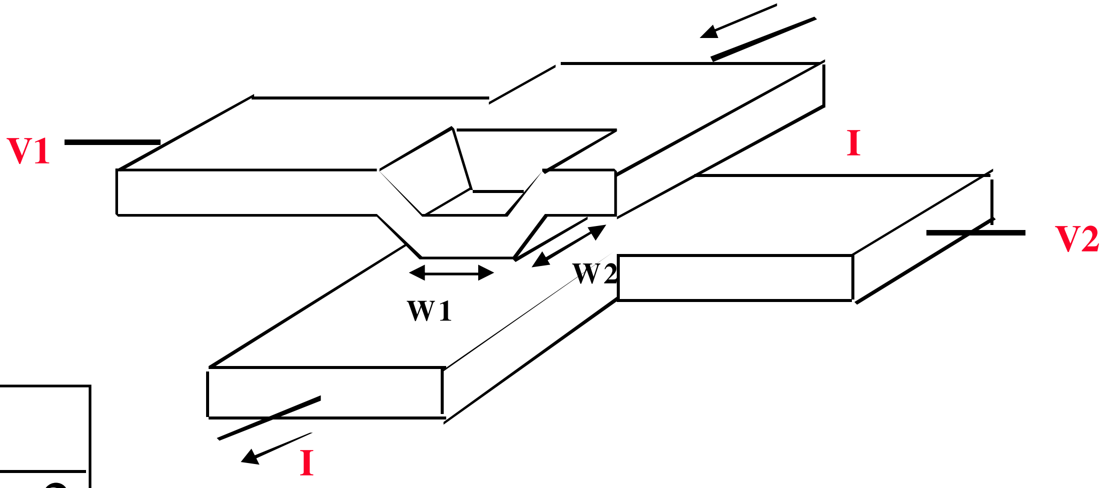
DI water rinse, 5 min.

SPIN/RINSE DRY

Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide

CONTACT RESISTANCE





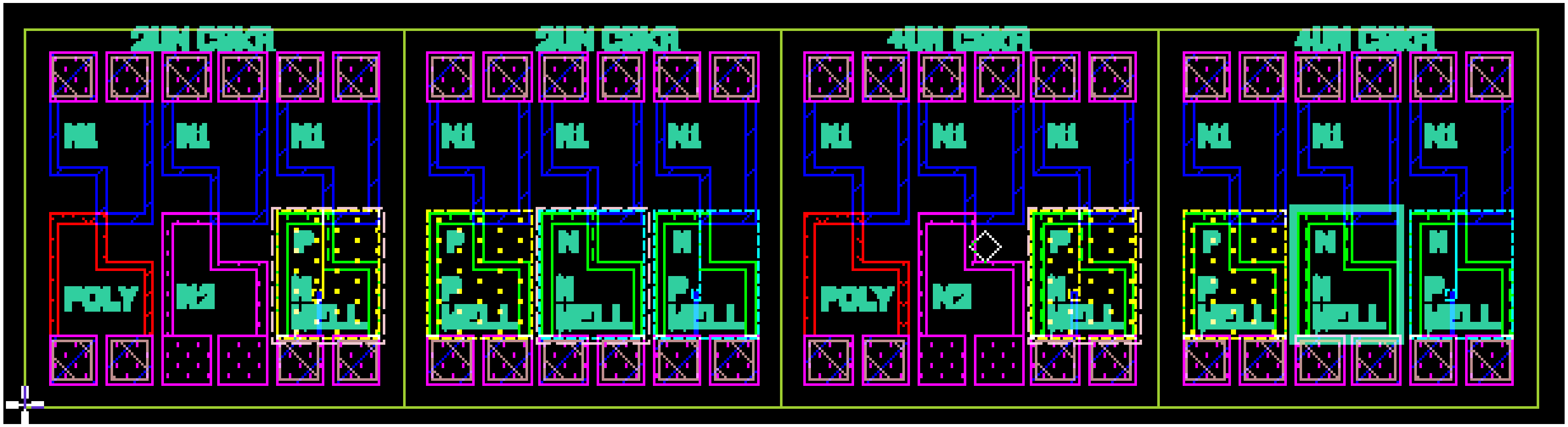
Metal	Rc
Al:Si/n+ Si	15 Ω - µm2
Al:Si/TiN/n+Si	1.0
Al:Si/TiN/p+Si	2.0
Al/Ti:W/TiSi2/n+Si	19
Al/TiW/TiSi2/p+Si	70

$$R = \frac{(V1-V2)}{I} \quad \text{ohms}$$

$$Gc = \frac{I}{(V1-V2)} \; \frac{1}{W1 \times W2} \quad \text{mhos}/\mu m^2$$

$$Rc = 1/Gc \quad \text{ohms - } \mu m^2$$

CBKR's



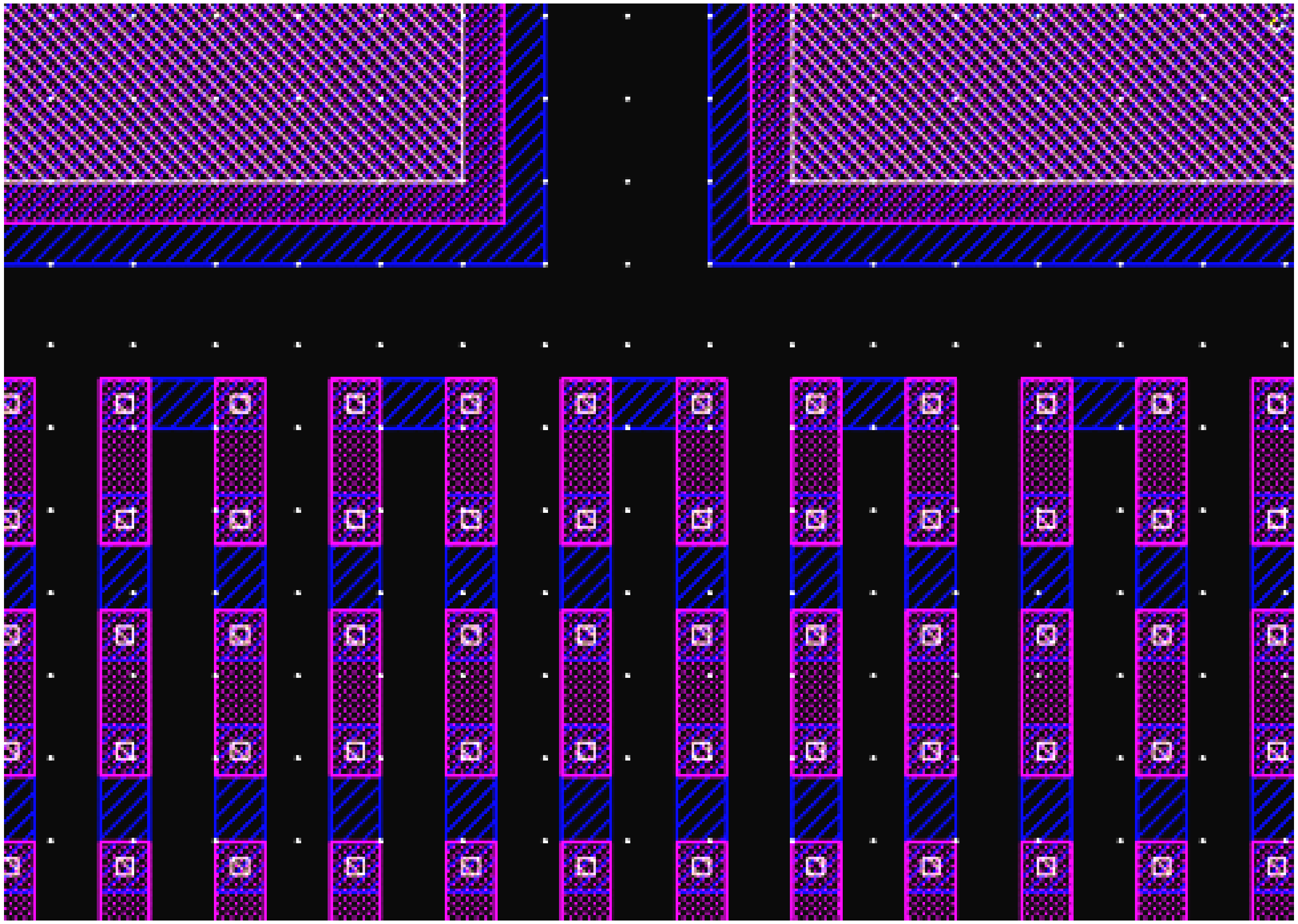
2µm M1toPoly
2µm M1toM2
2µm M1toP+

2µm M1toP+
2µm M1toN+
2µm M1toN+

4µm M1toPoly
4µm M1toM2
4µm M1toP+

4µm M1toP+
4µm M1toN+
4µm M1toN+

VIA CHAINS



Via Chain has 512 Vias

DRYTEK QUAD ETCH RECIPE FOR CC AND VIA

Recipe Name:		FACCUT
Chamber		3
Power		200W
Pressure		100 mTorr
Gas 1	CHF3	50 sccm
Gas 2	CF4	10 sccm
Gas 3	Ar	100 sccm
Gas 4	O2	0 sccm

(could be changed to N2)

TEOS Etch Rate	494	Å/min
Annealed TEOS	450	Å/min
Photoresist Etch Rate:	117	Å/min
Thermal Oxide Etch Rate:	441	Å/min
Silicon Etch Rate	82	Å/min
TiSi2 Etch Rate	1	Å/min

US Patent 5935877 - Etch process for forming contacts over titanium silicide

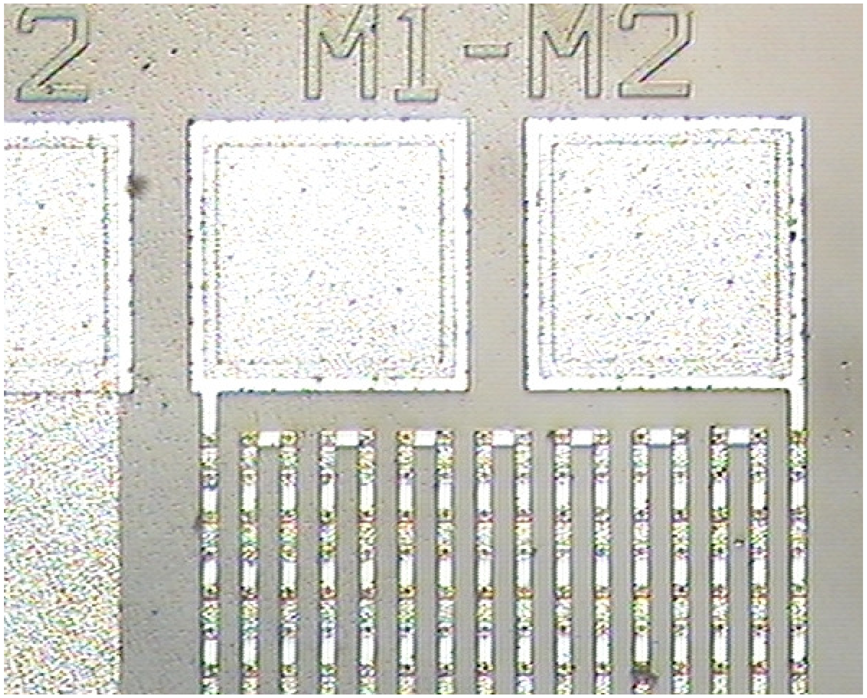
Drytek Quad

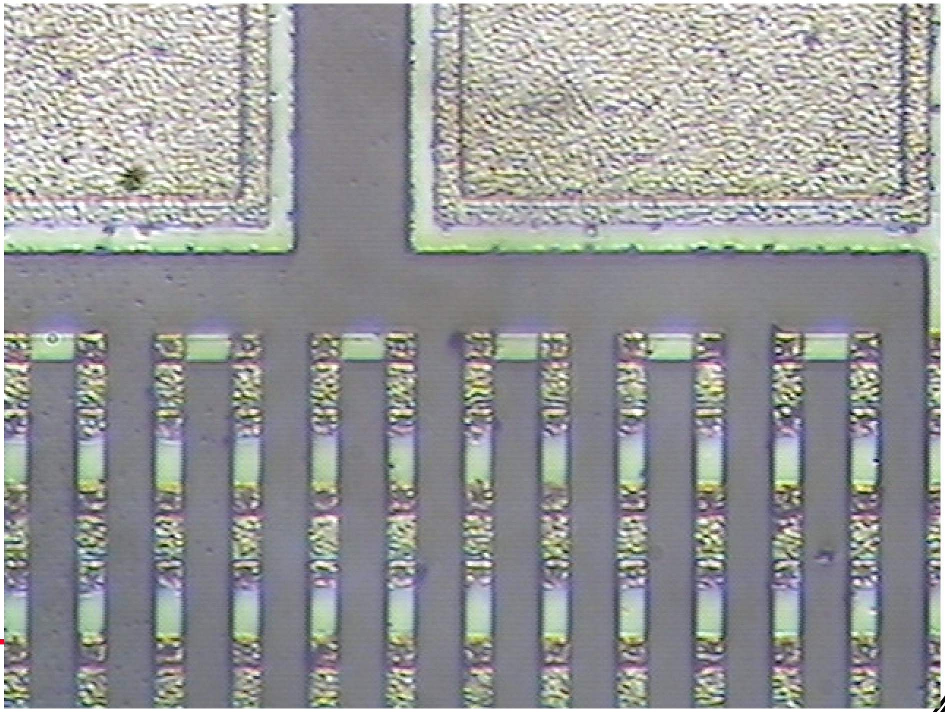
CONTACT CUT ETCH RECIPE

Theory: The CHF3 and CF4 provide the F radicals that do the etching of the silicon dioxide, SiO2. The high voltage RF power creates a plasma and the gasses in the chamber are broken into radicals and ions. The F radical combines with Si to make SiF4 which is volatile and is removed by pumping. The O2 in the oxide is released and also removed by pumping. The C and H can be removed as CO, CO2, H2 or other volatile combinations. The C and H can also form hydrocarbon polymers that can coat the chamber and wafer surfaces. The Ar can be ionized in the plasma and at low pressures can be accelerated toward the wafer surface without many collisions giving some vertical ion bombardment on the horizontal surfaces. If everything is correct (wafer temperature, pressure, amounts of polymer formed, energy of Ar bombardment, etc.) the SiO2 should be etched, polymer should be formed on the horizontal and vertical surfaces but the Ar bombardment on the horizontal surfaces should remove the polymer there. The O2 (O radicals) released also help remove polymer. Once the SiO2 is etched and the underlying Si is reached there is less O2 around and the removal of polymer on the horizontal surfaces is not adequate thus the removal rate of the Si is reduced. The etch rate of SiO2 should be 4 or 5 times the etch rate of the underlying Si. The chamber should be cleaned in an O2 plasma after each wafer is etched.

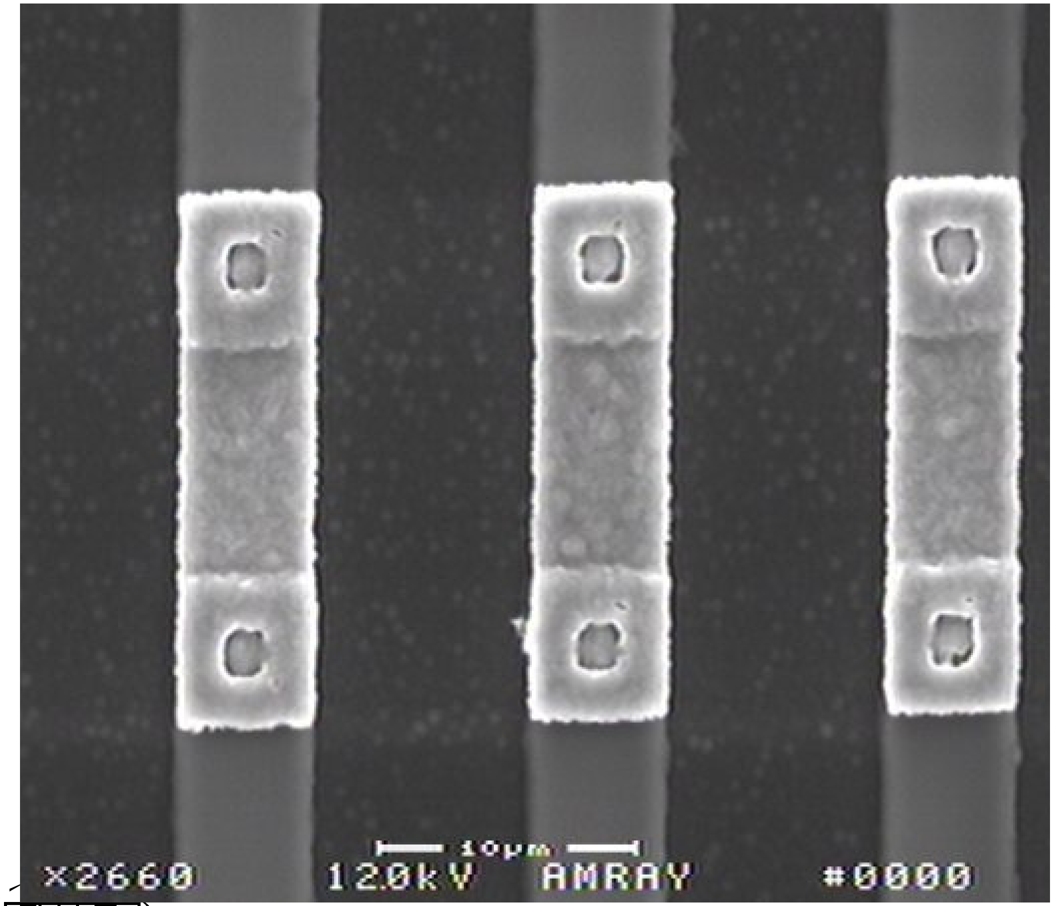
US Patent 5935877 - Etch process for forming contacts over Titanium Silicide

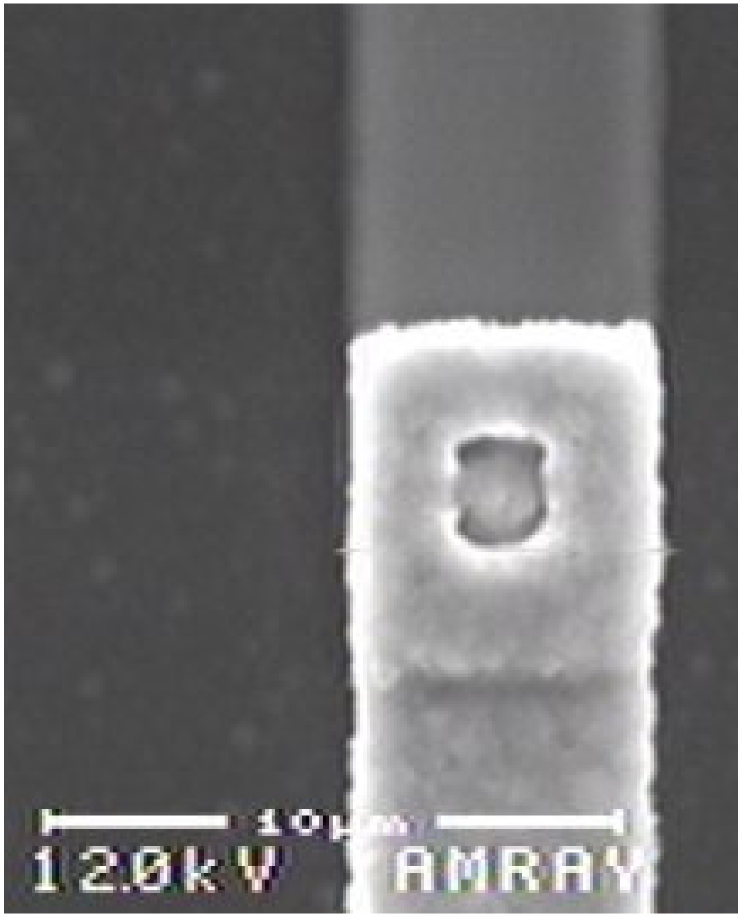
PICTURES OF M1-M2 VIA CHAIN





SEM OF 6μm LINES / 2X2μm VIAS

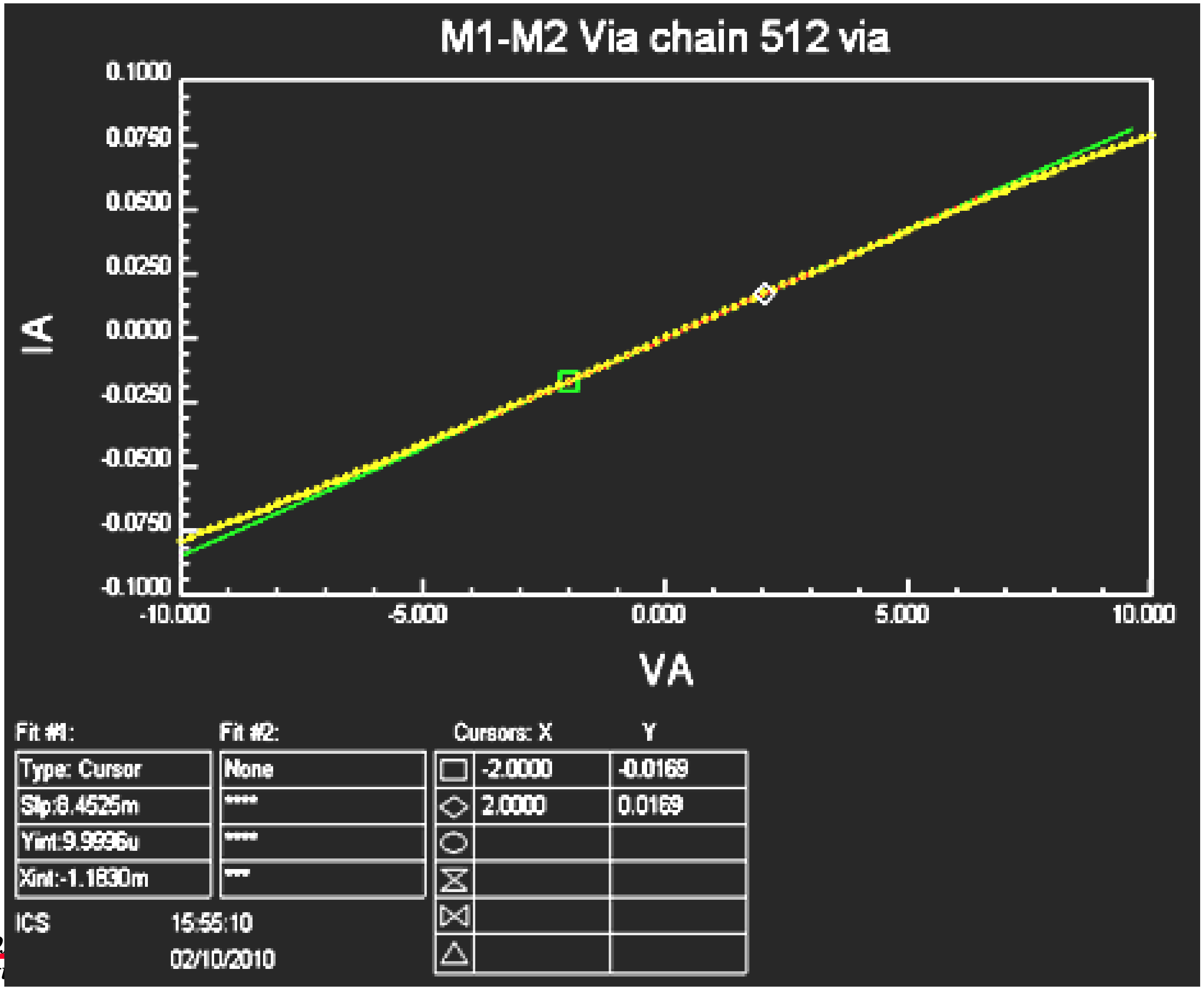




RESISTANCE MEASUREMENTS FOR M1-M2 VIA CHAIN

F081201

M1-M2 Via chain with 512 Vias and total resistance of 118 ohms or 0.231 ohms per contact

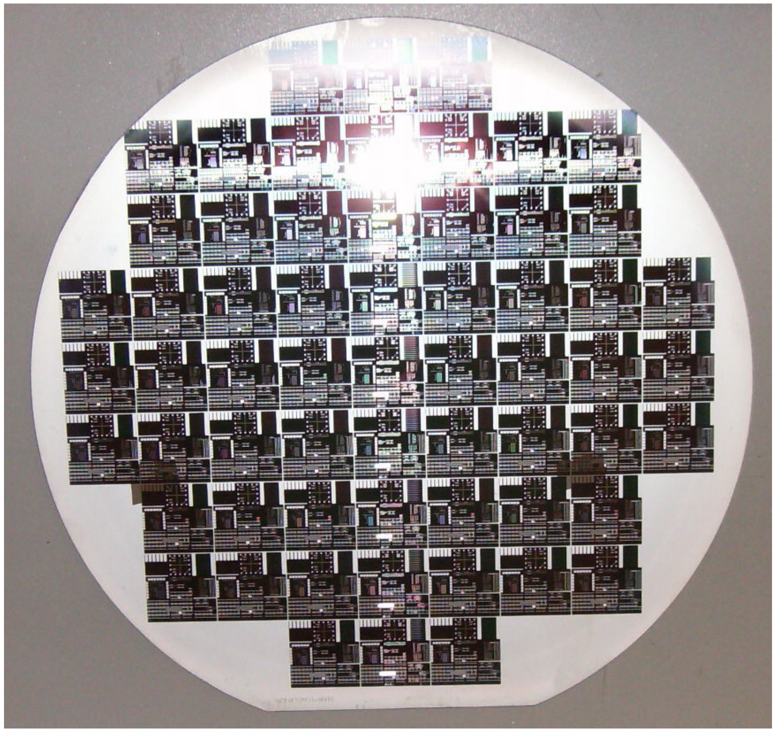


Fit #1:	Fit #2:
Type: Cursor	None
Slp:8.4525m	****
Yint:9.9996u	****
Xint:-1.1830m	***

	Cursors: X	Y
□	-2.0000	-0.0169
◇	2.0000	0.0169
○		
⧗		
⋈		
△		

ICS 15:55:10
02/10/2010

ALUMINUM ETCH USING LAM4600



LAM 4600 ALUMINUM ETCHER

Plasma Chemistry

- Cl_2 – Reduces Pure Aluminum
- BCl_3 – Etches native Aluminum Oxide
  - -Increases Physical Sputtering
- N_2 – Dilute and Carrier for the chemistry
- Chloroform – Helps Anisotropy and reduces Photoresist damage

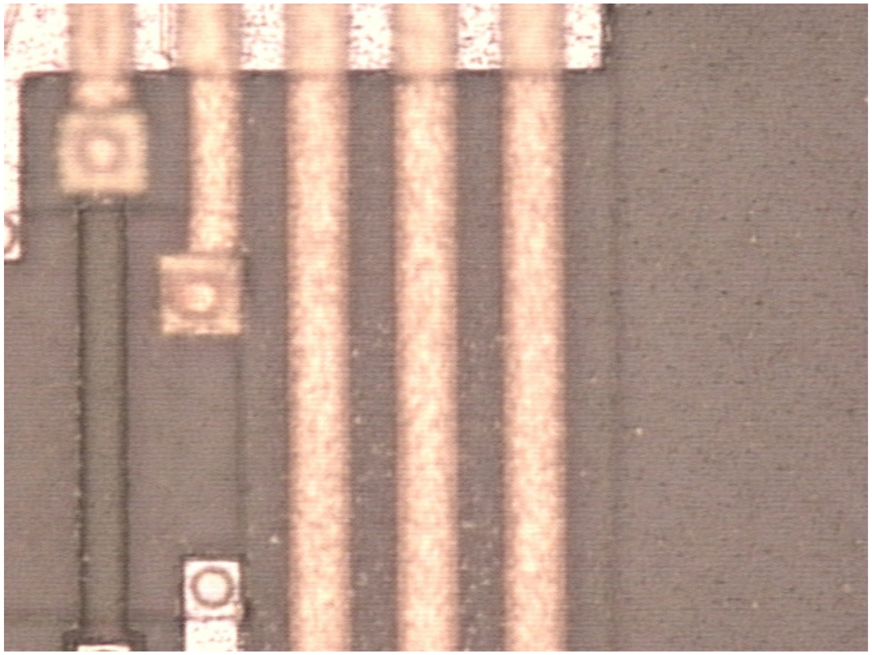
LAM4600 ANISOTROPIC ALUMINUM ETCH

Step	**1**	**2**	**3**	**4**	**5**
Pressure	100	100	100	100	0
RF Top (W)	0	0	0	0	0
RF Bottom	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
N2	13	13	20	25	25
BCl	50	50	25	25	0
Cl2	10	10	30	23	0
Ar	0	0	0	0	0
CFORM	8	8	8	8	8
Complete	Stabl	Time	Endpoint	Oetch	Time
Time (s)	15	8	180	10%	15

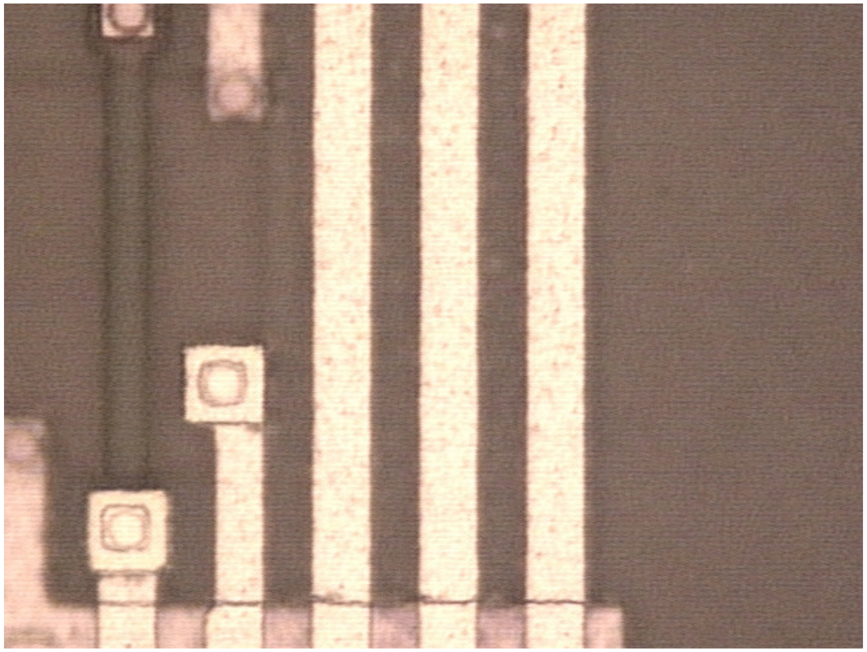
Channel	B
Delay	130
Normalize	10 s
Norm Val	5670
Trigger	105%
Slope	+

Fuller, December 2009

RESULTS FROM ALUMINUM PLASMA ETCH



Photoresist on Metal Two

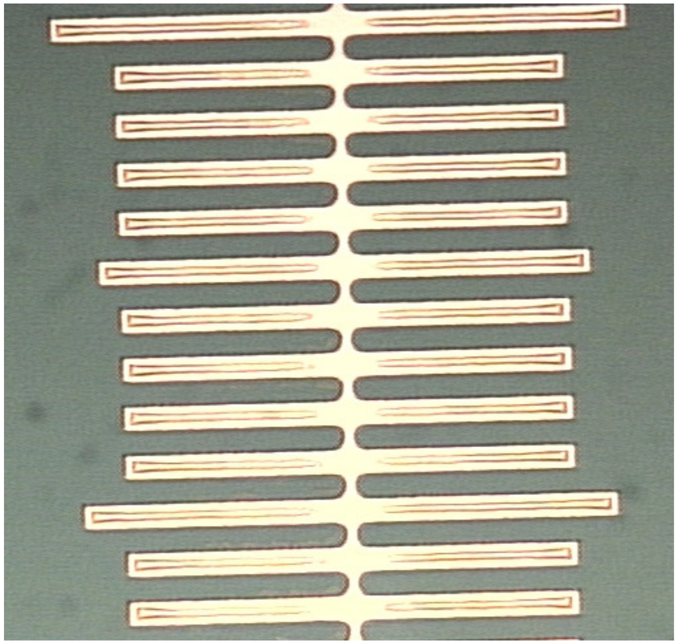


Photoresist Removed

RESIST REMOVAL POST CHLORINE RIE ALUMINUM ETCH

Problem: Photoresist is hardened (and chemically changed) in Chlorine RIE during Aluminum etch and ashing is ineffective in removing the resist.

Solution: Use a Solvent based photoresist stripper process. (similar to Baselinc CMOS process at U of California at Berkeley)

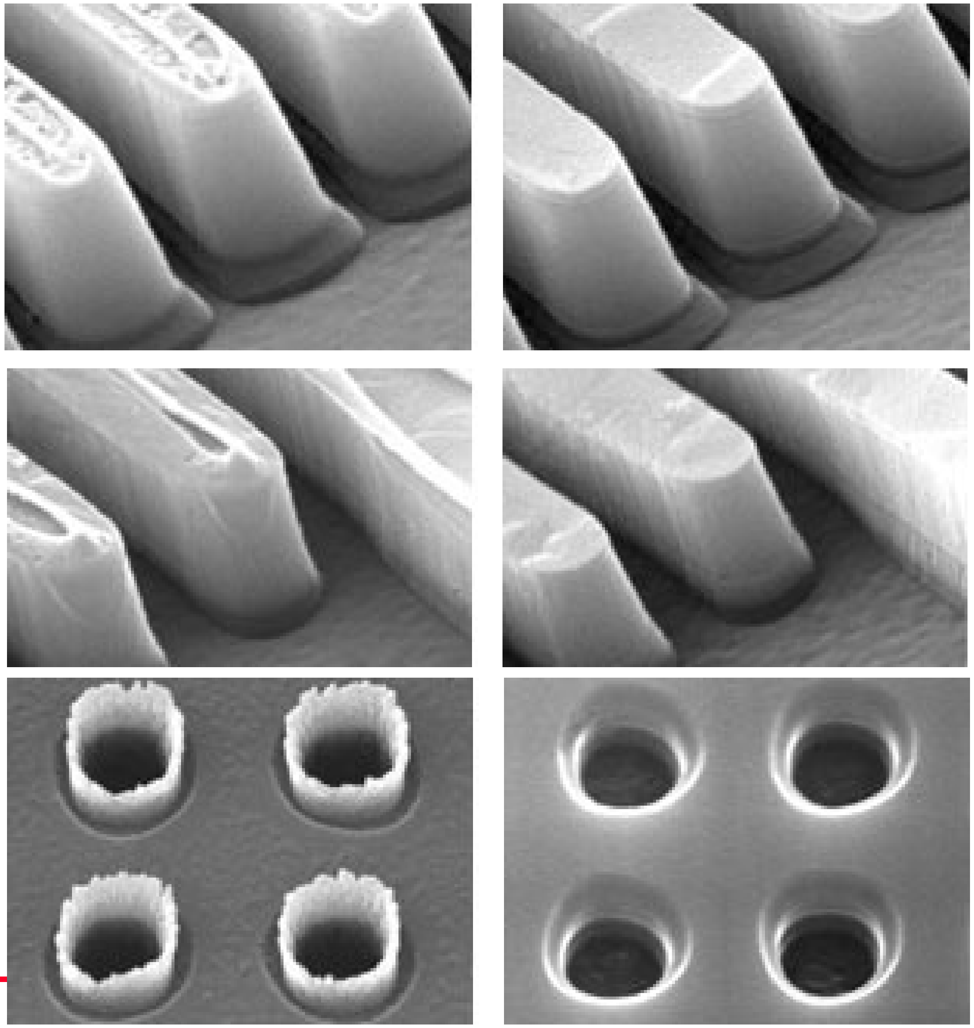


Picture of aluminum wafers post chlorine RIE and after ashing. Note resist remaining on aluminum. Even very long ashing (60 min.) does not remove residue.

Germain Fenger

MORE PICTURES OF RESIST SCUM PROBLEM

Pictures on left show resist residue after ashing. Pictures on right show effectiveness of ACT 935 solvent strip process.



From: [ACT-CMI Data Sheet]

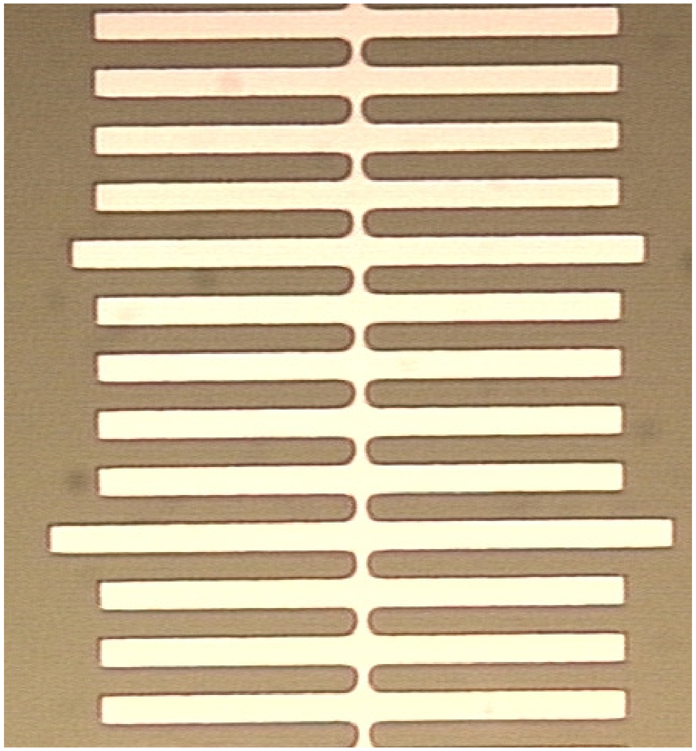
RESIST REMOVAL AFTER PE4600 PLASMA ETCH

Obserations:

A solvent based photoresist stripper followed by a plasma ash is effective at removing Chlorine “burned resist”

Recommendations:

PRS2000 at 90C for 10 min
Rinse 5 min. / SRD
Follow up with 6” Factory ash on the Branson Asher

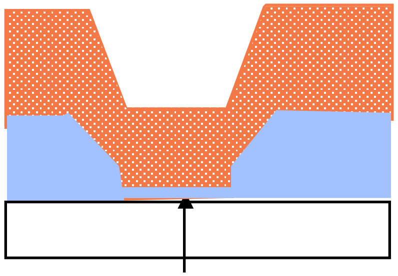


No photoresist was found on wafers

Germain Fenger

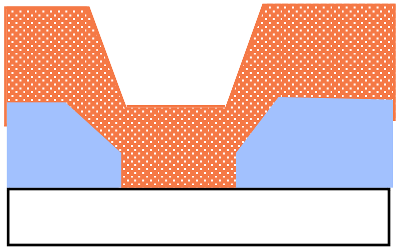
SINTERING 425 °C, N2/H2

Before Sinter

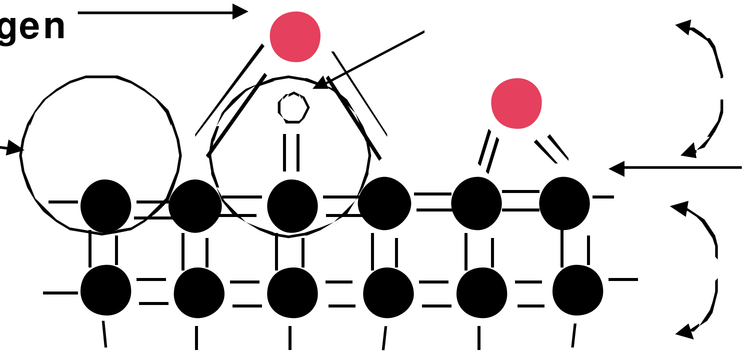


Native Oxide

After Sinter



Reduce Contact Resistance



Hydrogen, neutral region

Oxygen

+ charge region (silicon atom that lost an electron)

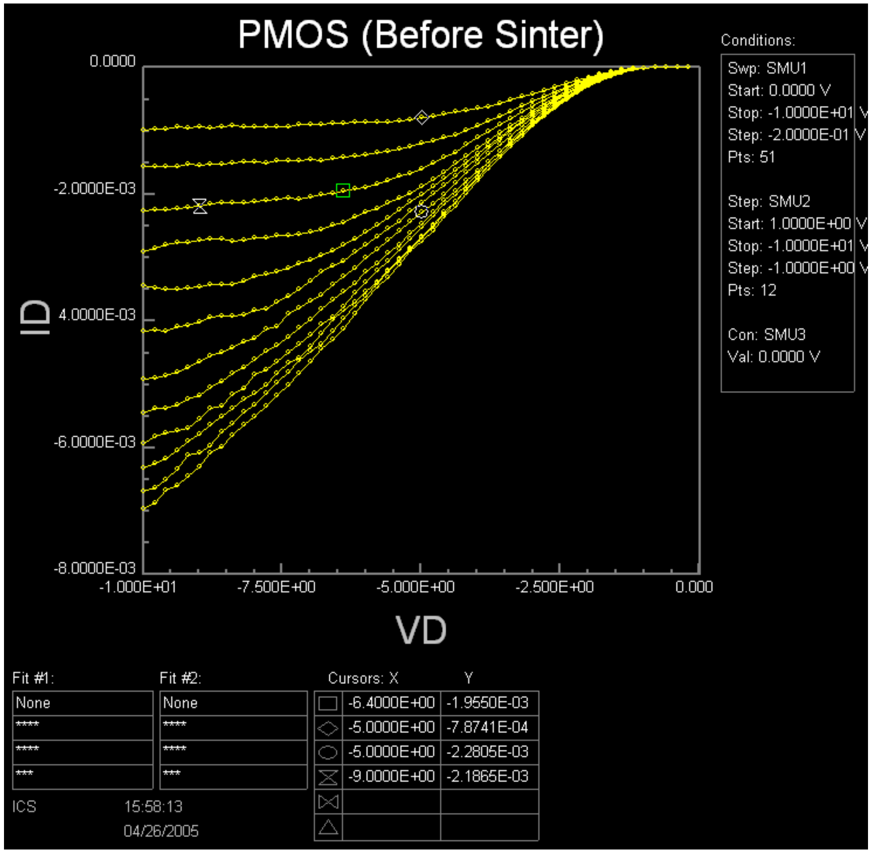
Silicon DiOxide

Interface

Silicon Crystal

Reduce Surface States

EFFECT OF SINTER ON IV CHARACTERISTICS



Conditions:

Swp: SMU1
Start: 0.0000 V
Stop: -1.0000E+01 V
Step: -2.0000E-01 V
Pts: 51

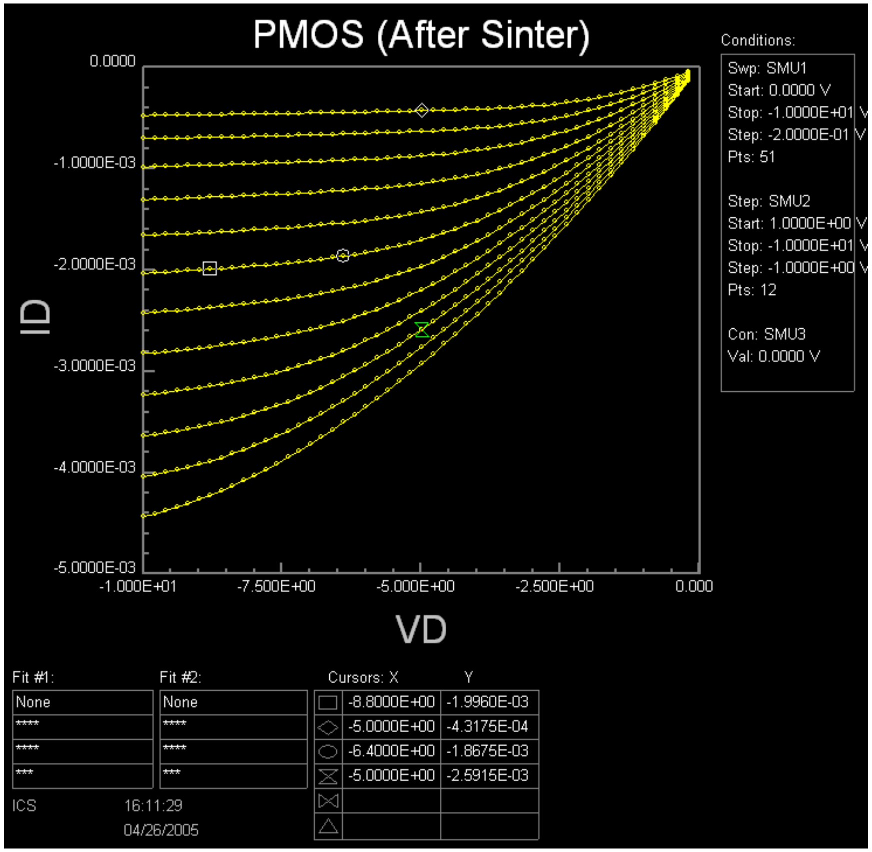
Step: SMU2
Start: 1.0000E+00 V
Stop: -1.0000E+01 V
Step: -1.0000E+00 V
Pts: 12

Con: SMU3
Val: 0.0000 V

Fit #1:	Fit #2:
None	None
****	****
****	****
***	***

Cursors:	X	Y
□	-6.4000E+00	-1.9550E-03
◇	-5.0000E+00	-7.8741E-04
○	-5.0000E+00	-2.2805E-03
⧖	-9.0000E+00	-2.1865E-03
⋈		
△		

ICS 15:58:13
04/26/2005



Conditions:

Swp: SMU1
Start: 0.0000 V
Stop: -1.0000E+01 V
Step: -2.0000E-01 V
Pts: 51

Step: SMU2
Start: 1.0000E+00 V
Stop: -1.0000E+01 V
Step: -1.0000E+00 V
Pts: 12

Con: SMU3
Val: 0.0000 V

Fit #1:	Fit #2:
None	None
****	****
****	****
***	***

Cursors:	X	Y
□	-8.8000E+00	-1.9960E-03
◇	-5.0000E+00	-4.3175E-04
○	-6.4000E+00	-1.8675E-03
⧖	-5.0000E+00	-2.5915E-03
⋈		
△		

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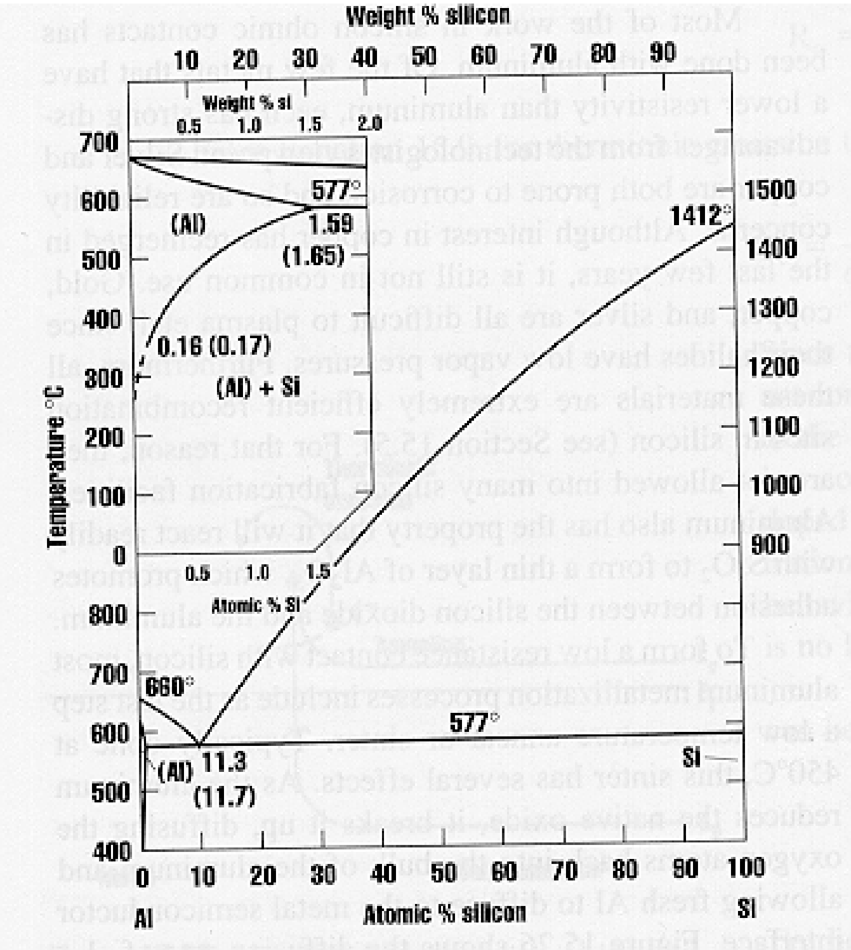
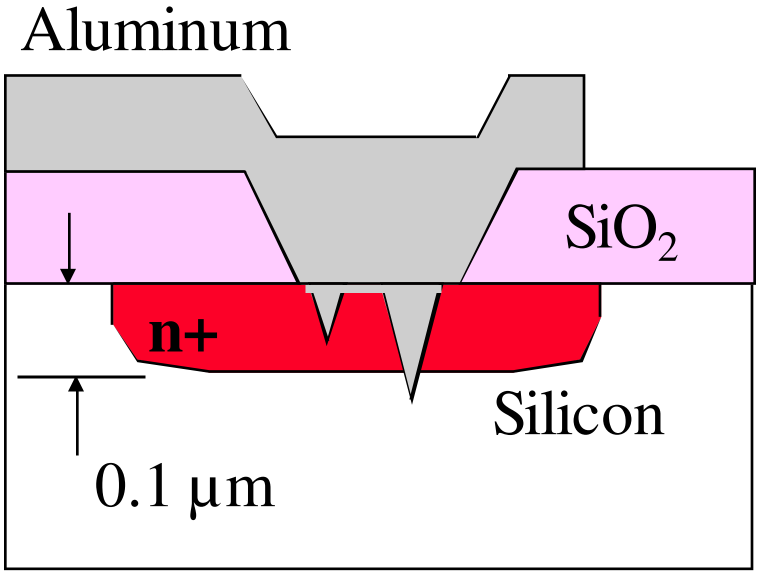
04/26/2005

SINTERING, SPIKING, EUTECTIC



Aluminum/Silicon

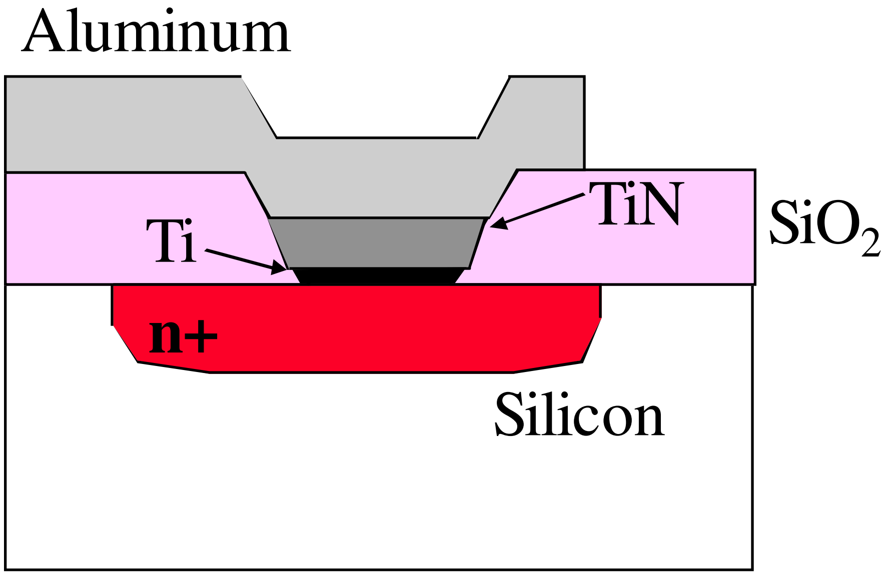
Eutectic point 577 °C



Spiking

DIFFUSION BARRIERS

Al(1% Si)/TiN/Ti/Si



Passivation
6000 Å Al 1% Si
800 Å TiN
300 Å Ti

TITANIUM SILICIDE FORMATION (TiSi2)

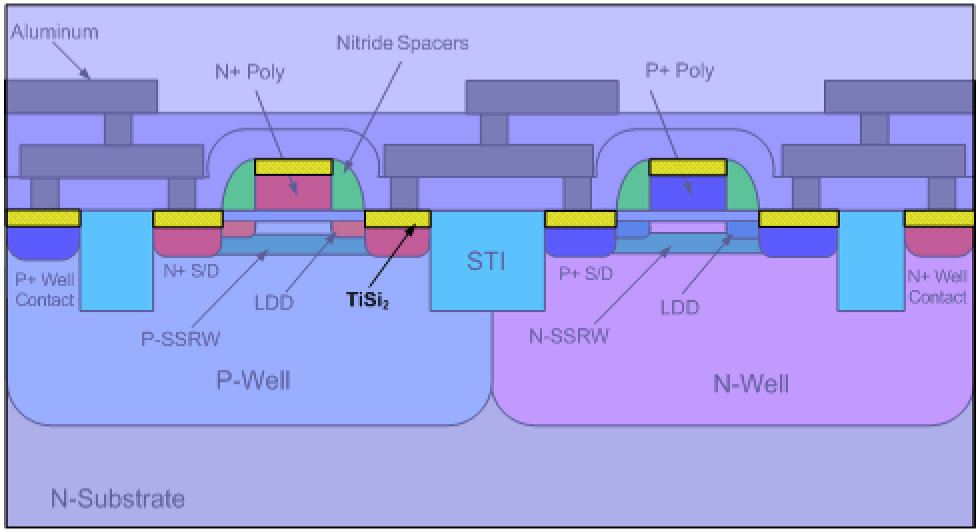
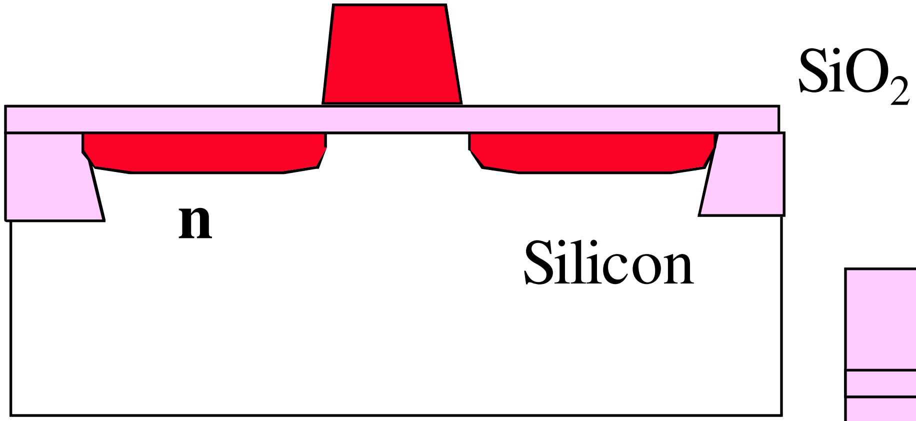


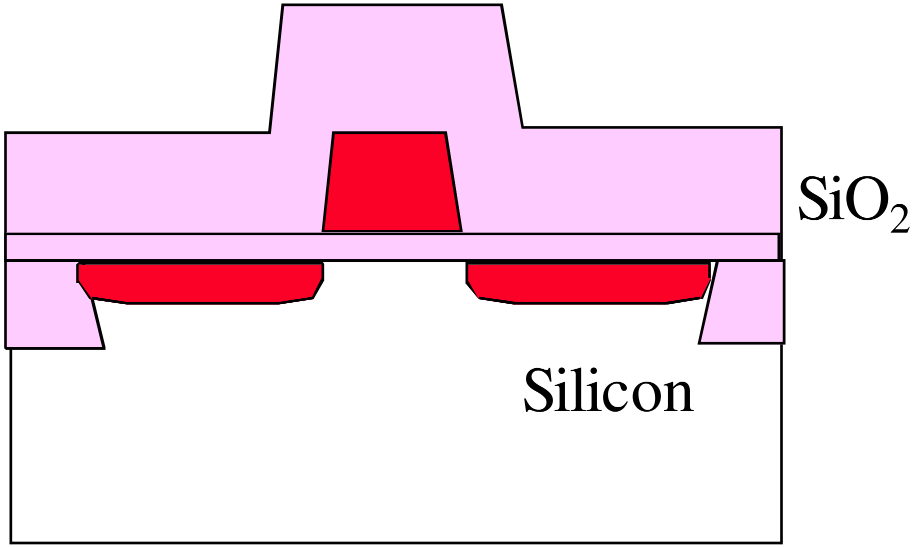
Figure 30: Titanium Silicide Formation

To reduce sheet resistance of source/drain contact regions from 50 – 75 Ω/sq to 4 Ω/sq To give high drive current for fast switching speeds. Titanium Silicide was widely used at the 0.25 µm node

SELF ALIGNED SILICIDE FORMATION

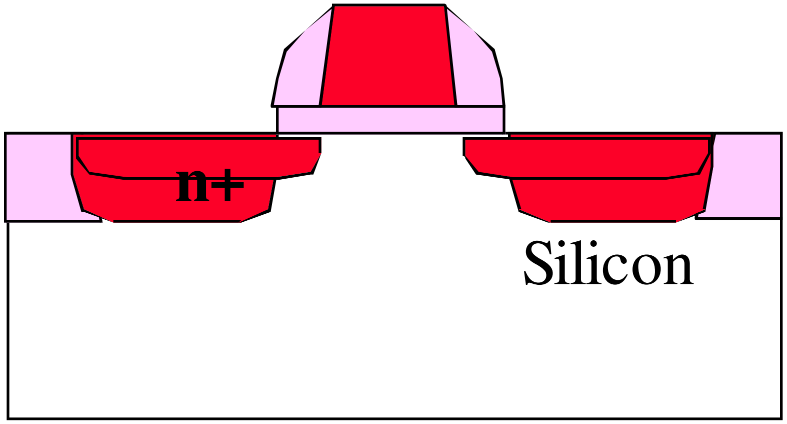


Etch poly gate and implant low doped drain.

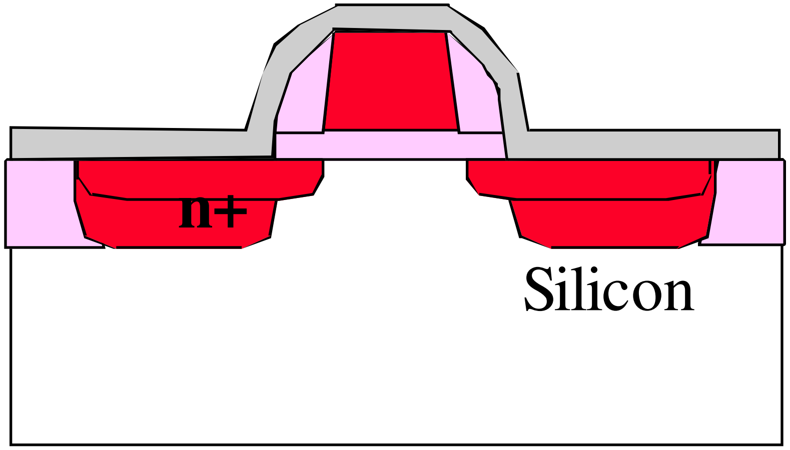


LPCVD oxide

SELF ALIGNED SILICIDE FORMATION

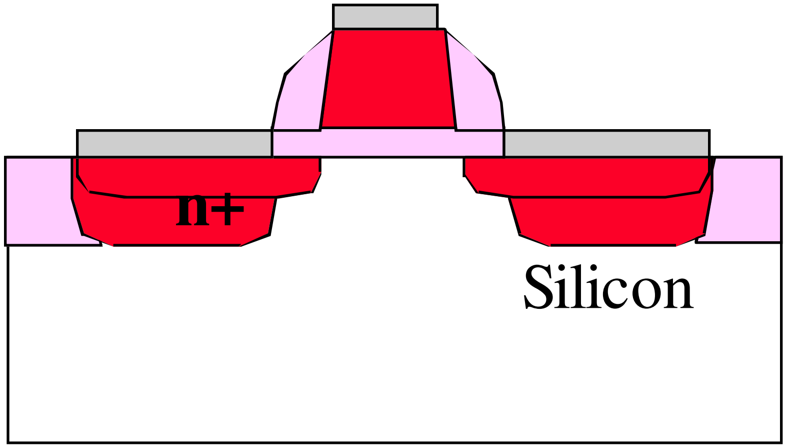


RIE oxide leaving side wall spacers and implant n+ D/S



Deposit Titanium and react it (RTP) with silicon forming Ti silicide (Ti does not react with SiO2)

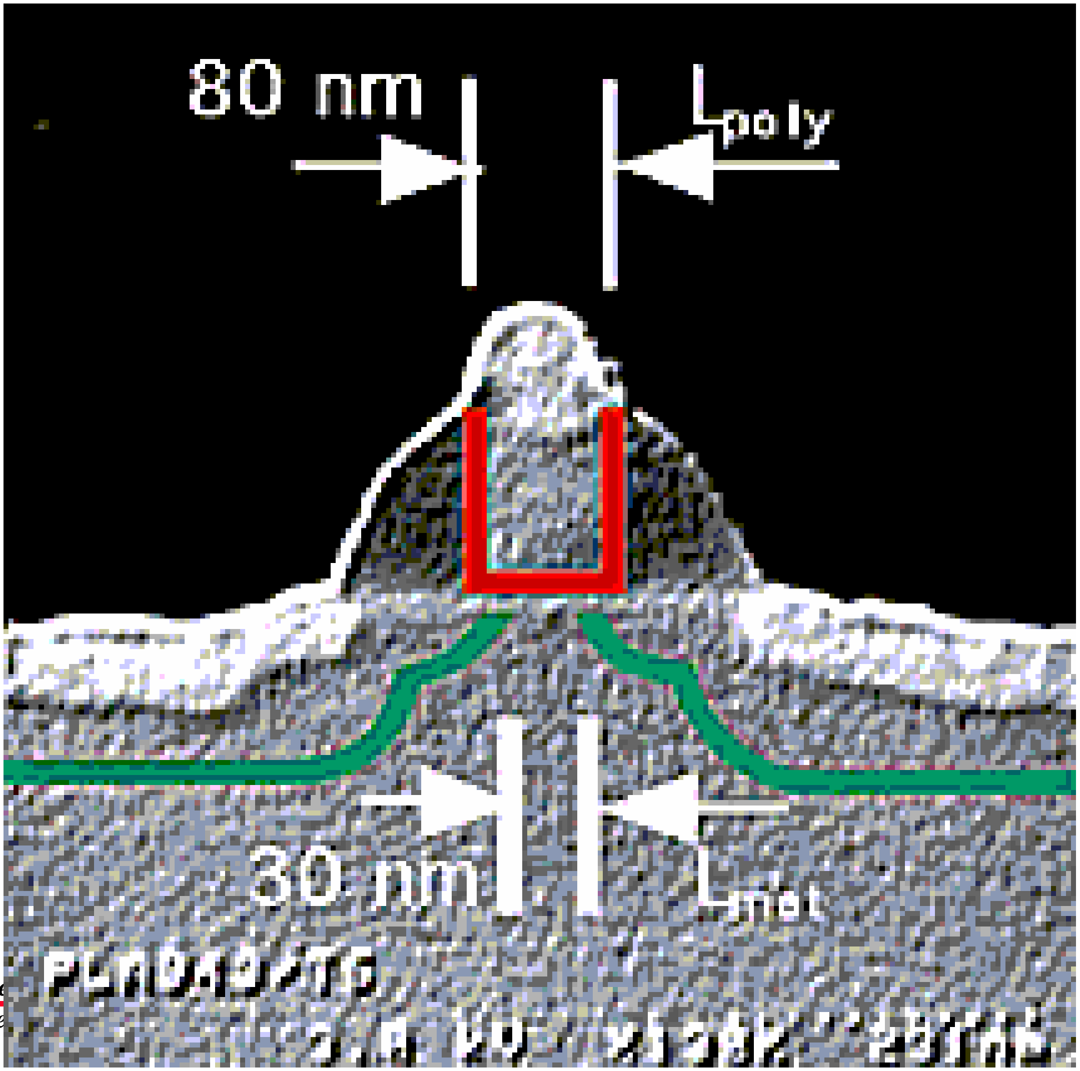
SELF ALIGNED SILICIDE FORMATION



Etch off Titanium leaving self aligned silicide called (salicide)

SILICIDE FORMATION

IMEC Meeting
December 1999



TITANIUM SILICIDE FORMATION (TiSi2)

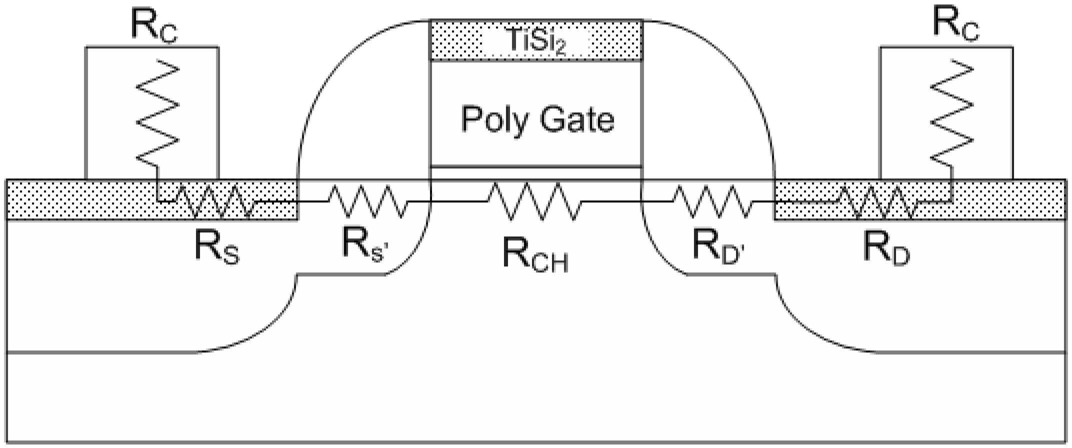


Figure 31: Transistor Cross section with Parasitic Resistances [14]

$$R_{TOTAL} = R_{CHANNEL} + R_{PARASITIC}$$

$$R_{PARASITIC} = R_{EXTENSION} + R_{EXTRINSIC}$$

$$R_{EXTENSION} = R_S' + R_D'$$

$$R_{EXTRINSIC} = R_S + R_D + 2R_C$$

$$R_S' \times W = R_{SLDD} \times L_{spacer}$$

$$R_D' \times W = R_{SLDD} \times L_{spacer}$$

$$R_S \times W = R_{SSILICIDE} \times L$$

$$R_D \times W = R_{SSILICIDE} \times L$$

$$R_C \times W = \frac{\rho_C}{L} \quad , \rho_C = 2 \times 10^{-9}\,\Omega \times cm^2$$

TITANIUM SILICIDE FORMATION (TiSi2)

Require < 10% reduction in drive current due to $R_{PARASITIC}$

Sample calculation shown in Table 7, assume:

$R_{S\text{-}LDD}$ = 400 Ω/sq
L_{SPACER} = 0.25 µm
$R_{S\text{-}Silcide}$ = 4 Ω/sq
$L_{SILICIDE}$ = 0.75 µm

$R_{EXTENSION} \times W$ (Ω x µm)	$R_{EXTRINSIC} \times W$ (Ω x µm)	$R_{PARASITIC} \times W$ (Ω x µm)	$R_{SAT} \times W$ (Ω x µm)	$\dfrac{R_{PARASITIC} \times W}{R_{SAT} \times W}$
200	7	207	4108	5.1 %

All Resistances are calculated for a nominal 1 µm width

As width is increased, the total resistance components will decrease but the ratio for drive current reduction will remain the same

Drive current is only reduced by ~5% including integration of silicide

TITANIUM SILICIDE FORMATION (TiSi2)

Silicide	Thin Film Resistivity (µΩ-cm)	Sintering Temp (°C)	Stable on Si up to (°C)	Reaction with Al at (°C)	nm of Si consumed per nm of metal	nm of resulting silicide per nm of metal
$TiSi_2$ (C54)	13-16	700-900	~900	450	2.27	2.51
$TiSi_2$ (C49)	60-70	500-700			2.27	2.51

45 nm of Si is consumed by 20 nm of Ti to produce 50 nm of $TiSi_2$ in C49 phase

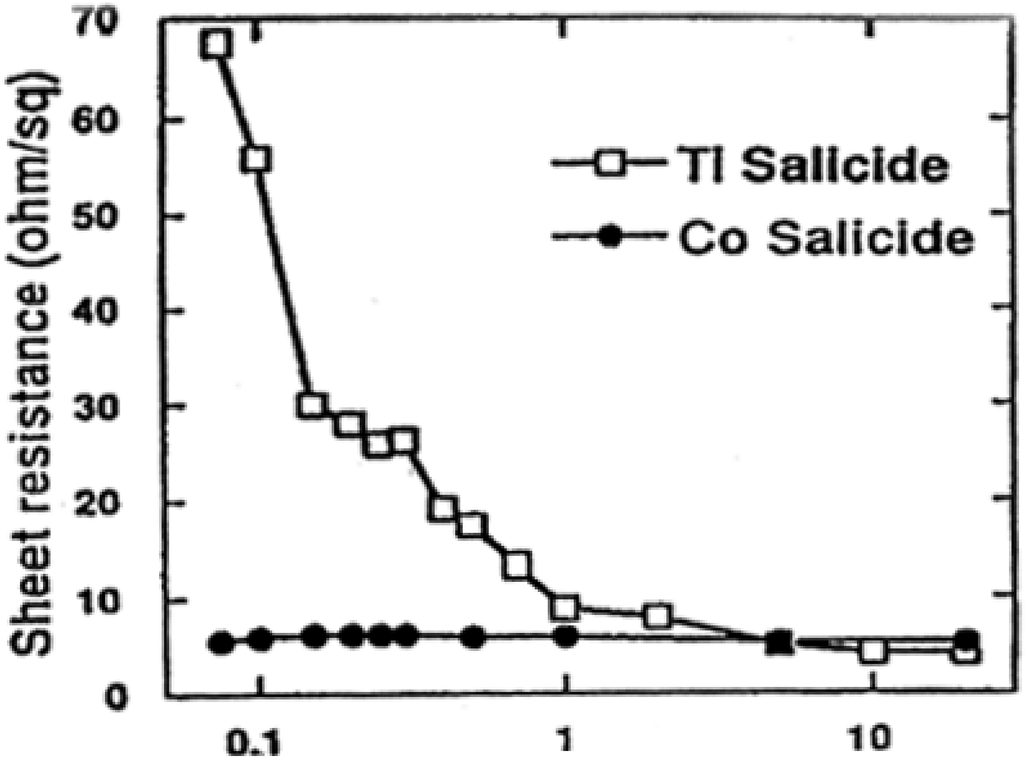
The C49 phase is a higher resistivity phase created after a 500-700°C rapid thermal step

The un-reacted Ti is removed by wet chemistry and a 2nd thermal step is performed at 700-900°C to form lower resistivity C54 phase

50 nm of $TiSi_2$ in the C54 phase should yield an $R_s \sim 4\ \Omega/sq$

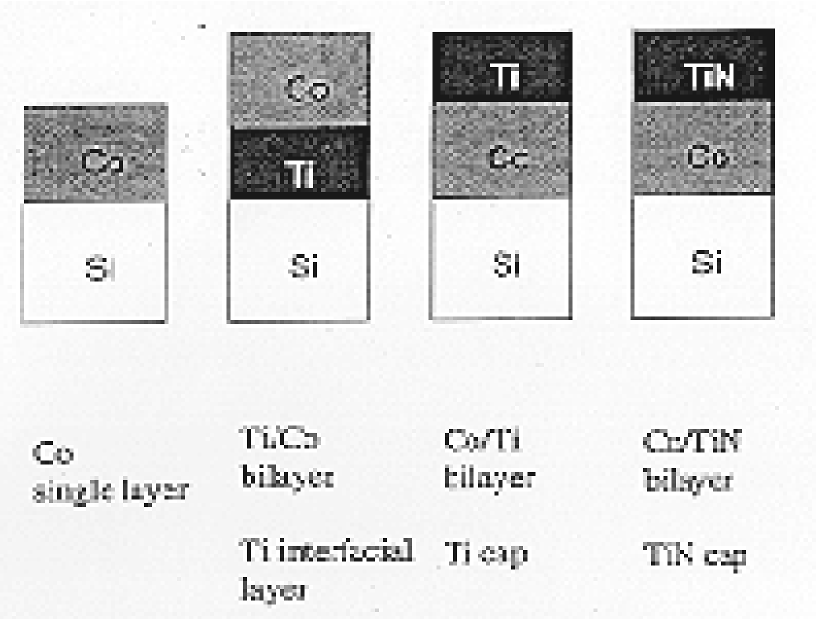
TITANIUM SILICIDE FORMATION (TiSi2)

Titanium Silicide suffers from a narrow line width effect where R_s increases as line width is decreased. This is why the industry transitioned to $CoSi_2$ for sub-0.25 µm CMOS. Intel reports an R_S of 4 Ω/sq for their 0.25 µm CMOS process, although it is not reported if this is for the source/drain regions only, or gate too



COBALT SILICIDE (CoSi2)

$CoSi_2$ is being used commonly for the advanced IC technologies. There are several process choices to be made for the formation of a high yielding and reproducible silicide. The Co/Ti(cap) process is the best for 0.18µm and below.



PROPERTIES OF ALUMINUM CONDUCTORS

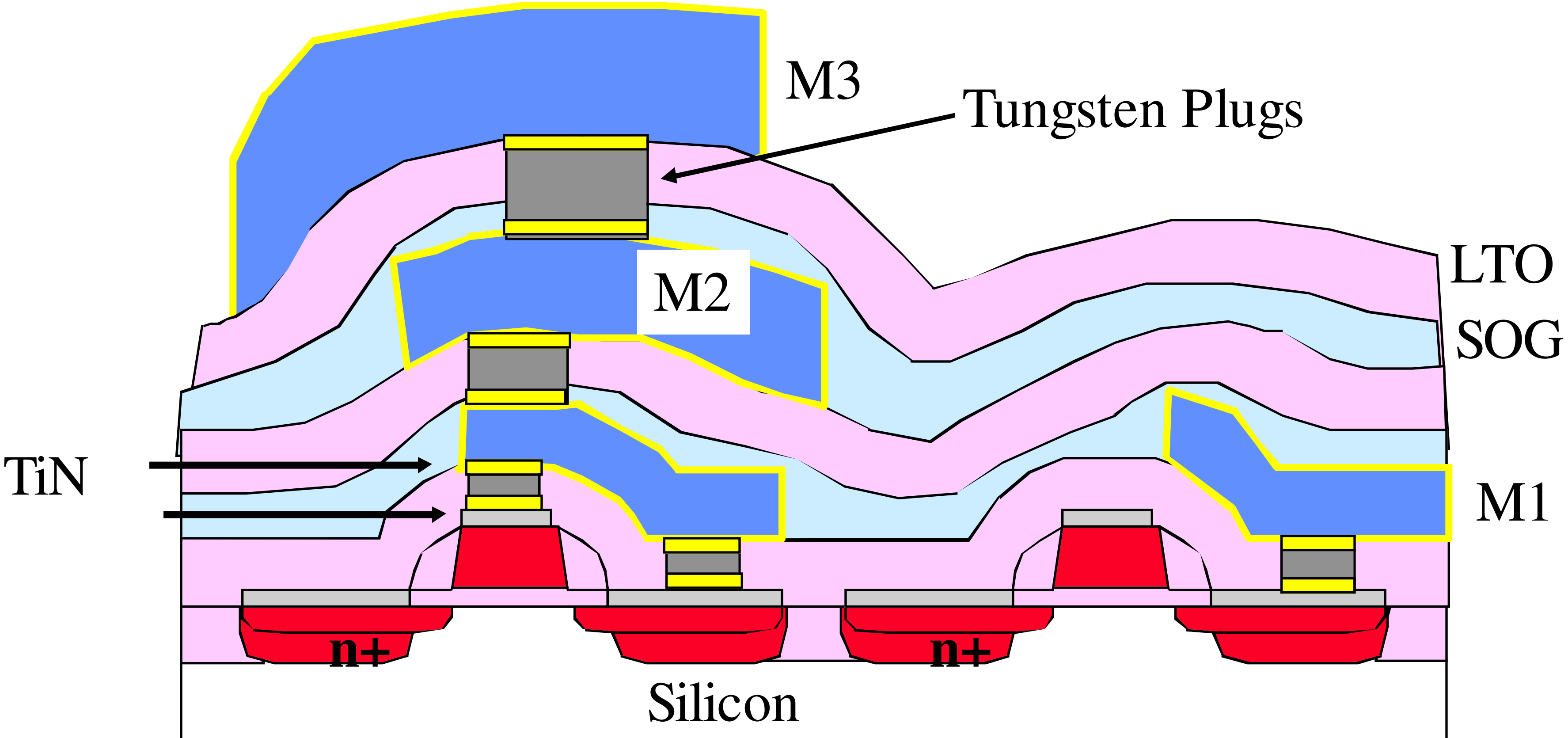
Advantages:

- High Electrical Conductivity, r (bulk) = 2.7 µohm-cm
- Good ohmic Contact to n+ and p+ Silicon (~40 ohms for 0.5µm)
- Easy to Deposit
- Good Adherence to $SiO2$ and Si
- Easy to Pattern
- Easy to Wire Bond To
- Low Cost

Limitations:

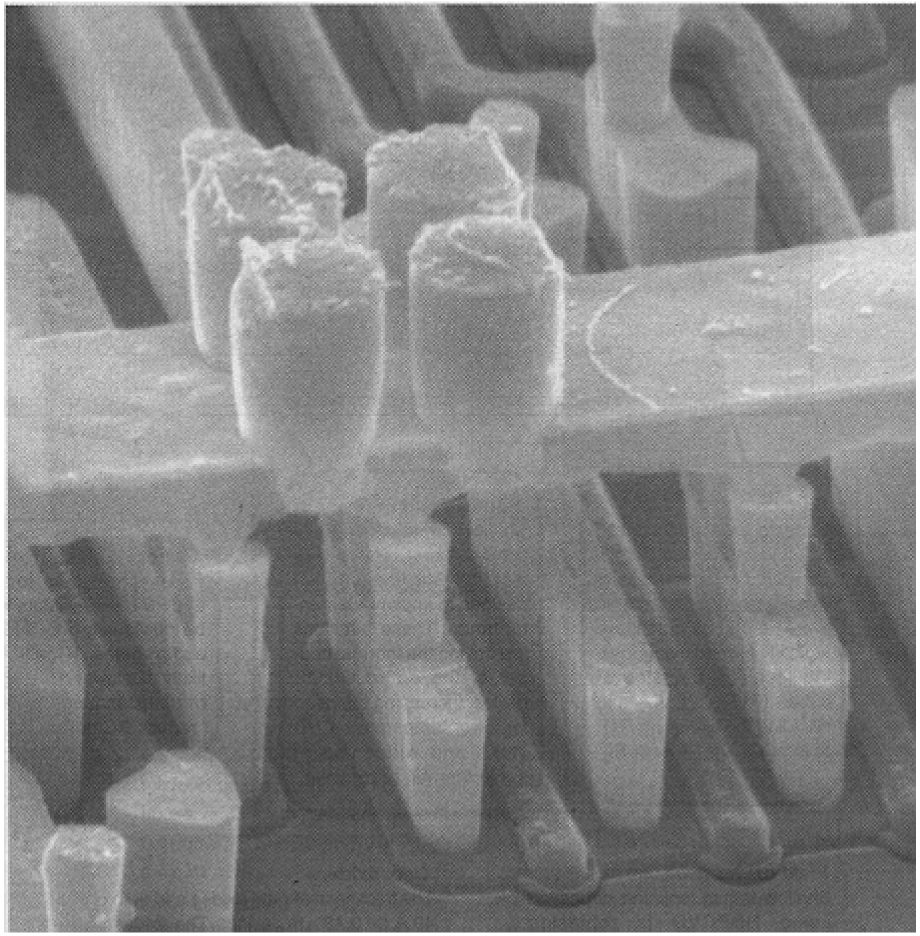
- Low temperature Reaction with Silicon Spiking
- Low Electromigration
- Hillock Growth
- Dry Etching uses Chlorine Chemistry
- No suitable CVD process
- Step Coverage is Poor in High Aspect Ratio Contacts/Vias

0.5 µM THREE LEVEL METAL PROCESS NO CMP

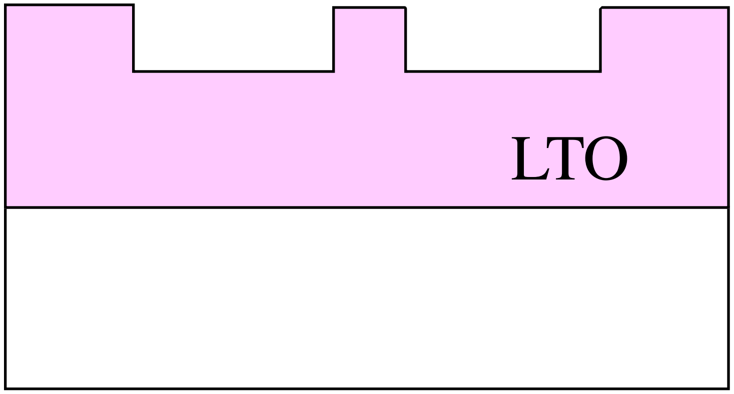


SIX LAYER ALUMINUM, W PLUGS, CMP, DAMASCENE OF LOCAL W INERCONNECT

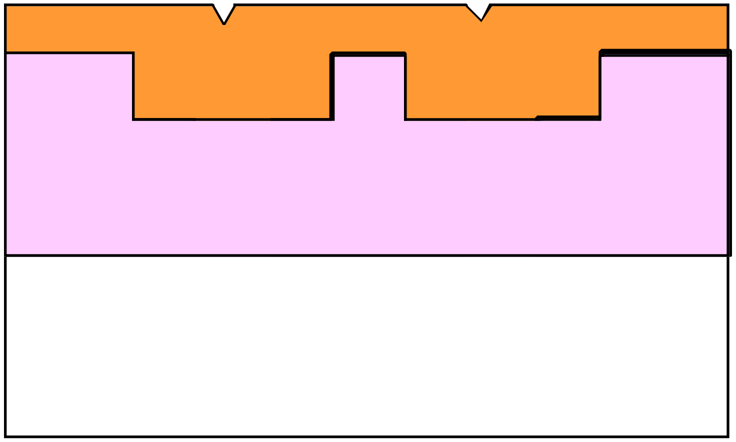
Six levels aluminum interconnect with tungsten plugs, CMP, and damascene of local tungsten interconnect for 0.18 µm gates.



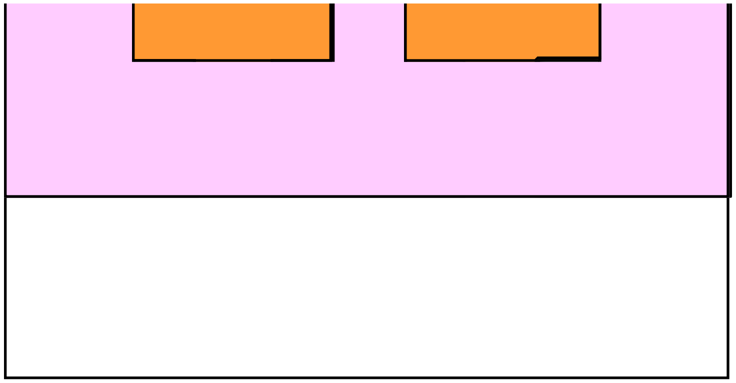
DAMASCENE PROCESS



Pattern Trenches in Oxide

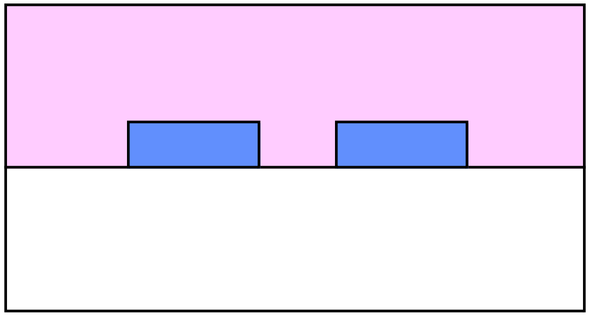


Fill with Copper Metal

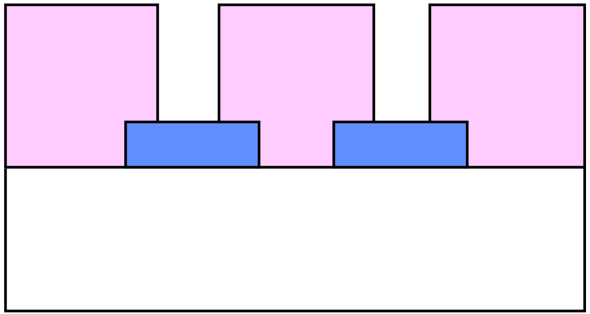


CMP Excess Metal Off

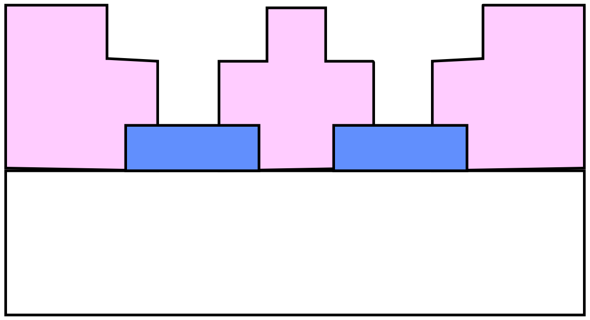
DUAL DAMASCENE PROCESS



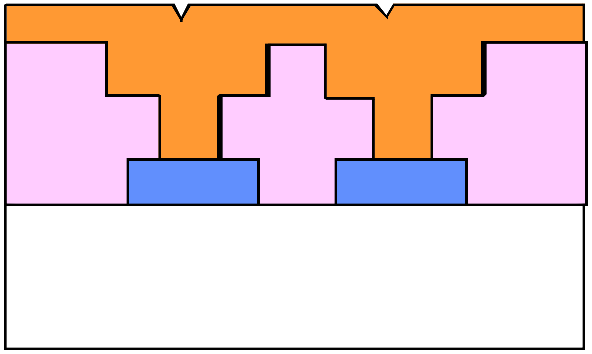
Prior Metal Layer
+ LTO



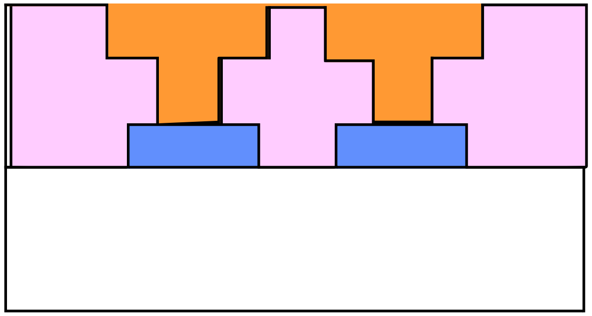
Pattern and Etch
Contact to Prior Metal



Pattern and Etch
Trench for Conductor

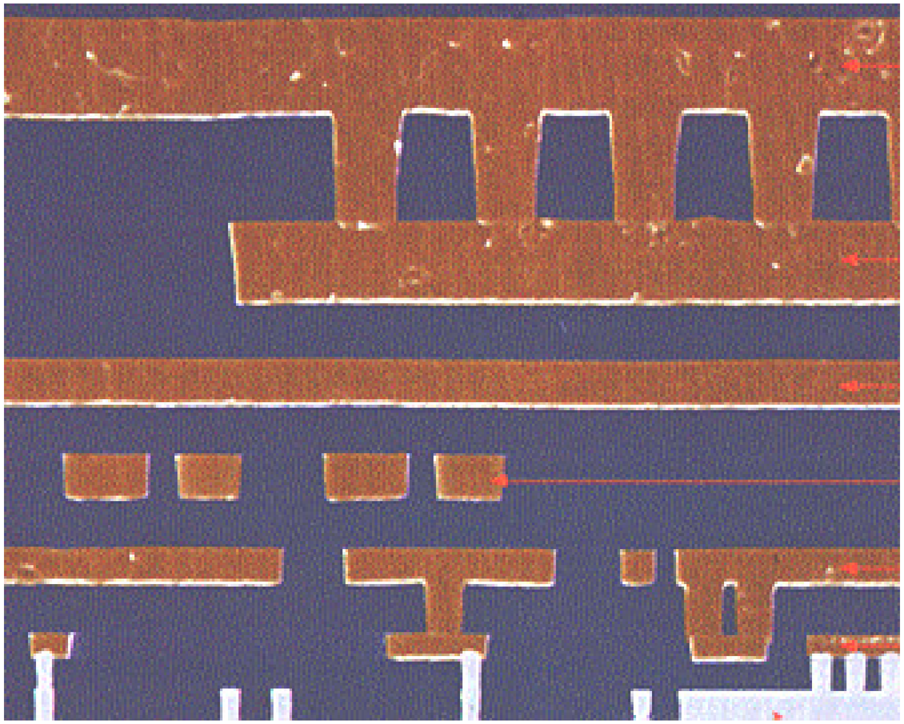


Deposit Copper



CMP excess Metal off

6 LAYER COPPER INTERCONNECT



Copper Layer 6

Copper Layer 5

Copper Layer 4

Copper Layer 3

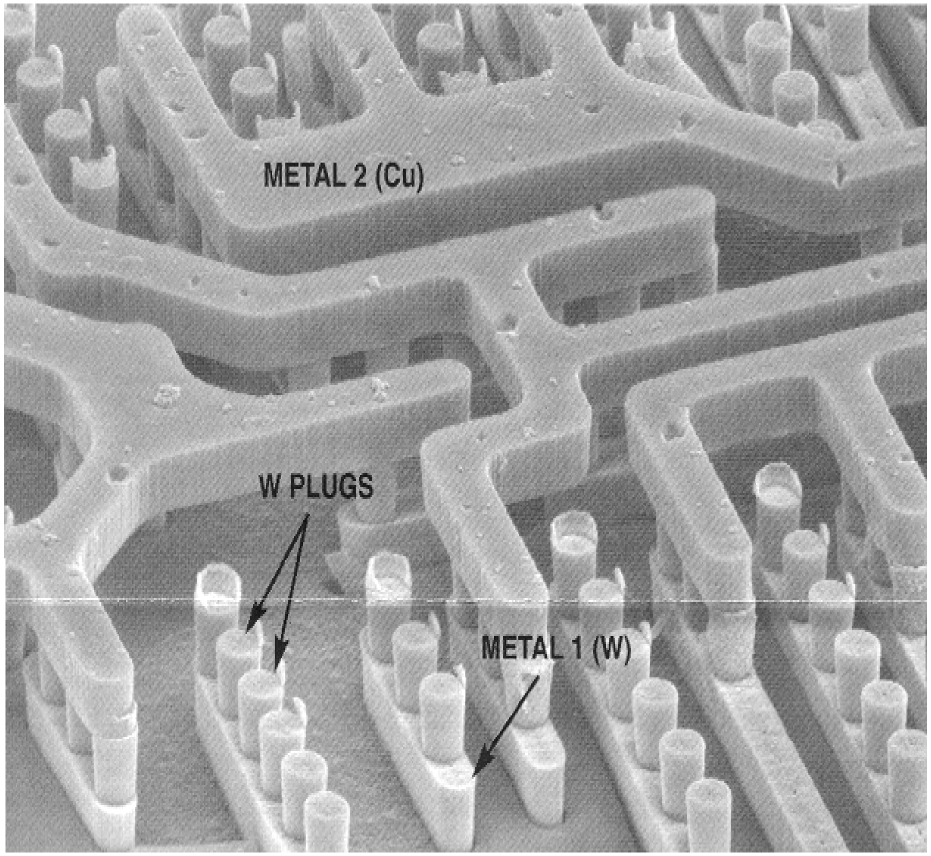
Copper Layer 2

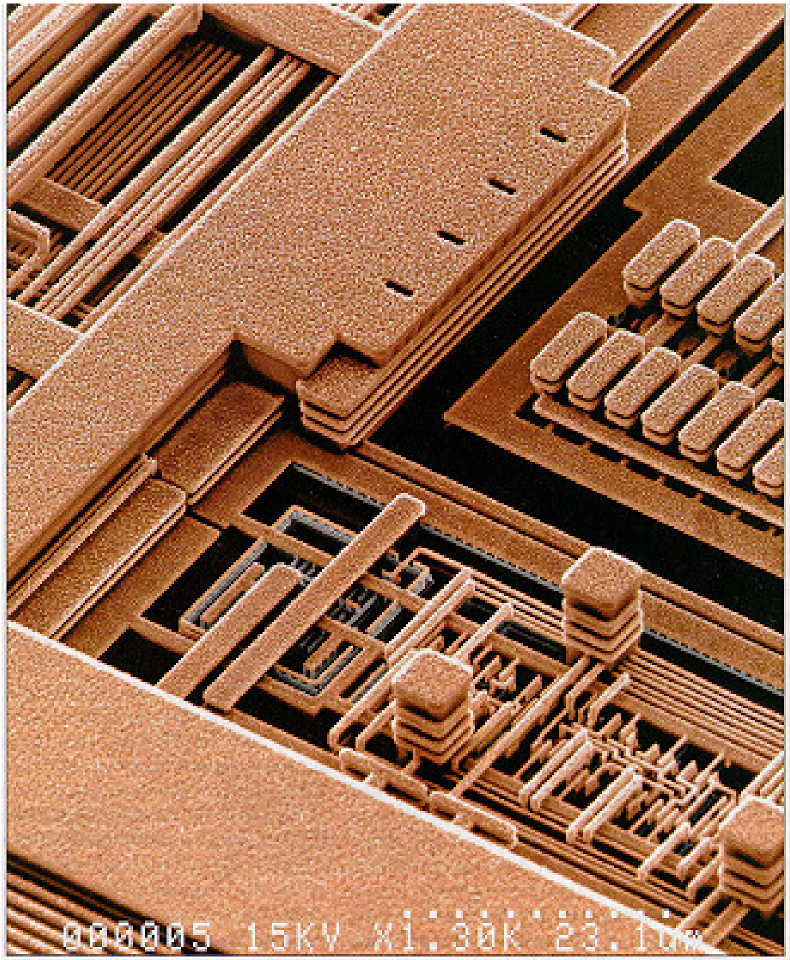
Copper Layer 1

Local tungsten interconnect at 0.2 µm transistor gates

Copper resistivity ~2 µohm cm

COPPER INTERCONNECT





[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].

FINAL PASSIVATION

Funtions of Passivation Layers

Scratch protection for metal
Immunity to shorts by loose conductive particles
Corrosion protection for metal
Reduce susceptibility to electromigration
Provide alkali gettering capability

Materials

SiNxHy by PECVD
SiOxNyHz by PECVD
3 wt % P-PSG by LPCVD, PECVD
BPSG by LPCVD
Polyimides by Spin Coating

REFERENCES

1. Handbook of Thin film Technology, Maissel and Glang, McGraw Hill, 1970.
2. IEEE Spectrum, January 1998.
3. “Copper Goes Mainstream low K to Follow”, Peter Singer, Semiconductor International, November 1997.
4. “CVD TEOS/O3 Development History and Applications”, Kazuo Maeda, Stephen M. Fisher, Solid State Technology, June 1993.
5. “Interconnect metallization for Future Device Generations”, Bruce Roberts, et.al., Solid State Technology, February 1995.