

**ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING**

Testing – Device Problem Analysis

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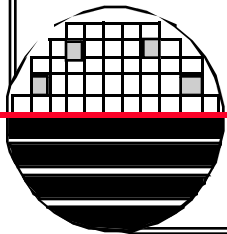
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OUTLINE

Introduction

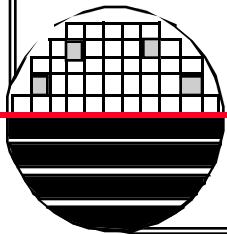
Good Device Characteristics

Various Not So Good Device Characteristics

Discussion of Characteristics

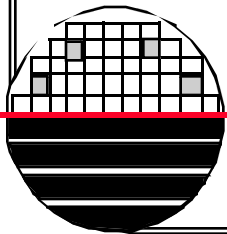
Design Errors

Fabrication Problems

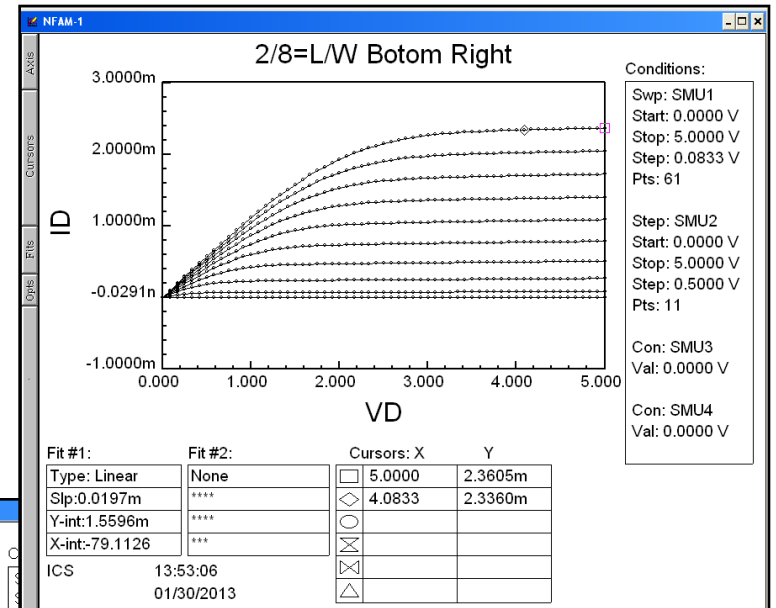
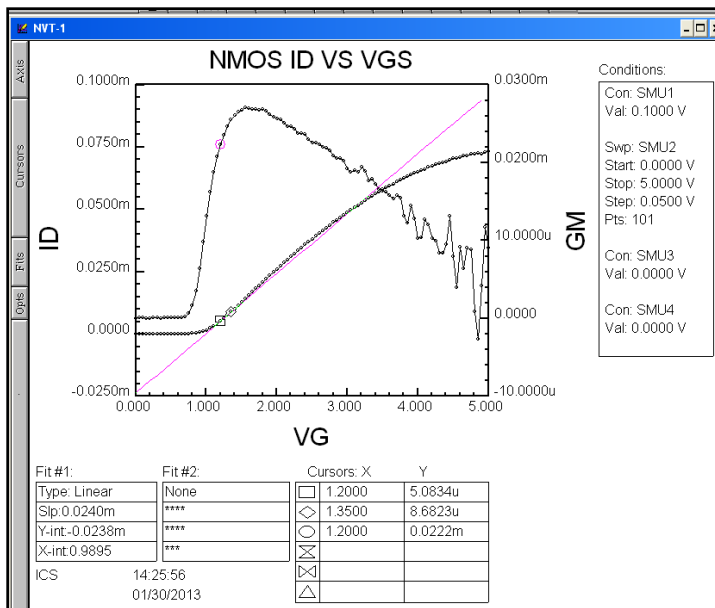


INTRODUCTION

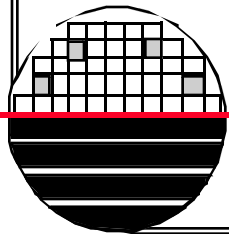
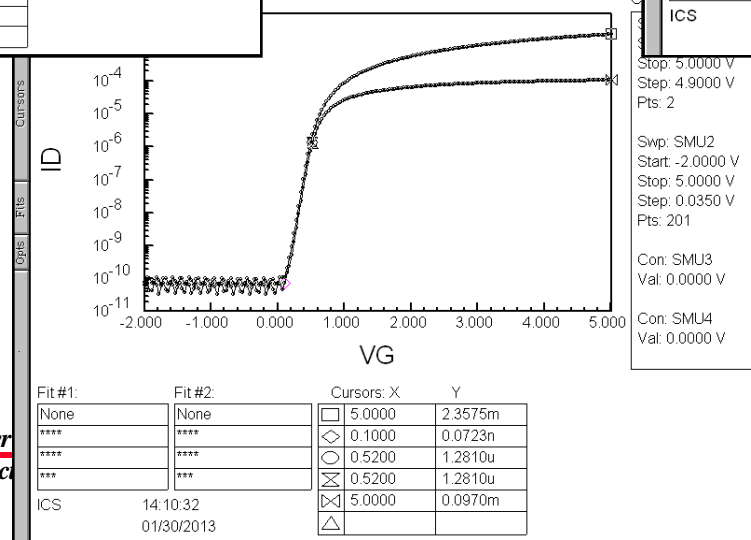
This document is a collection of test results showing problems with various semiconductor devices made in the microelectronics fabrication laboratory. The objective is to provide useful information for identification of the source of problems and to enhance the education of our students.



GOOD NMOS DEVICE CHARACTERISTICS

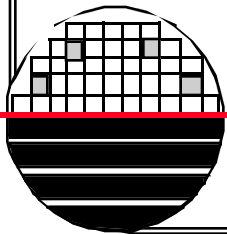
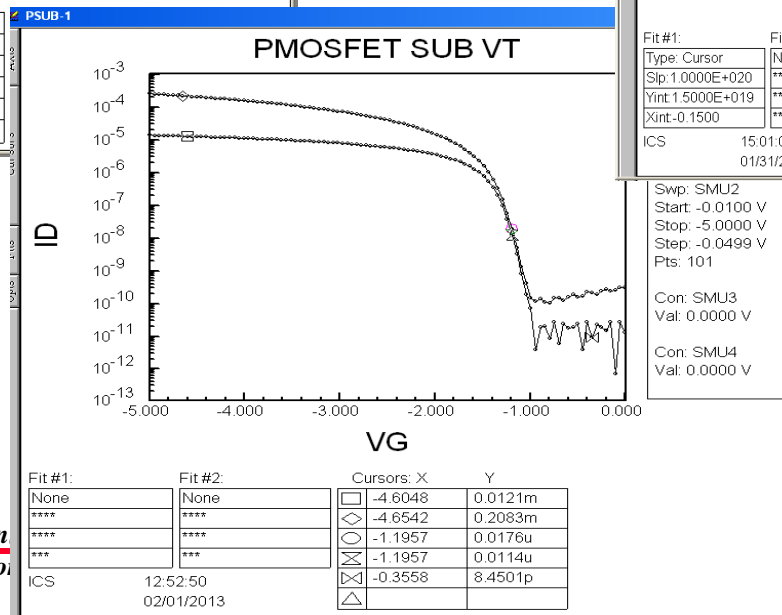
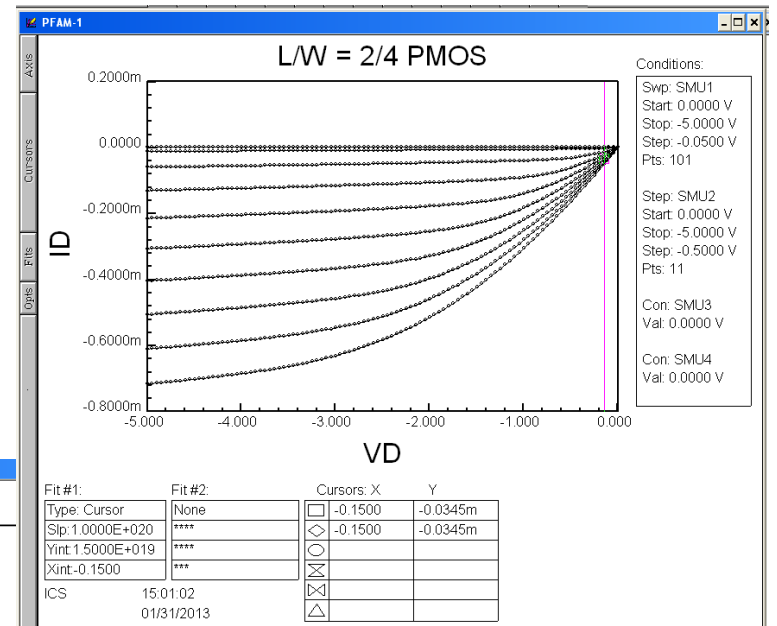
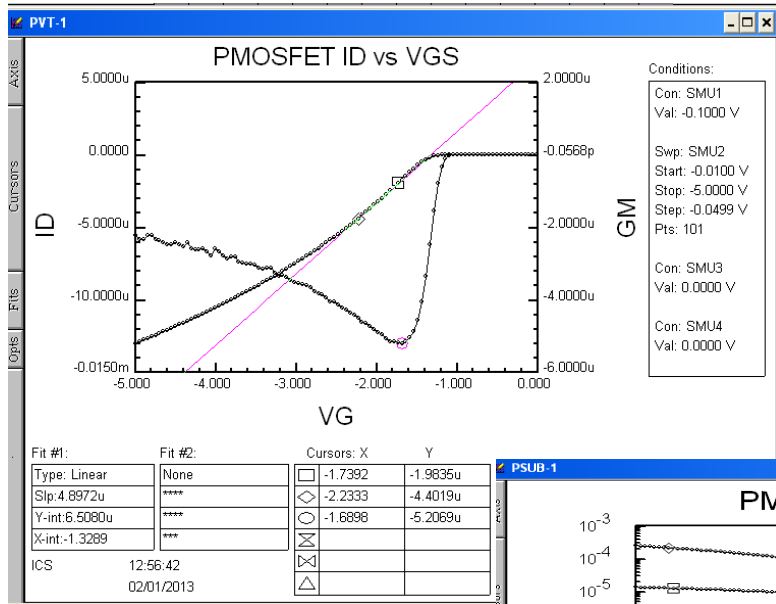


NMOS SUB VT



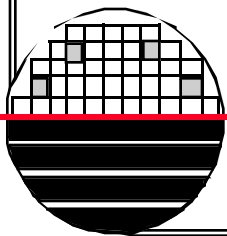
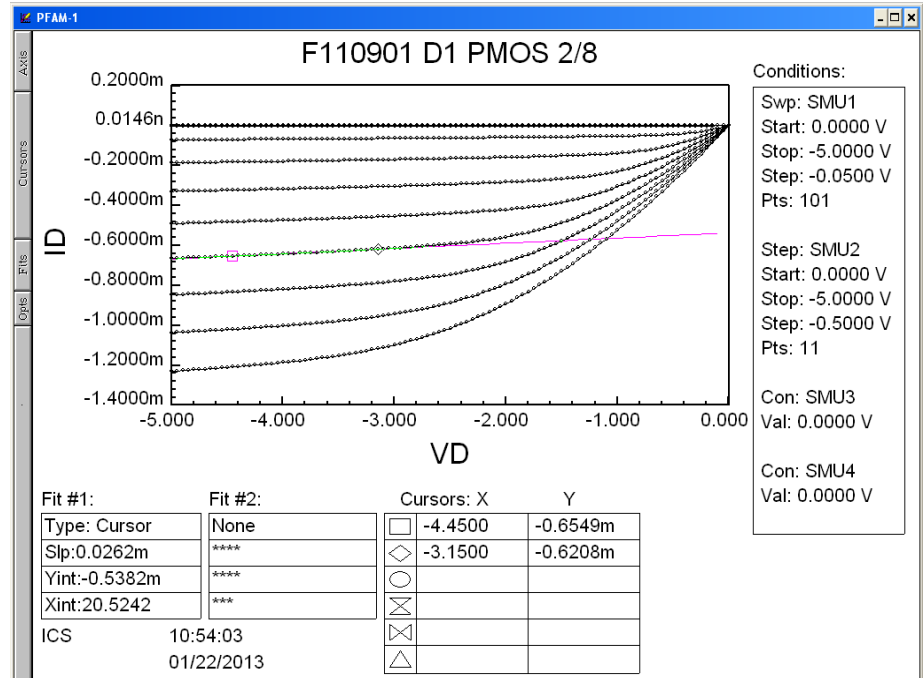
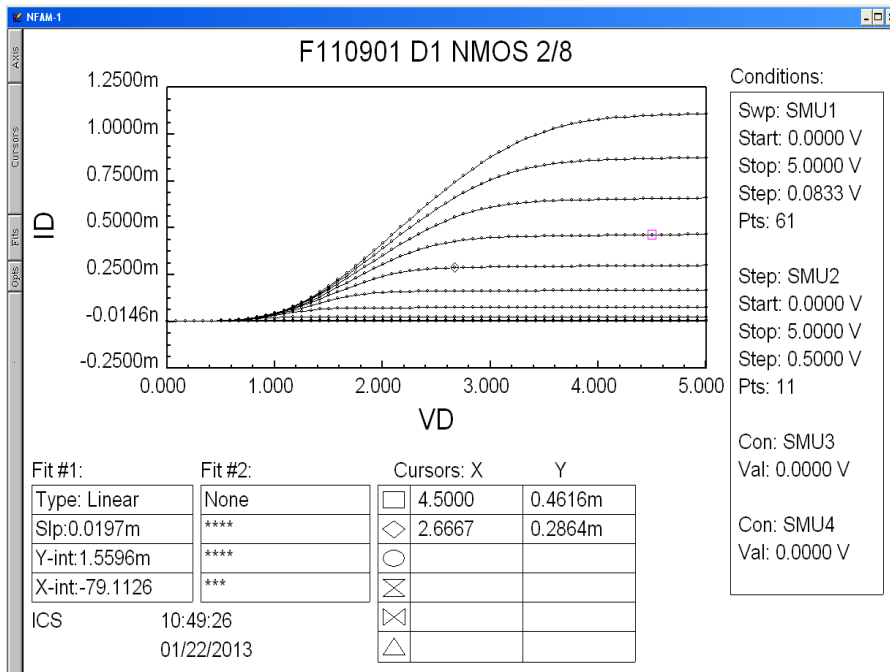
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GOOD PMOS DEVICE CHARACTERISTICS

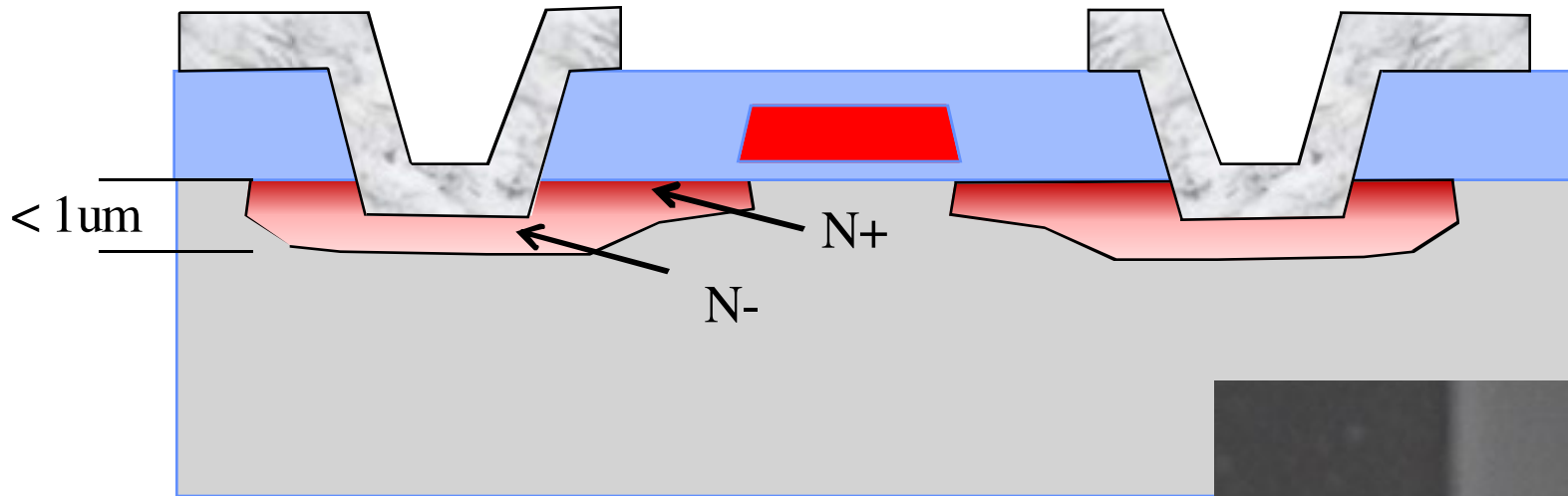


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Microelectro

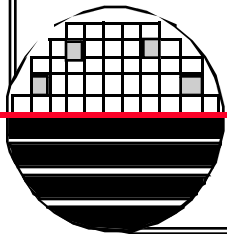
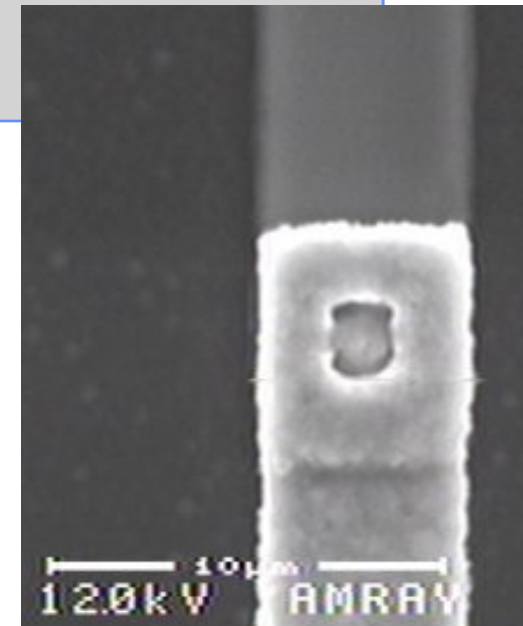
NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN SUB-CMOS PROCESS



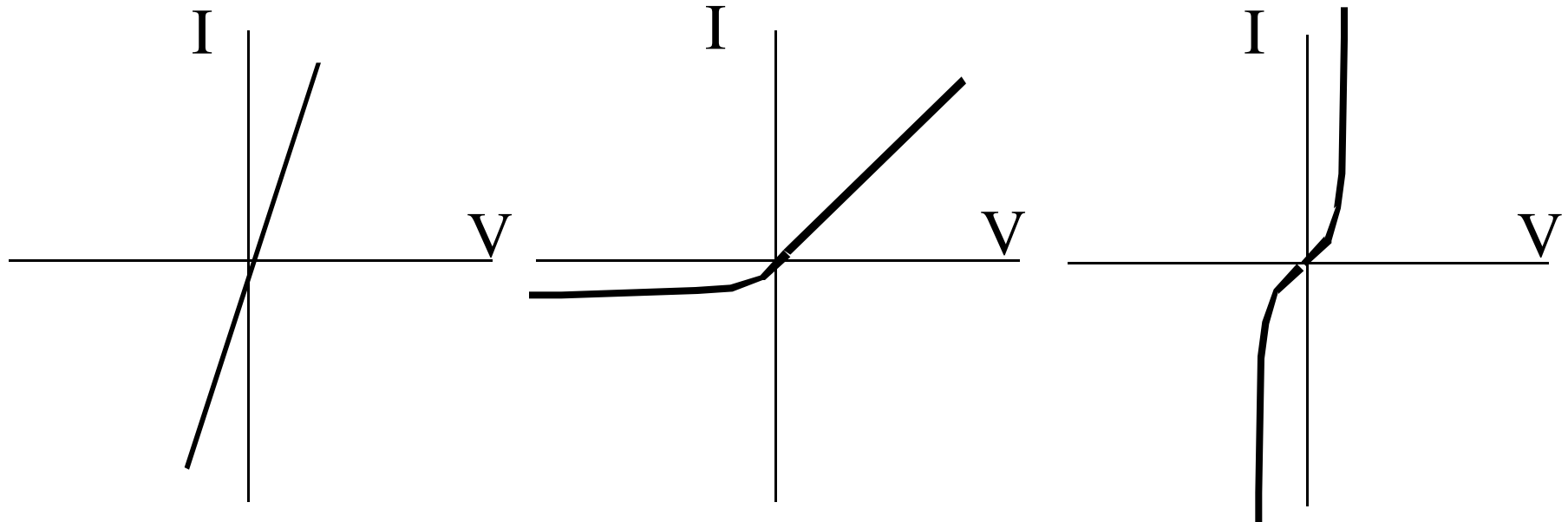
NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN SUB-CMOS PROCESS



Over etched contact cuts makes a non-ohmic (rectifying or Schottky) contact with the lighter doped n-type area of the drain/source. P-type devices have ohmic contacts.



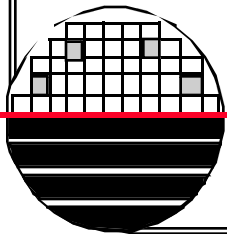
CONTACTS TO SILICON



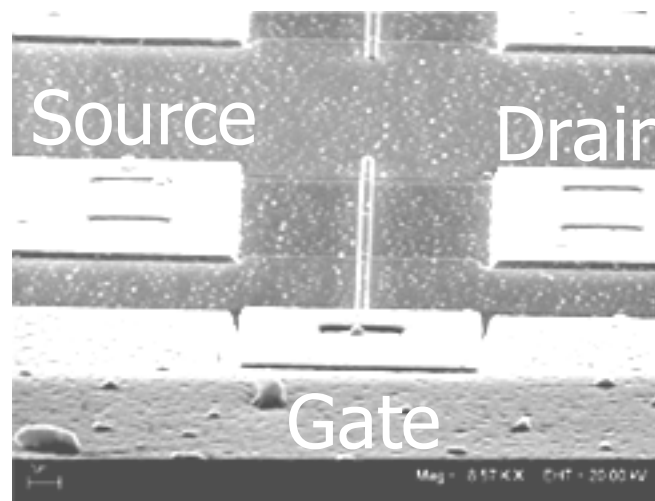
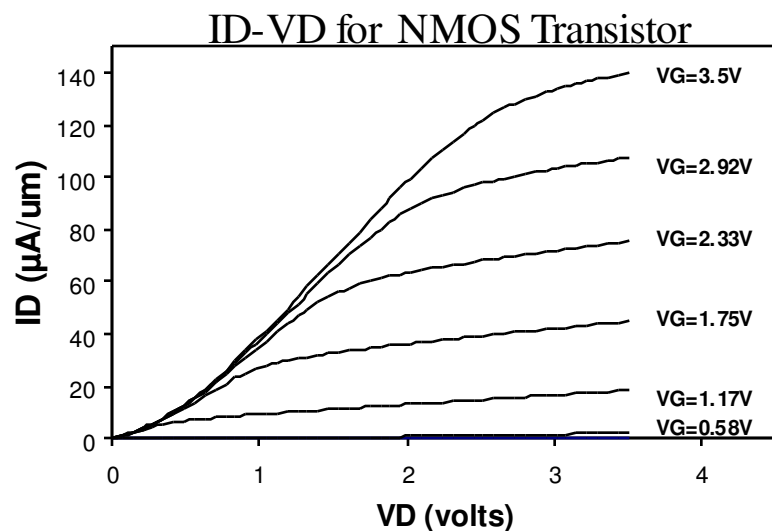
Ideal Ohmic
Al/p-silicon

Rectifying
Al/n-silicon

Tunneling Ohmic
Al/n⁺-silicon



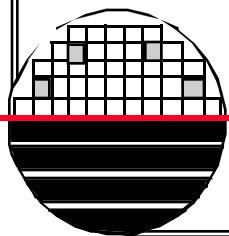
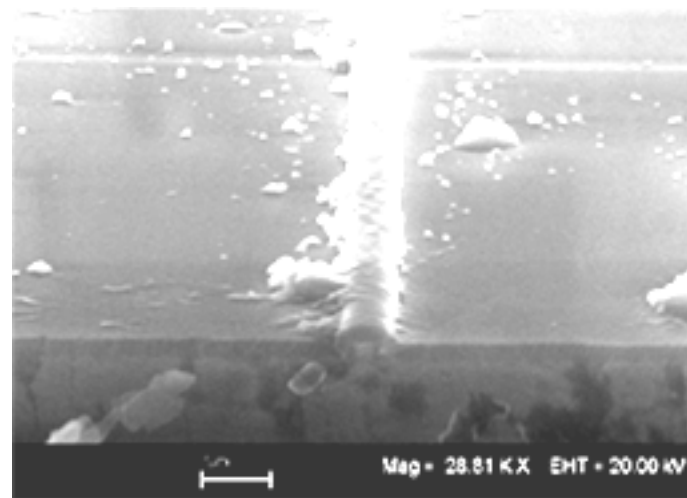
NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN ADV-CMOS PROCESS



$$L_{\text{mask drawn}} = 0.6 \mu\text{m}$$

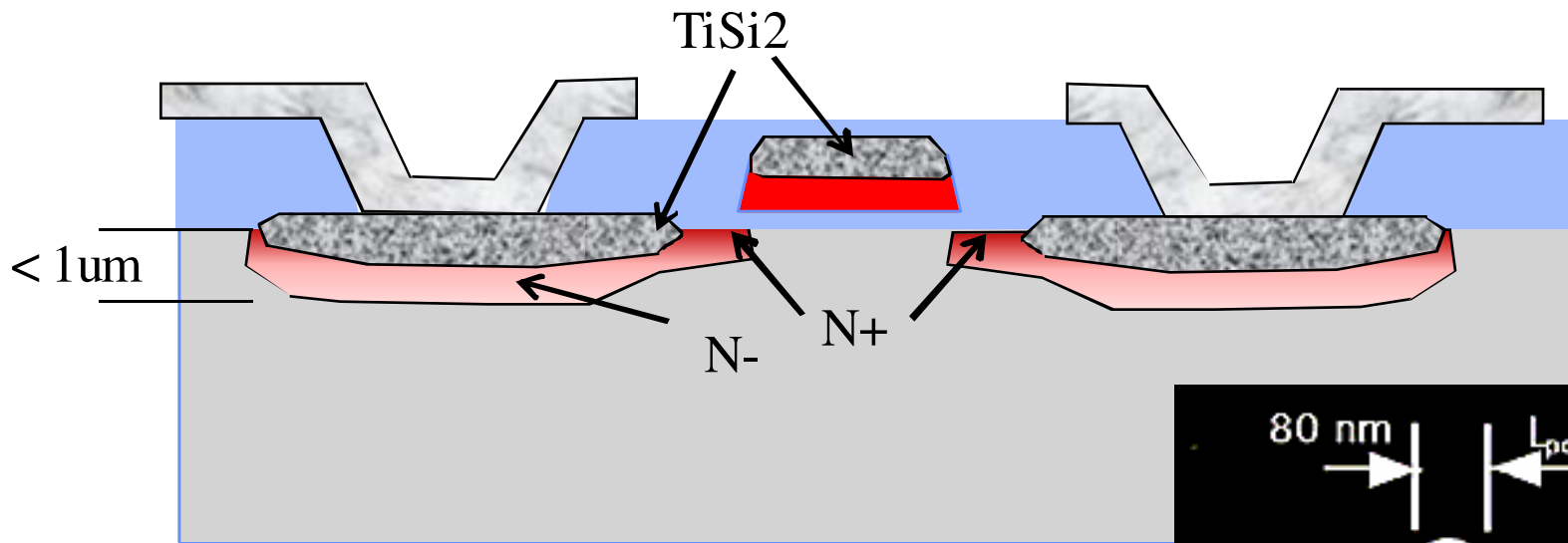
$$L_{\text{effective}} = 0.4 \mu\text{m}$$

This is RIT's first sub-0.5 μm Transistor

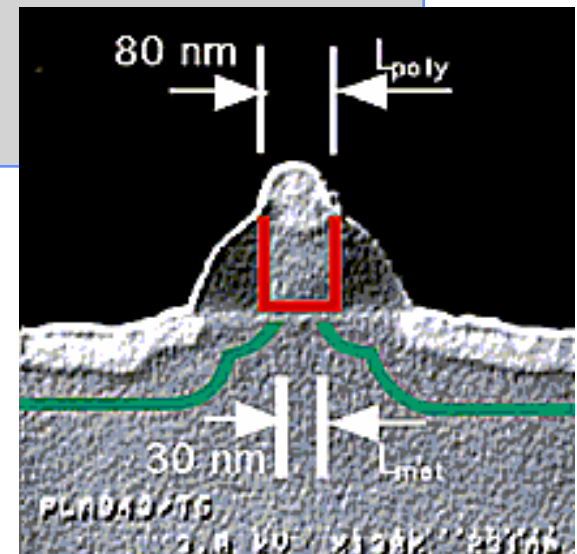


Mike Aquilino May 2004

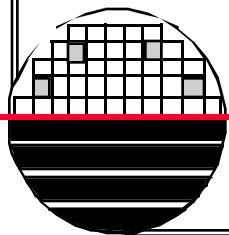
SILICIDE FORMATION CONSUMES SILICON



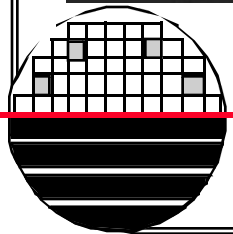
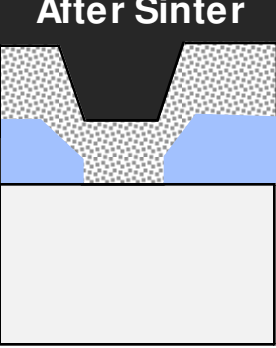
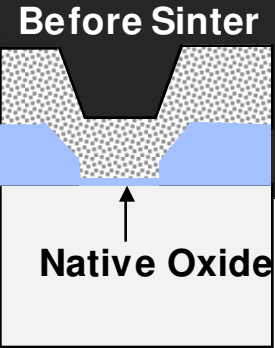
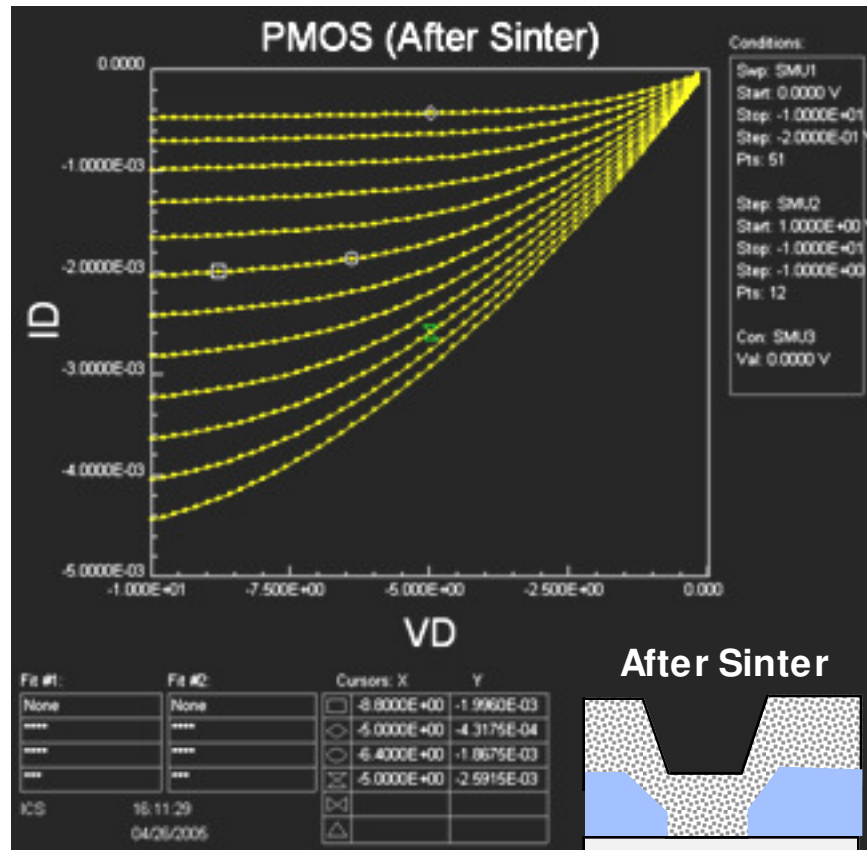
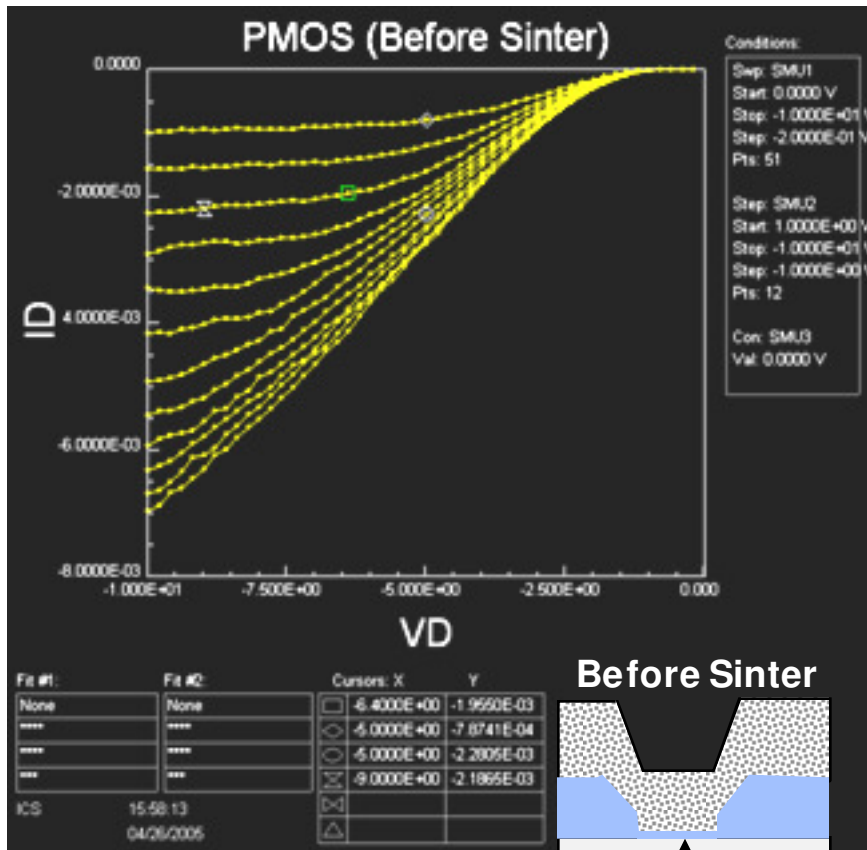
Too much silicide formation makes a non-ohmic (rectifying or Schottky) contact with the lighter doped n-type area of the drain/source.



IMEC Meeting
December 1999

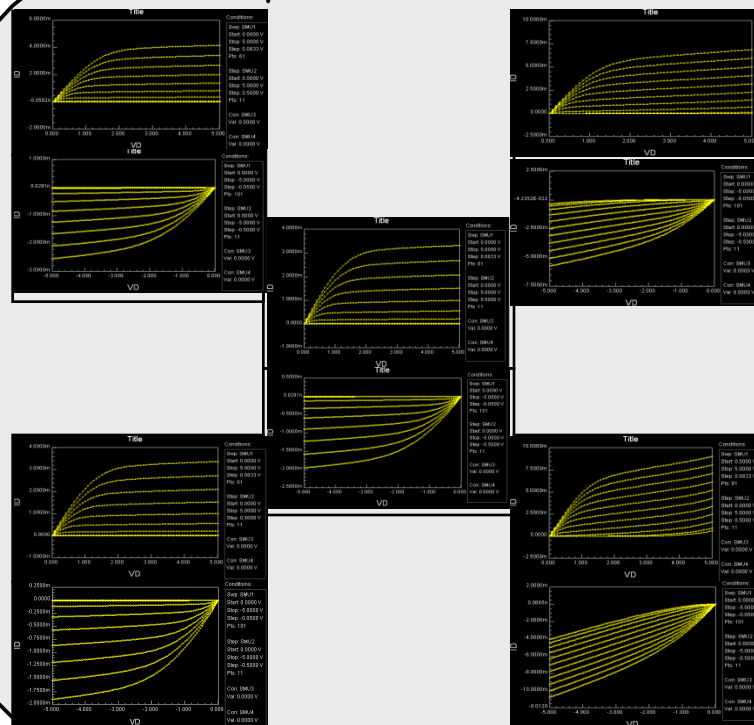


EFFECT OF SINTER ON IV CHARACTERISTICS

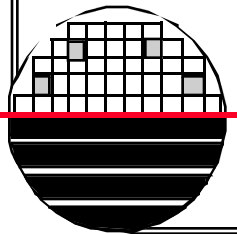


DIFFERENT LOOKING FAMILY OF CURVES AT DIFFERENT LOCATIONS ON THE WAFER

Family of curves for $L=2\mu\text{m}$ MOSFETs

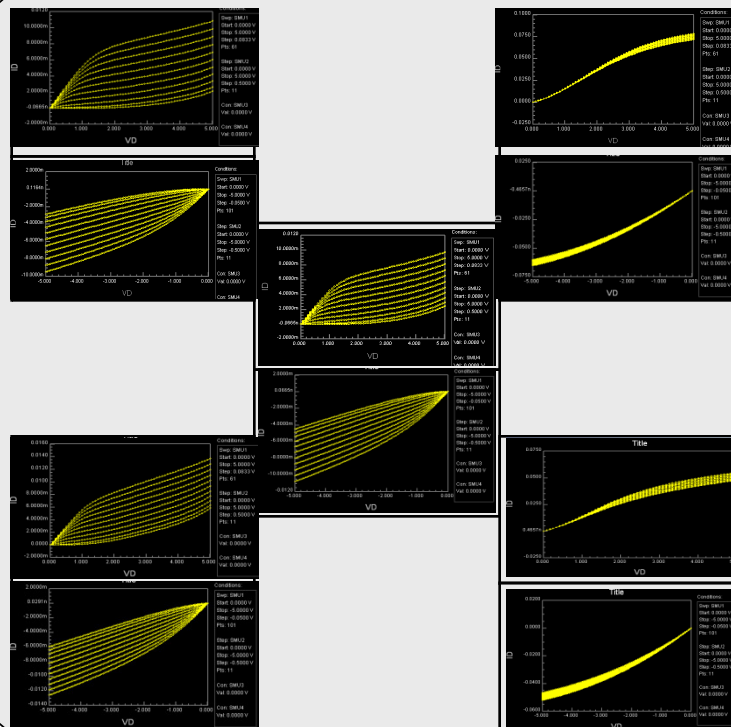


$2\mu\text{m}/32\mu\text{m}$ L/W NMOS AND PMOS

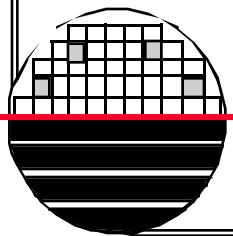


NON UNIFORMITY IN PLASMA ETCH OF POLY

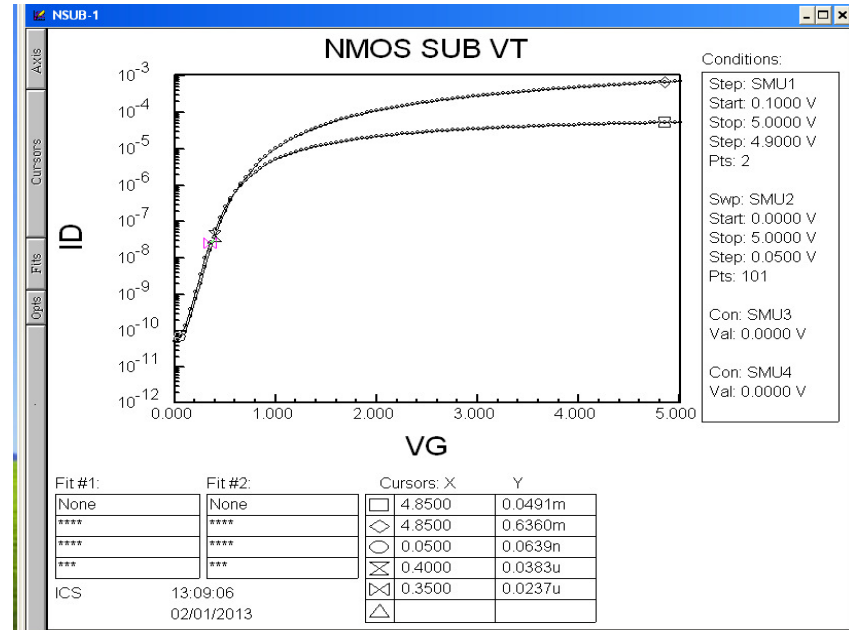
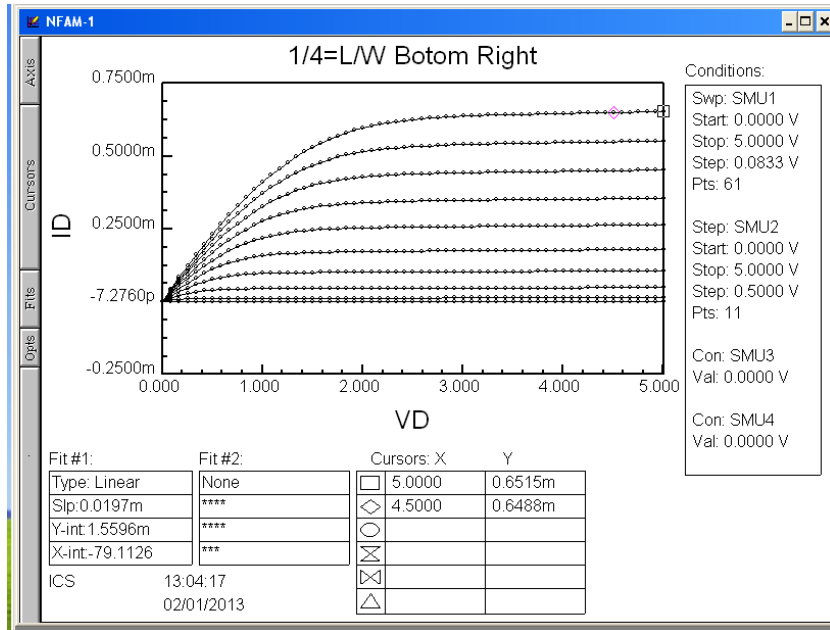
Family of curves for
 $L=2\mu\text{m}$ MOSFETs



$2\mu\text{m}/32\mu\text{m}$ L/W NMOS AND PMOS



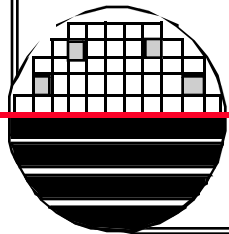
GOOD DEVICE SUB THRESHOLD CHARACTERISTICS



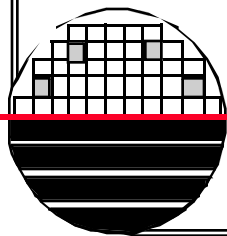
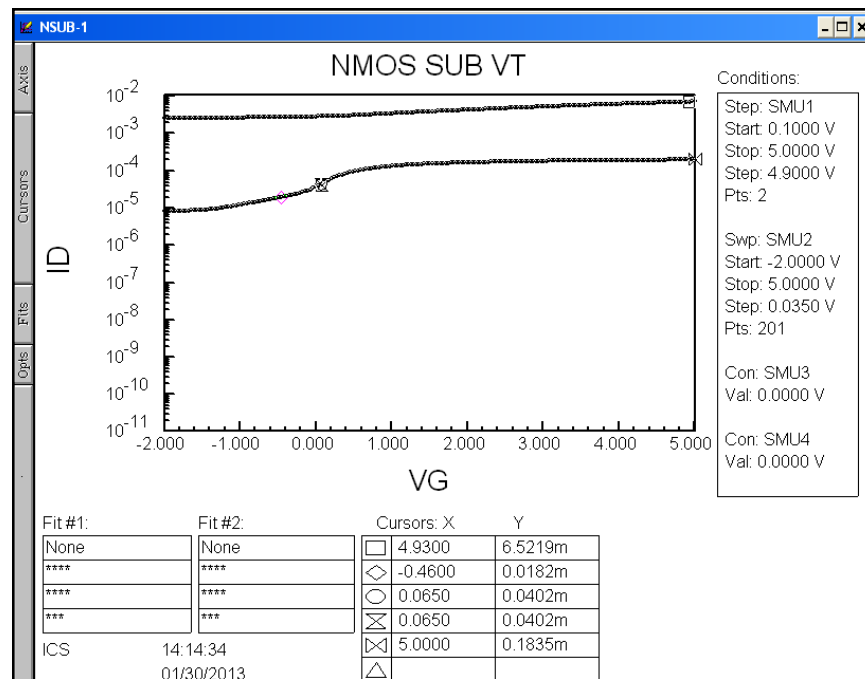
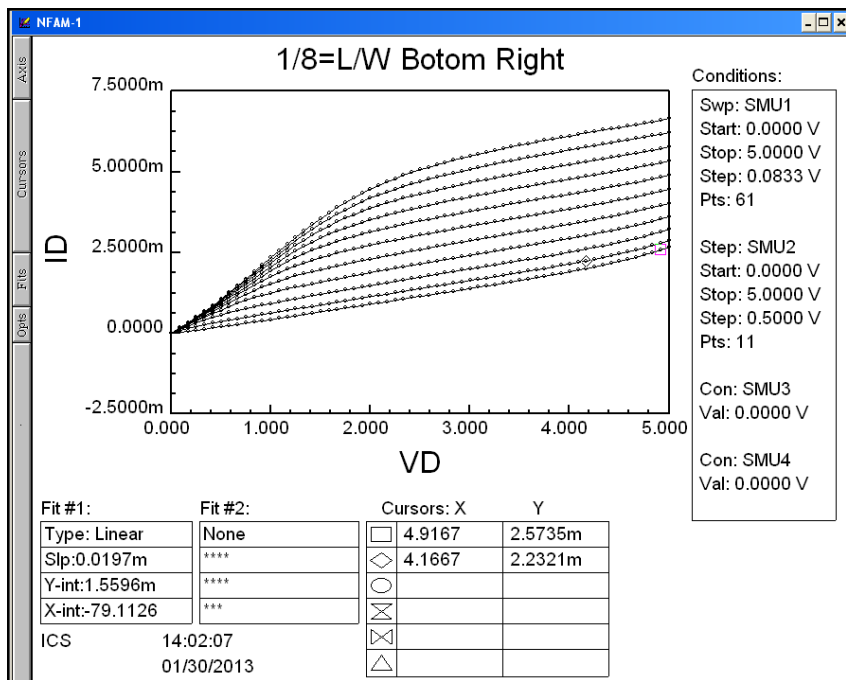
Occasionally our 1um Devices Work

Why does the sub-threshold plot not flatten out at the bottom?

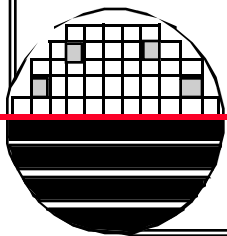
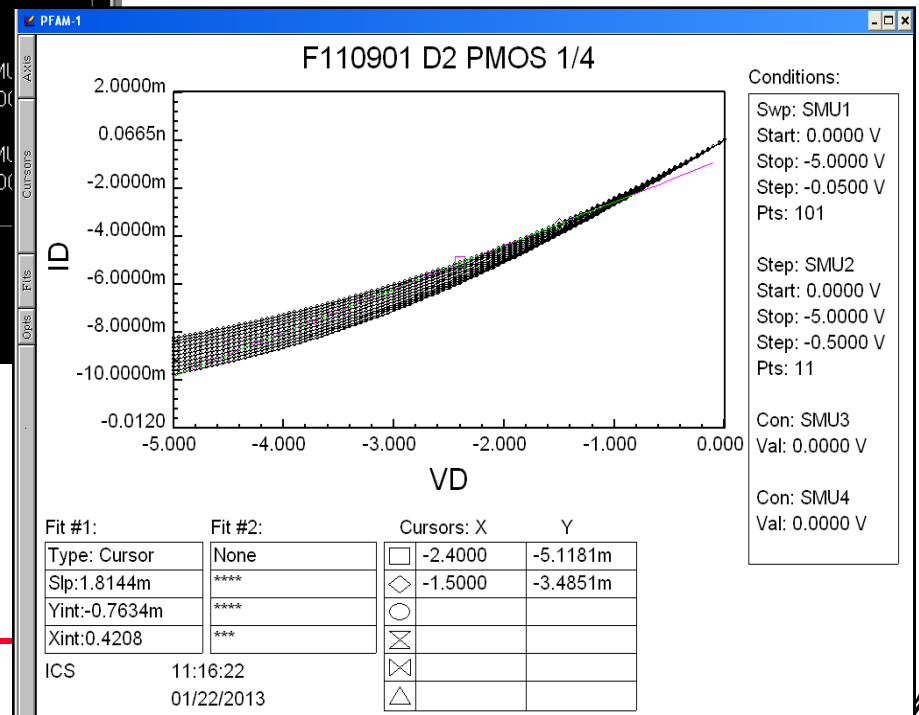
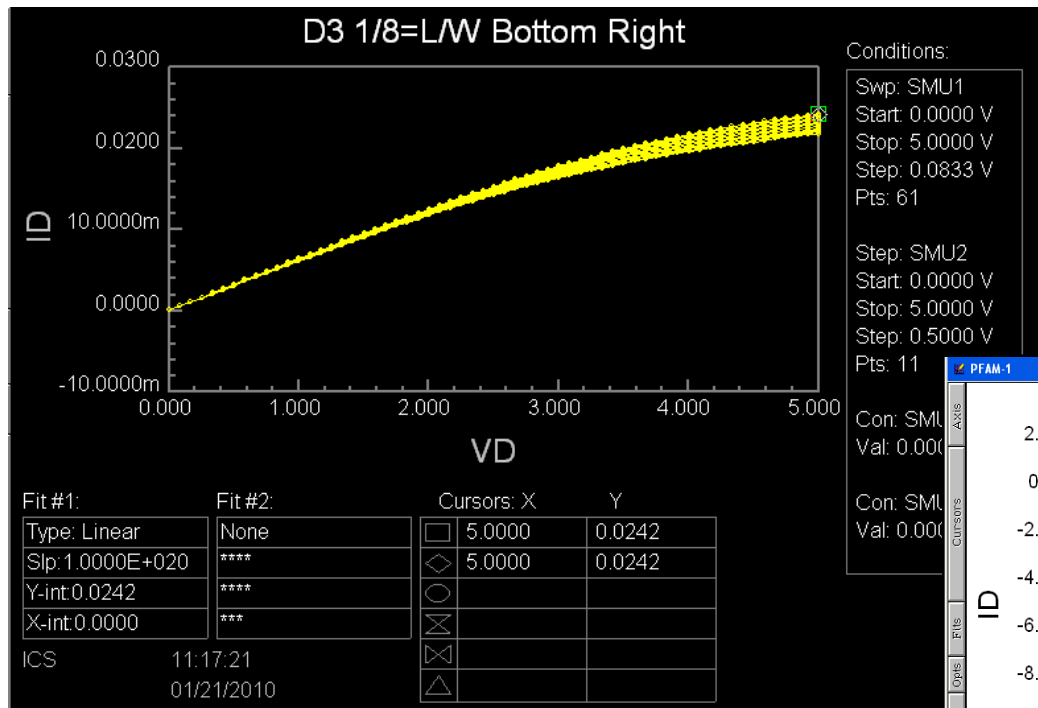
Answer: V_t is ~ 0.5 volt and swing is ~ 100 mV/decade so at zero volts the device can be down 5 decades of current which is 10^{-10} it should flatten out at $\sim 10^{-11}$ or 10^{-12} need higher V_t or smaller swing



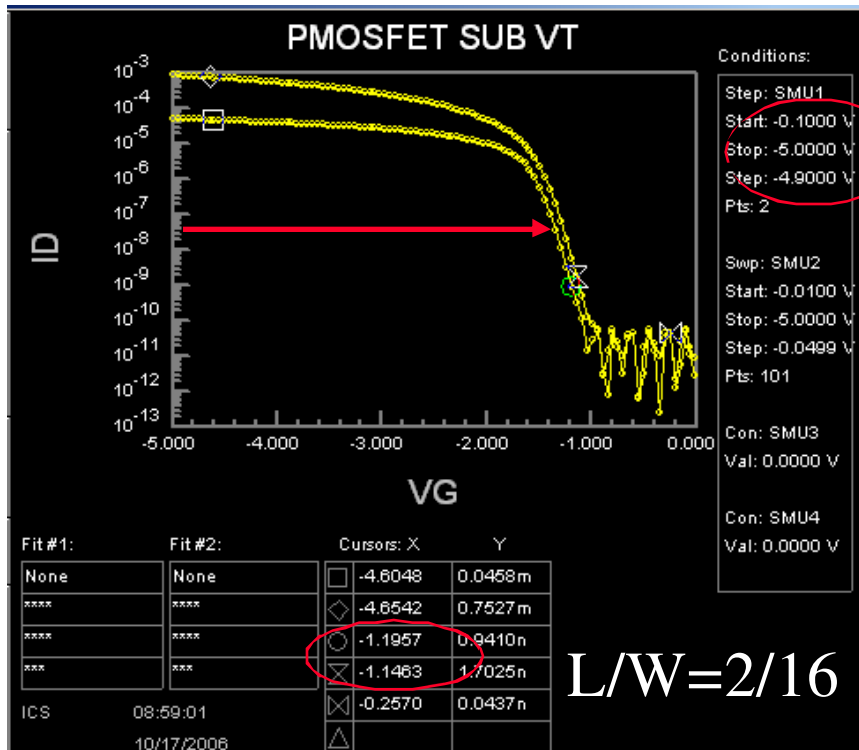
SHORT CHANNEL – BAD SUB THRESHOLD



REALLY SHORT CHANNEL



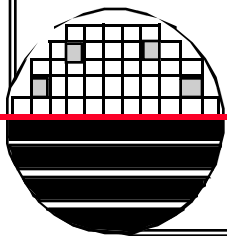
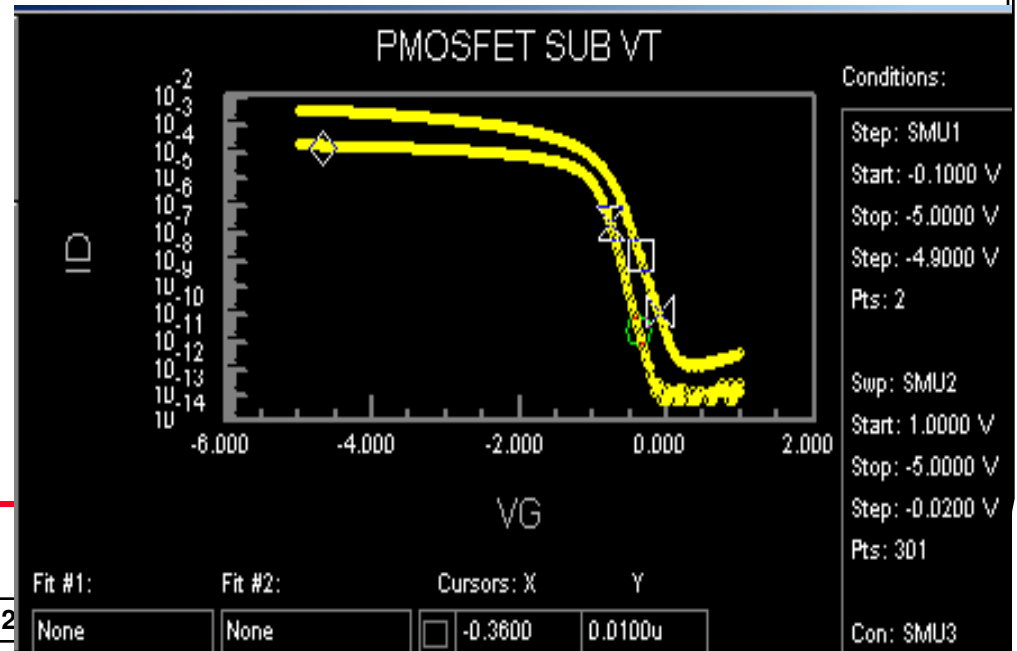
DRAIN INDUCED BARRIER LOWERING



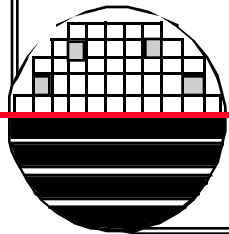
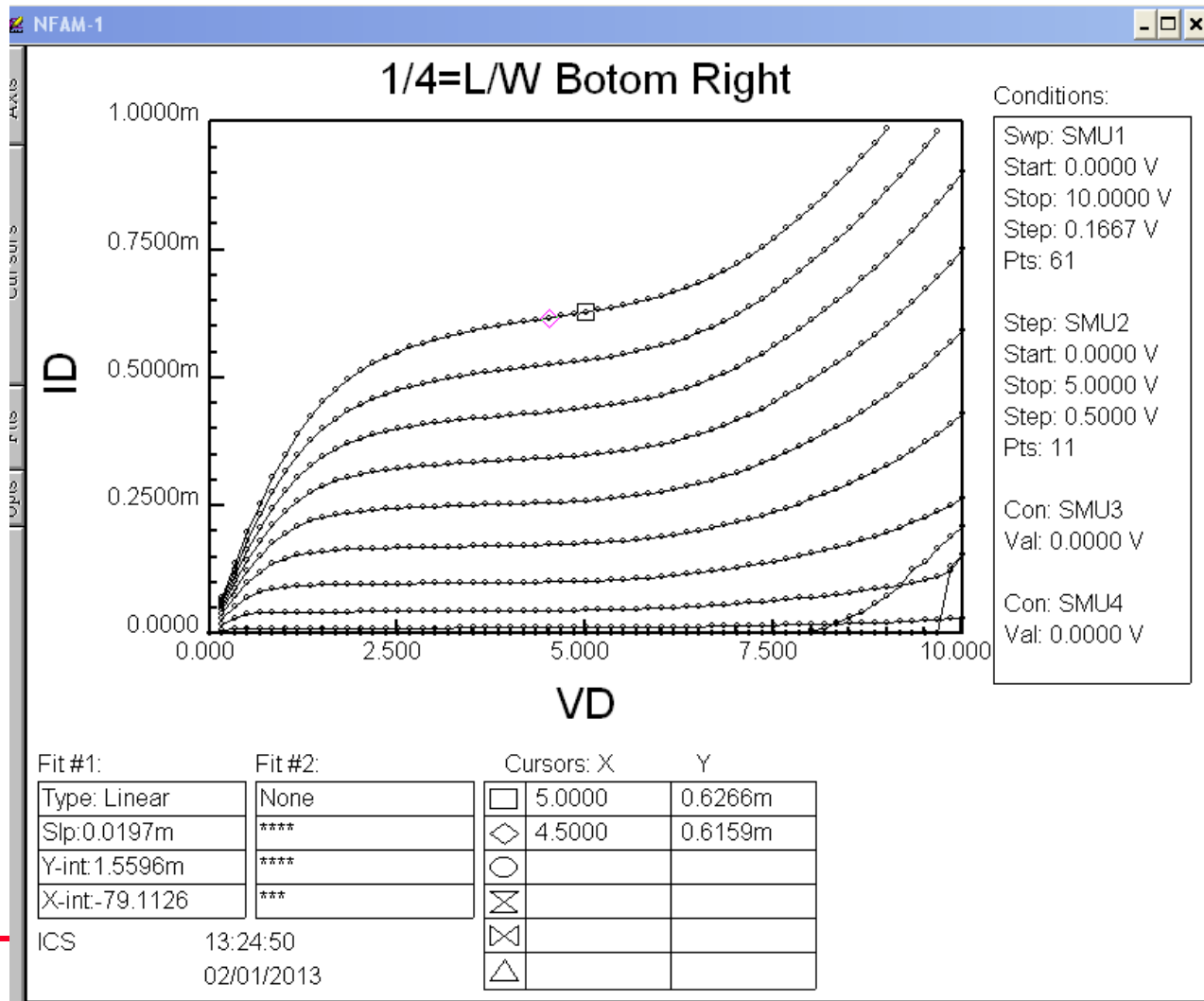
DIBL = change in VG /change in VD
 at ID=1E-9 amps/μm
 or 1.6E-8 amps for this
 size transistor

$$= \sim (1.1957 - 1.1463) / (5 - 0.1)$$

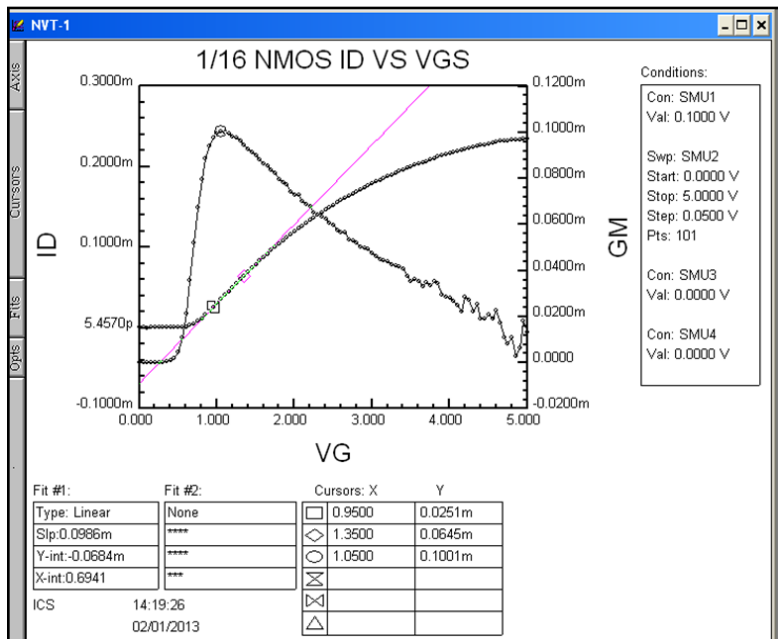
$$= \sim 10 \text{ mV/V}$$



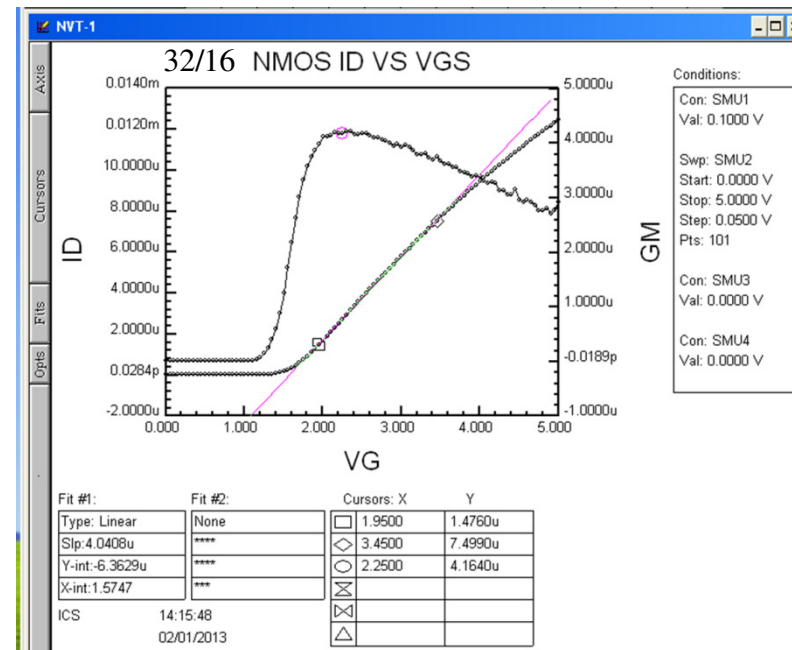
PUNCH THROUGH



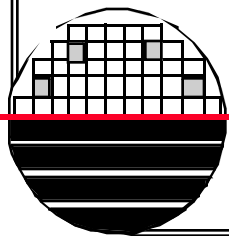
MOBILITY DEGRADATION



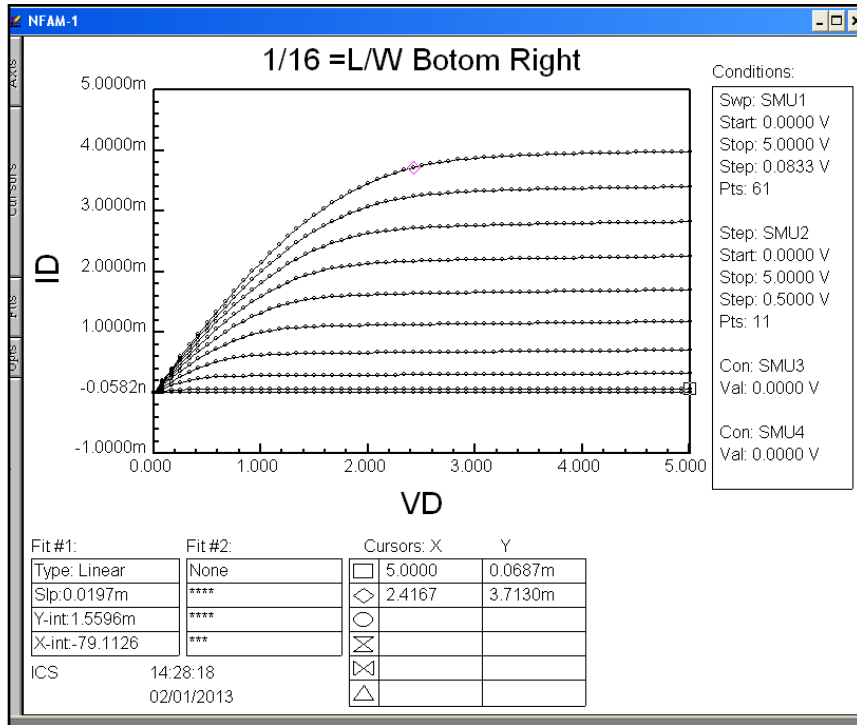
Short channel



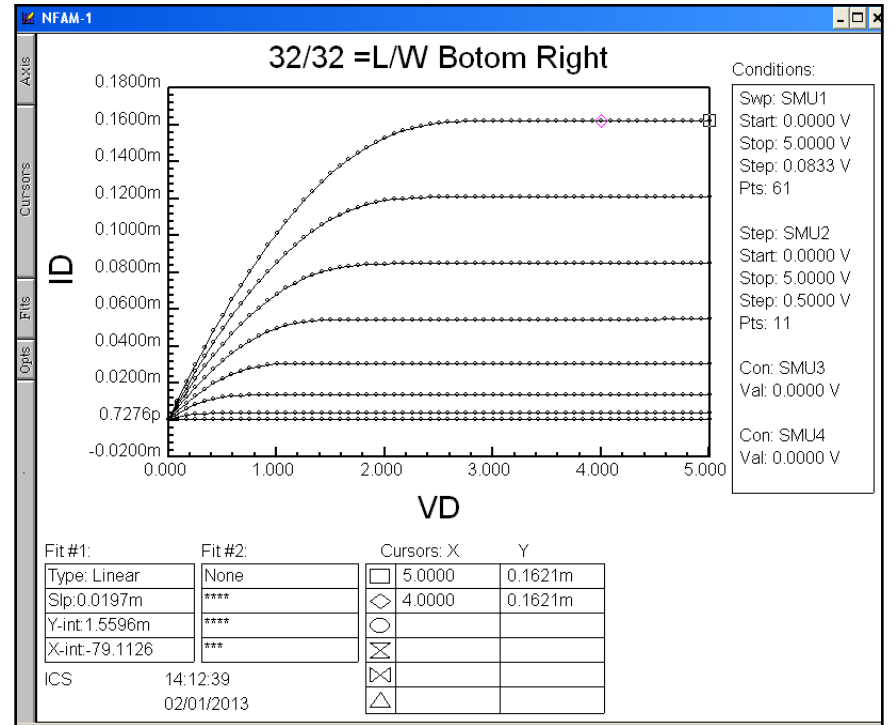
long channel



VELOCITY SATURATION

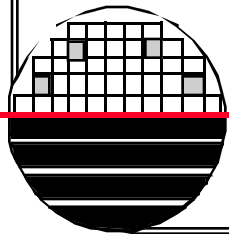


Short channel



long channel

Note: Id should increase with $(V_{gs}-V_t)^2$ in long channel devices



RIT's FIRST SUB MICRON TRANSISTOR

Mark Klare 7/22/94 Electron beam direct write on wafer, n-well process 5E12 dose, P+ Poly Gate PMOS, shallow BF2 D/S implant, no Vt adjust implant.

$L=0.75 \mu\text{m}$

$X_{\text{ox}}=300 \text{ \AA}$

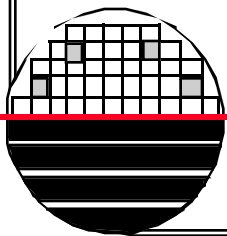
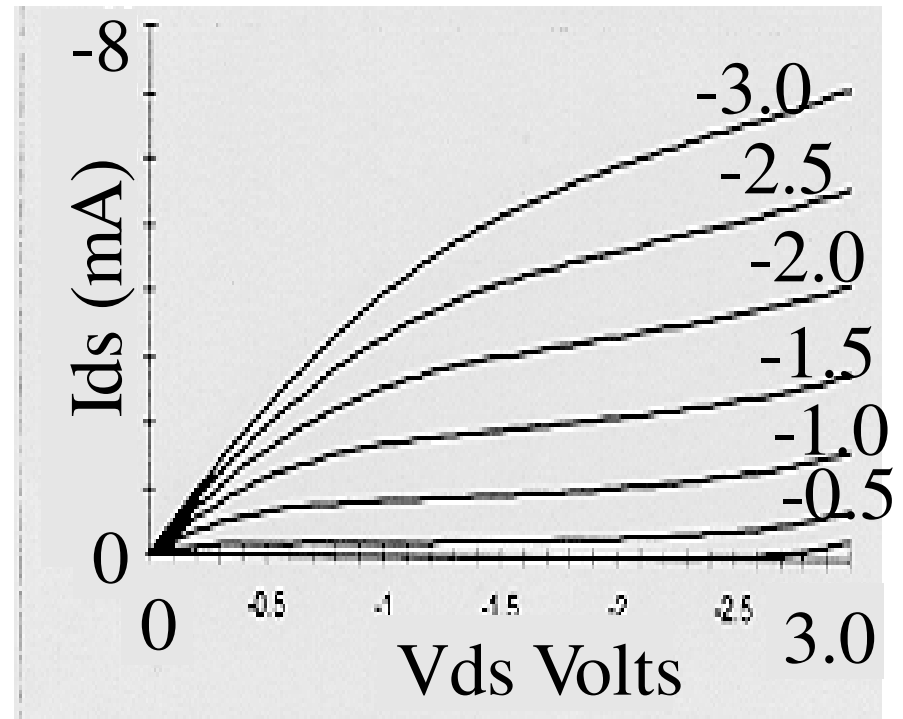
D/S $X_j = 0.25 \mu\text{m}$

P+ poly

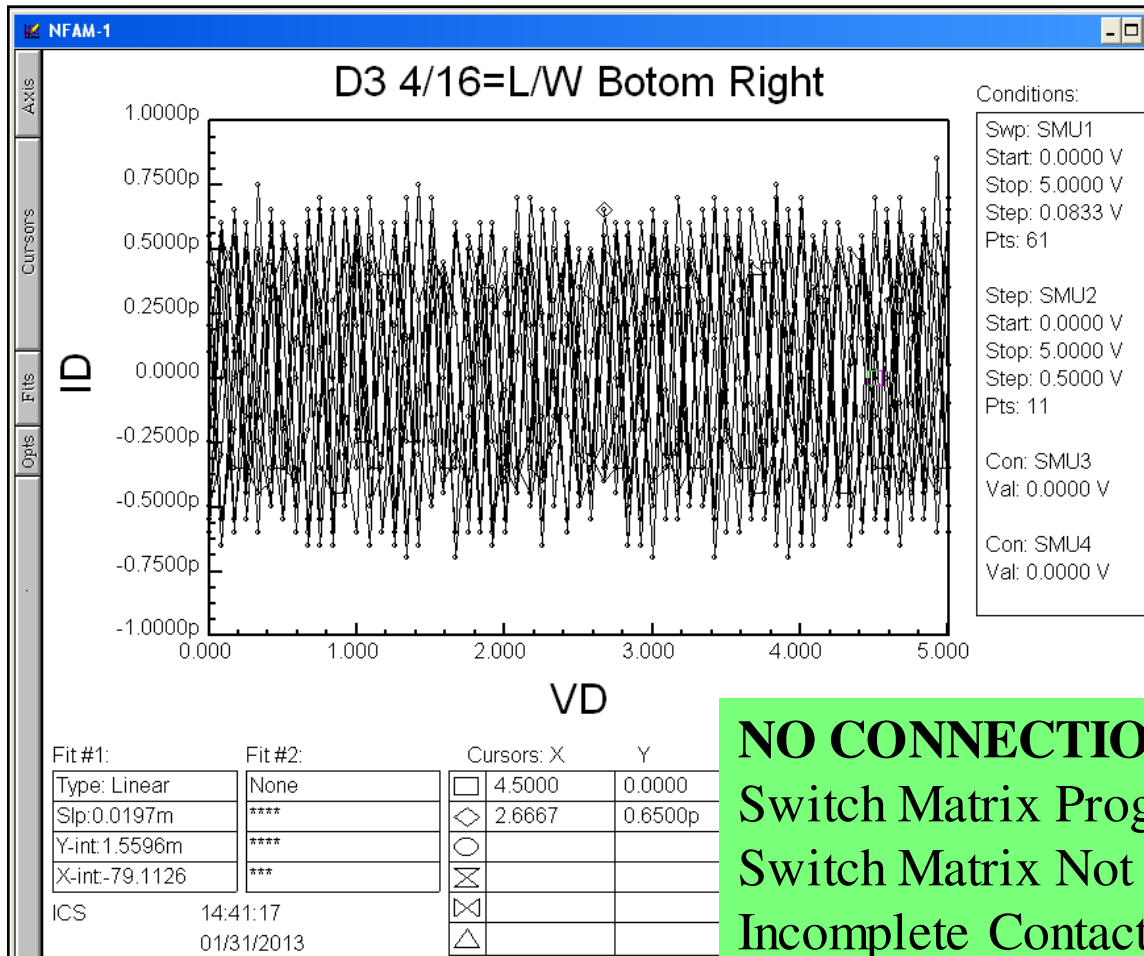
Nd well $\sim 3\text{E}16$

$V_t = -0.15$

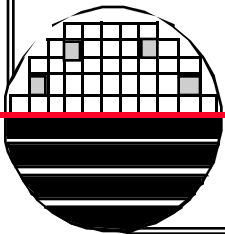
Sub Vt Slope=130 mV/dec



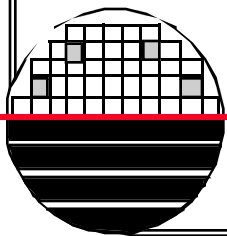
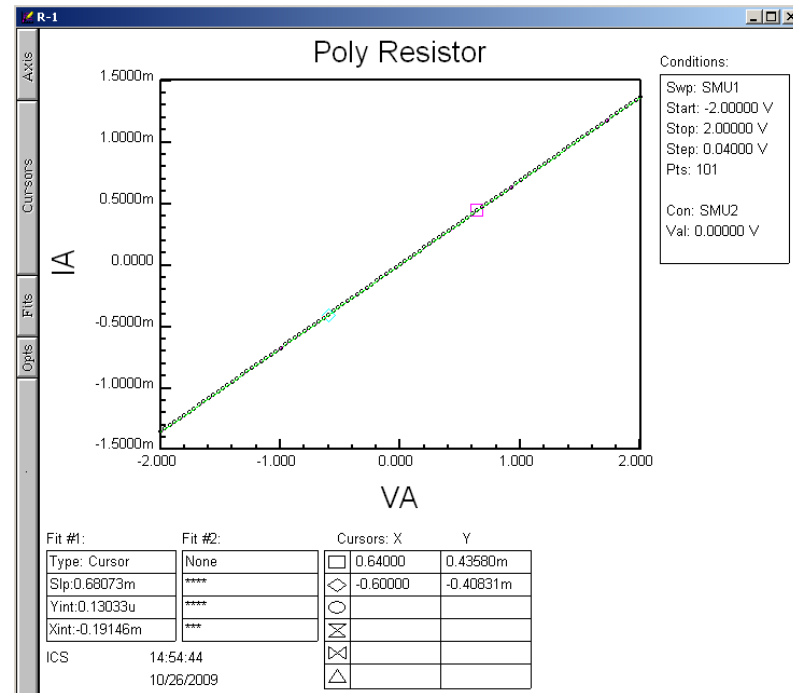
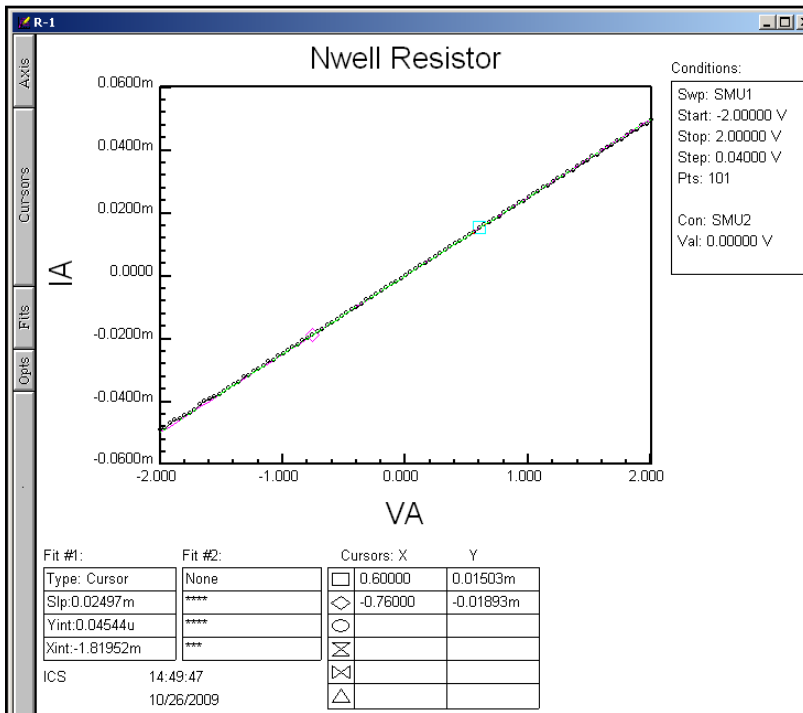
WHAT IS WRONG?



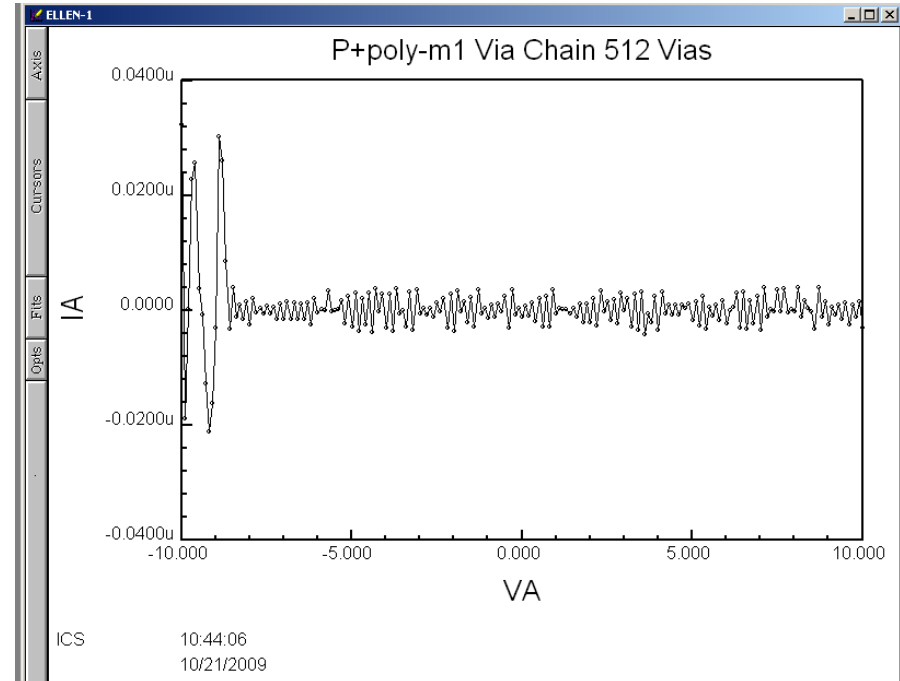
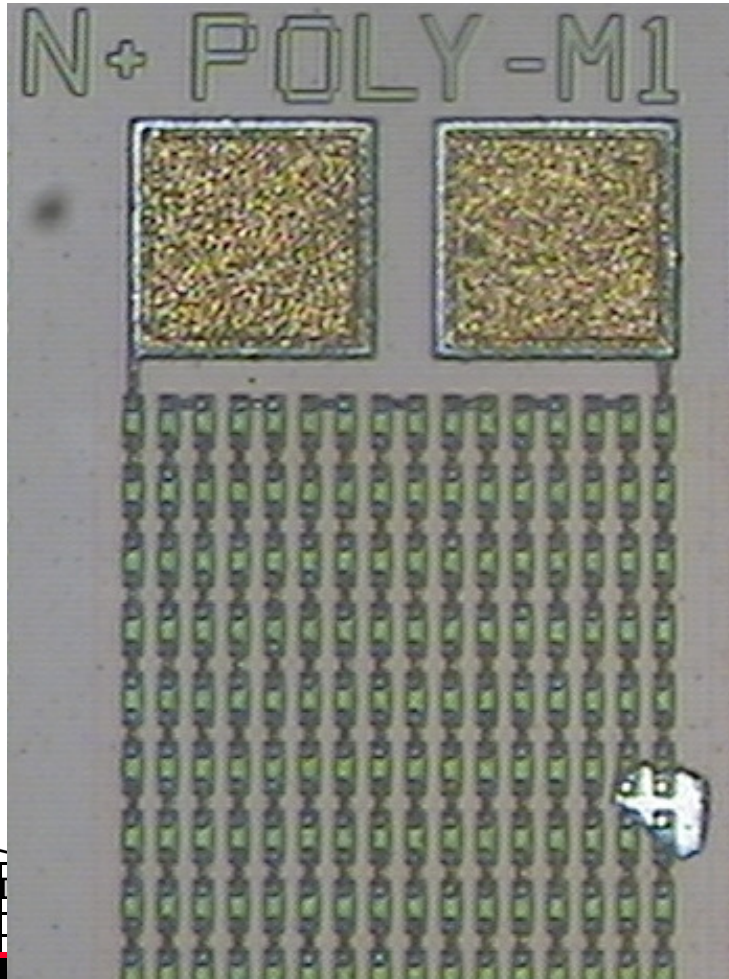
NO CONNECTION
Switch Matrix Programmed Wrong
Switch Matrix Not Copied
Incomplete Contact Cut Etch
Aluminum Oxide Between M1 and M2



GOOD RESISTOR CHARACTERISTICS

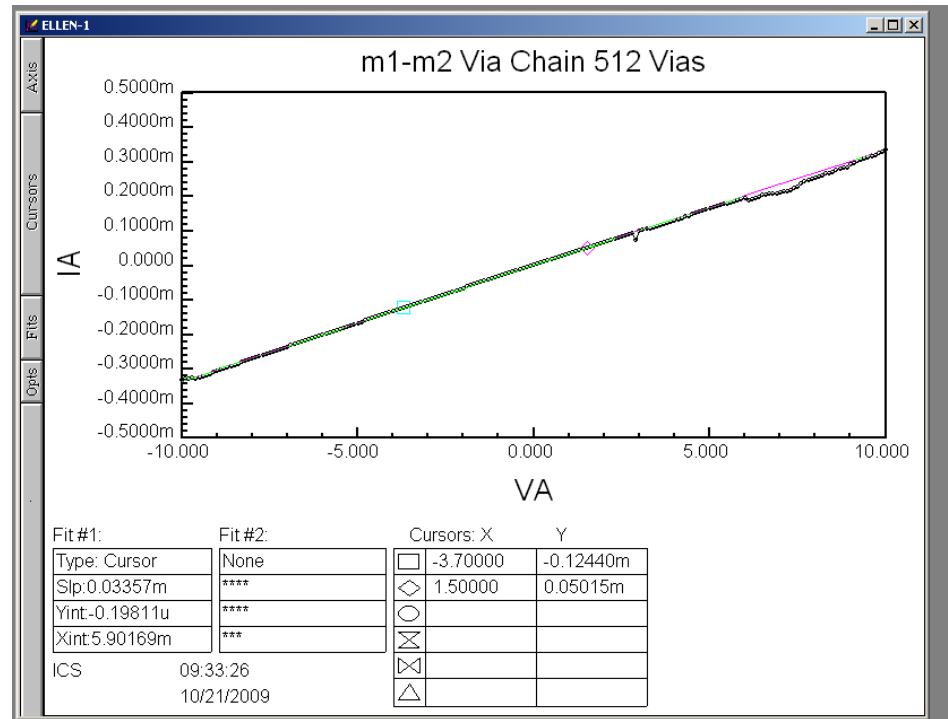
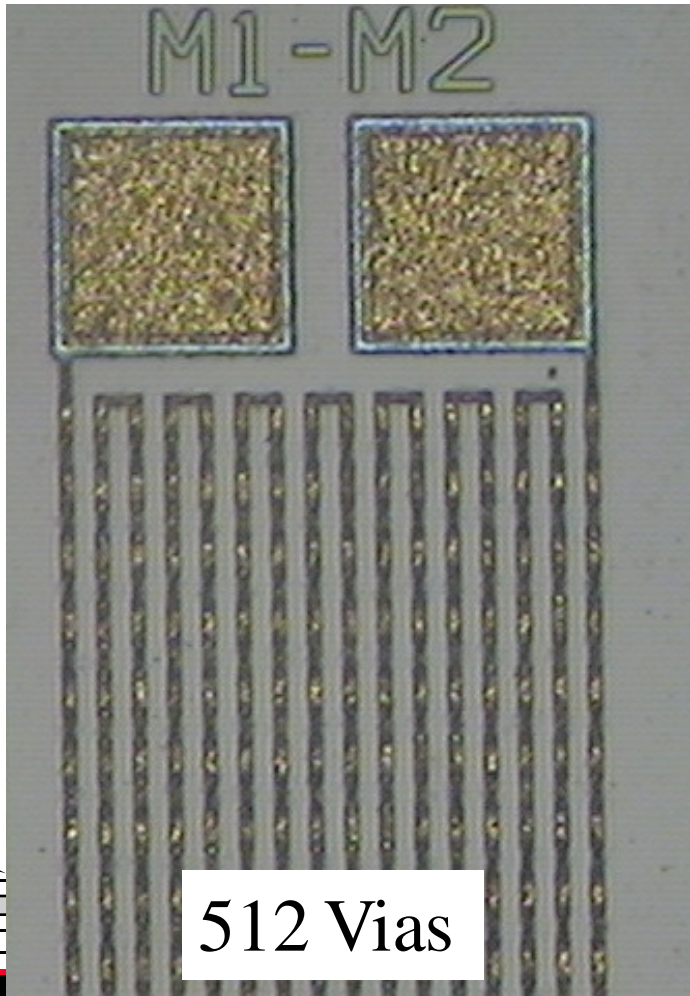


IS THIS GOOD?



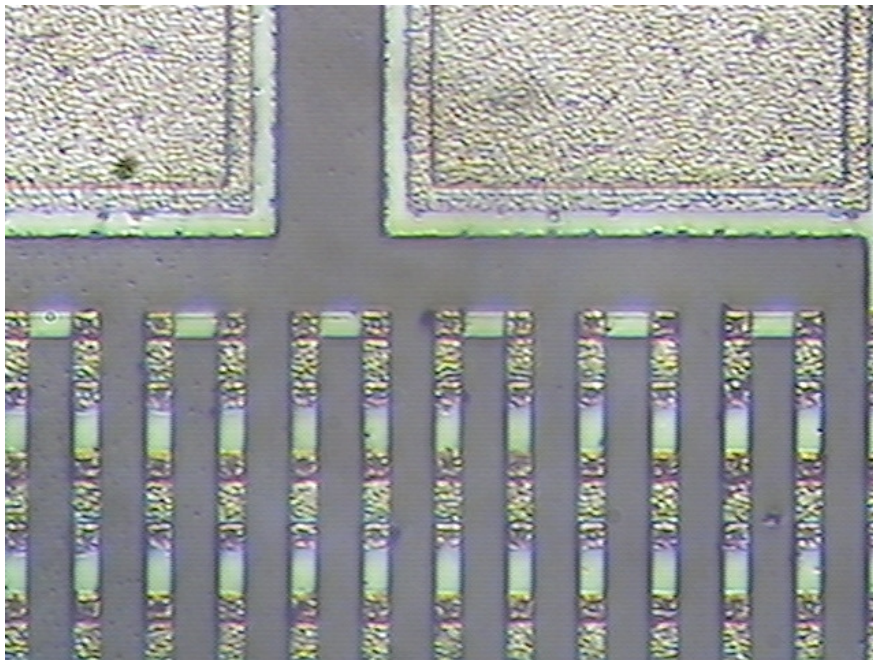
NO
Open Circuit, both electrical and visual evidence

IS THIS GOOD?

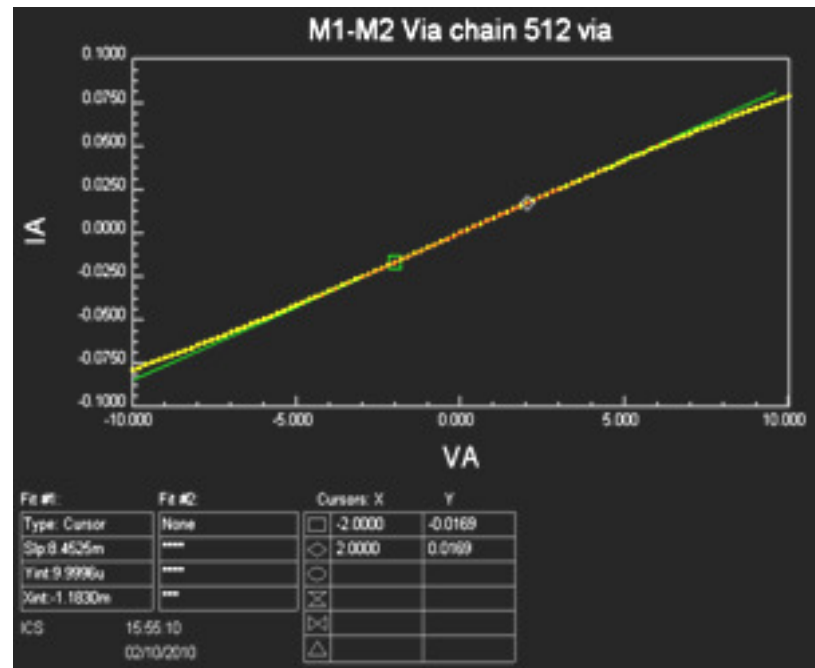


NO
 $R = 1 / \text{slope} = 1 / 0.03357\text{m} = 29,788 \text{ ohms}$
which is 58 ohms/contact

IS THIS GOOD?



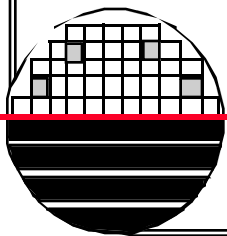
512 Vias



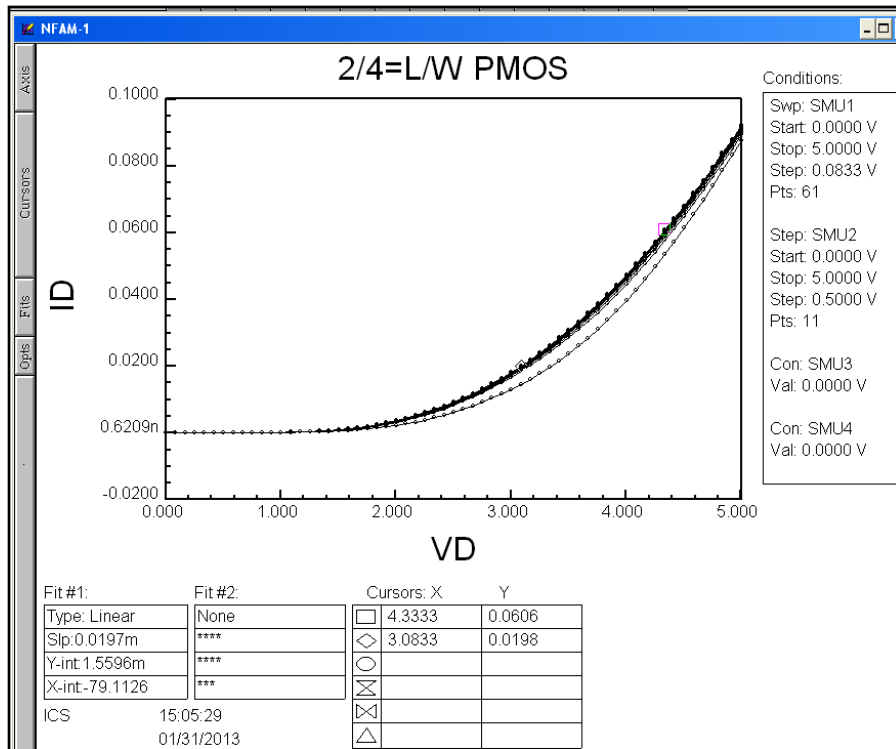
F081201

YES

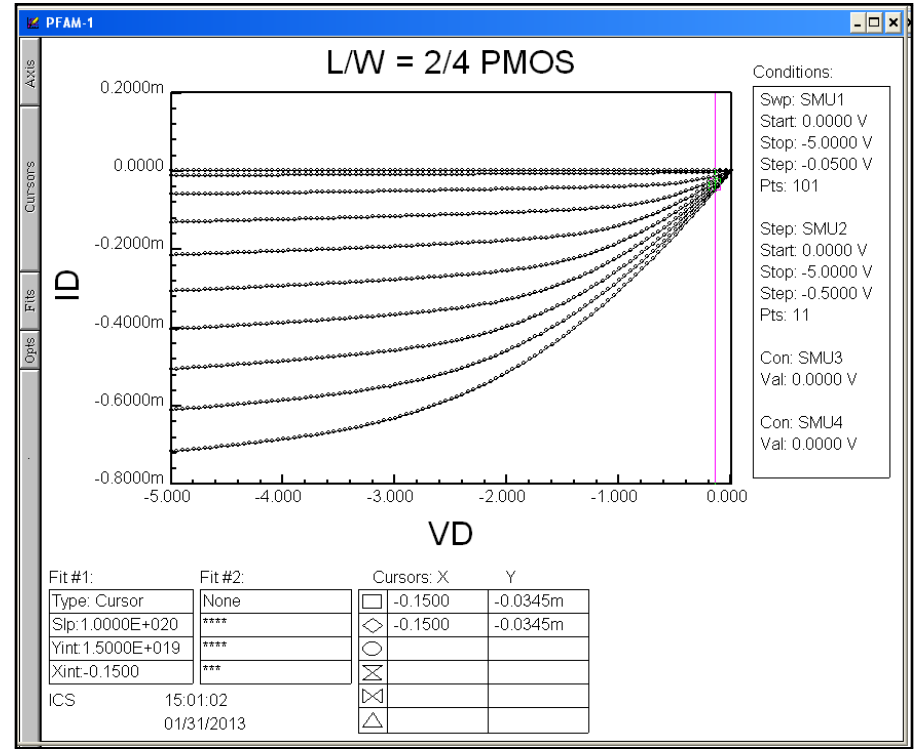
M1-M2 Via chain with 512 Vias and total resistance of 118 ohms or 0.231 ohms per contact



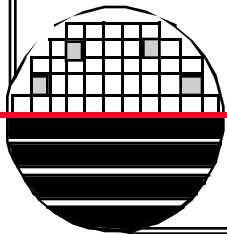
WHAT IS WRONG?



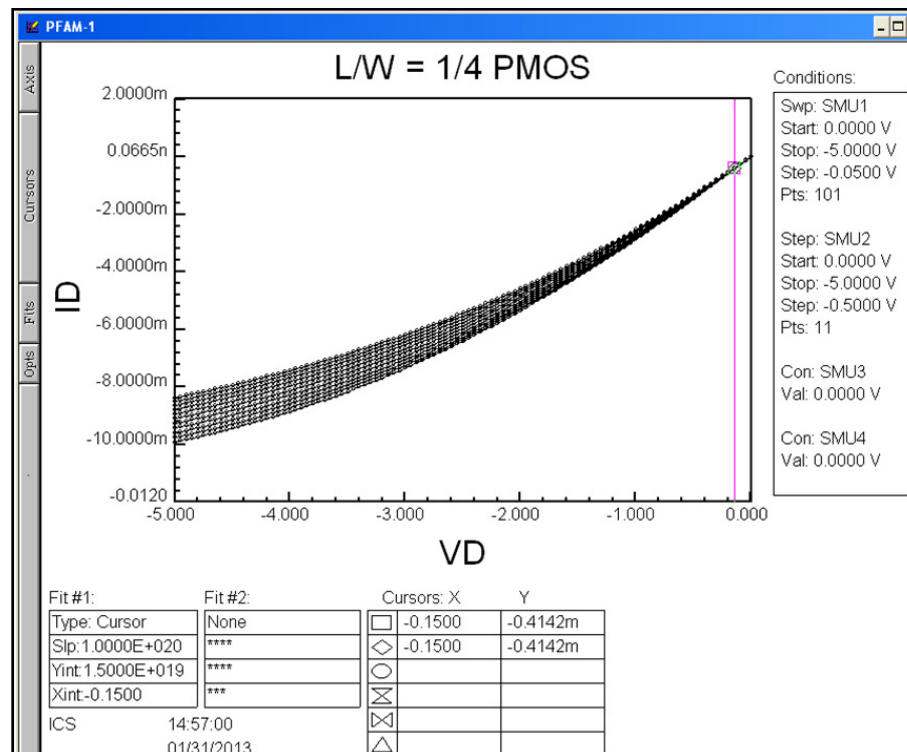
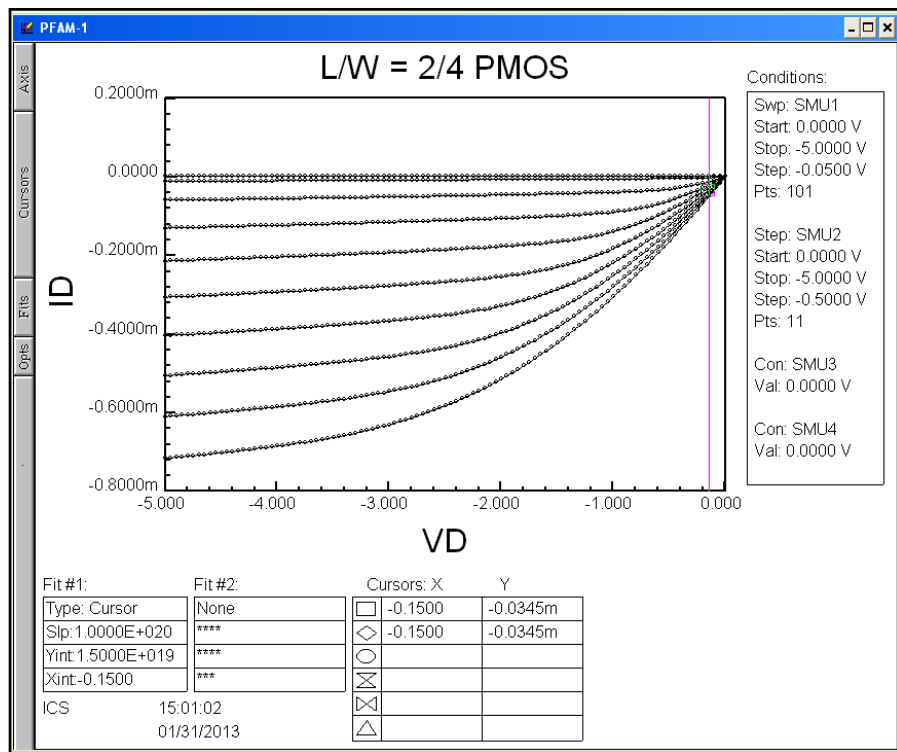
Testing PMOS with NMOS-1 Setup



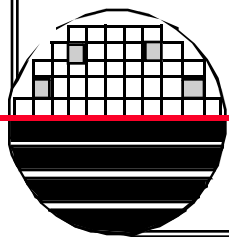
Testing PMOS with PMOS-1 Setup



WHAT IS WRONG?



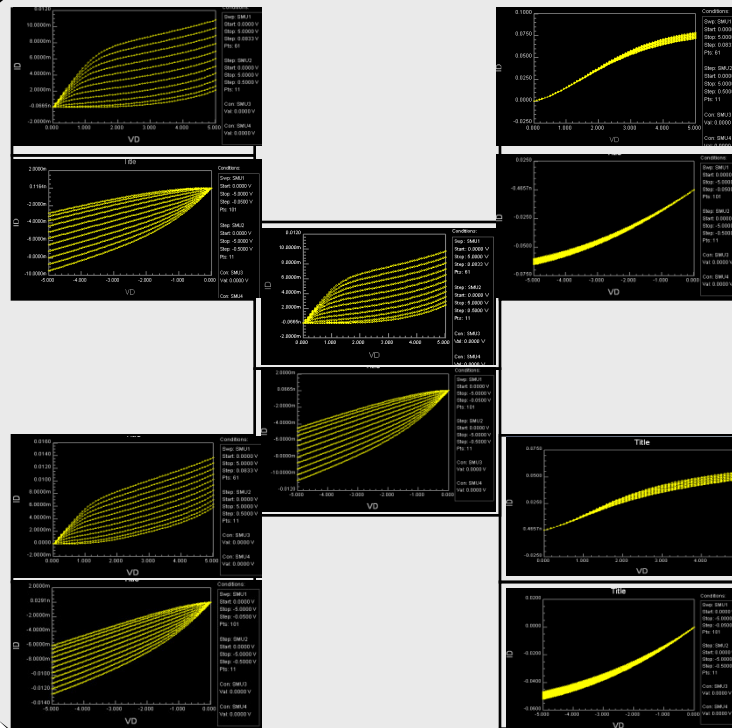
Leff is almost zero
Poly over etched making L too small
PMOS works at L/W = 2/4 but not at 1/4



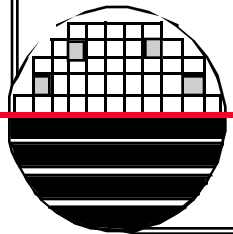
NON UNIFORMITY IN PLASMA ETCH OF POLY

Lot Number = F050118
Wafer Number = D3

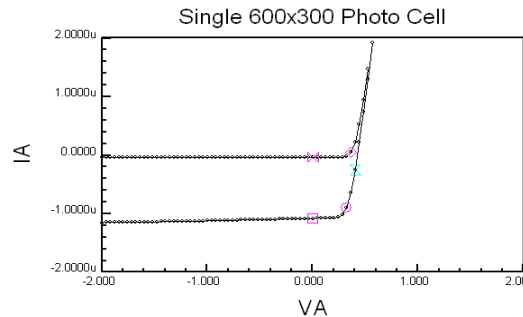
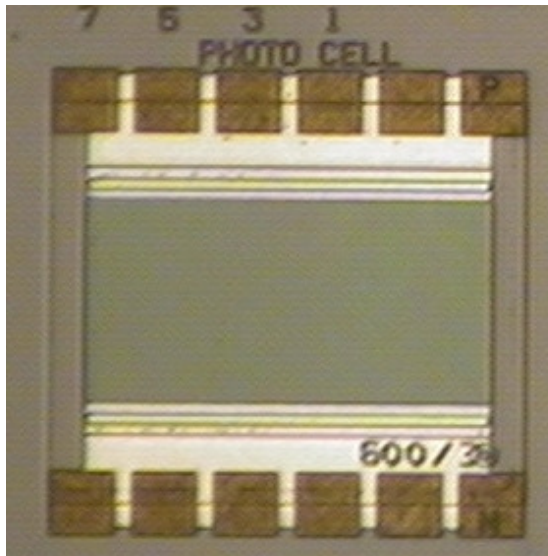
Family of curves for
L=2 μ m MOSFETs



2 μ m/32 μ m L/W NMOS AND PMOS



SINGLE AND DUAL PHOTO CELL

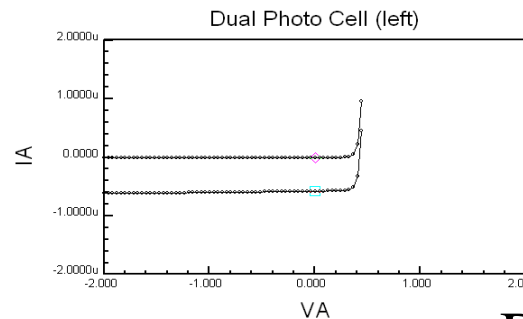
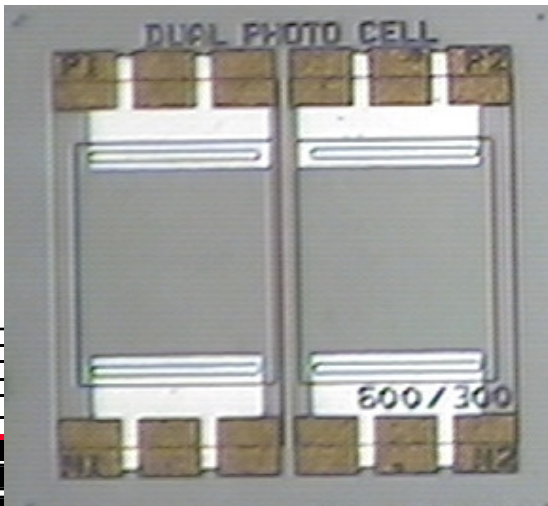


Conditions:
 Swp: SMU1
 Start: -2.00000 V
 Stop: 2.00000 V
 Step: 0.04000 V
 Pts: 101
 Con: SMU2
 Val: 0.00000 V

Isc = 1.088 uA
 or 6 A/m²

Fit #1:	Fit #2:	Cursors: X	Y
None	None	0.00000	-1.08800u
***	***	0.36000	0.04135u
***	***	0.32000	-0.90894u
***	***	0.40000	-0.26045u
***	***	0.00000	-0.04408u

ICS 10:48:12
10/27/2009



Conditions:
 Swp: SMU1
 Start: -2.00000 V
 Stop: 2.00000 V
 Step: 0.04000 V
 Pts: 101
 Con: SMU2
 Val: 0.00000 V

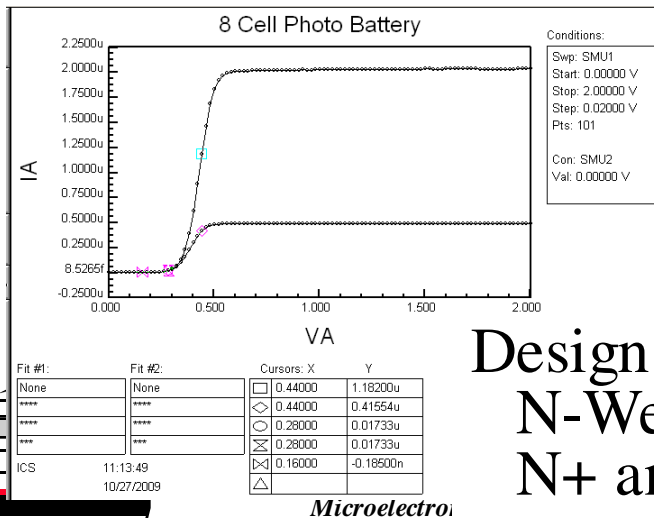
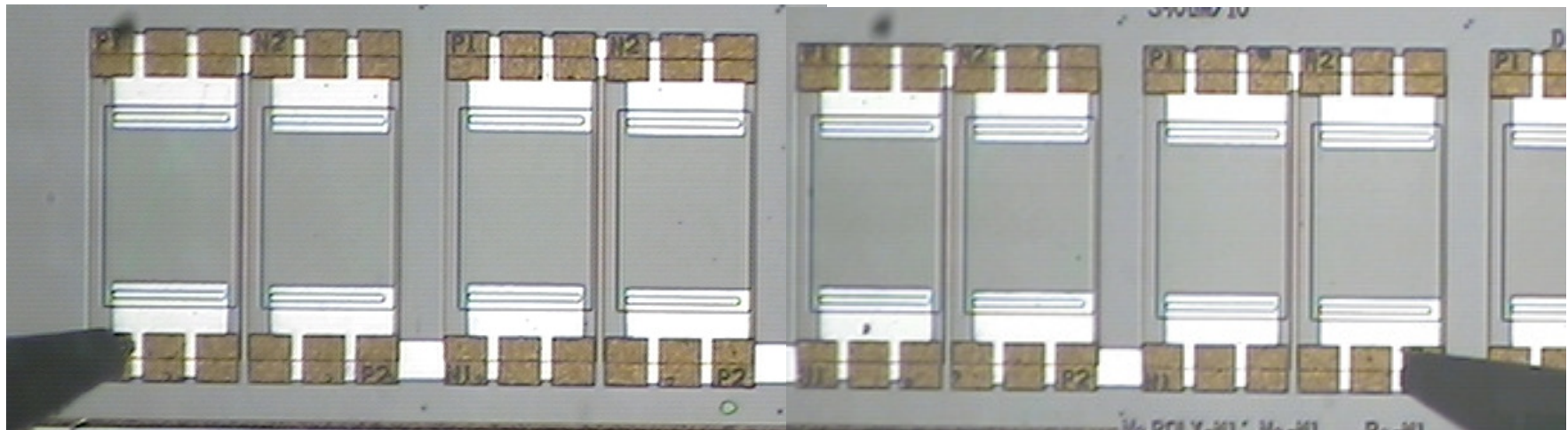
Isc = 0.585 uA
 or 3.25 A/m²

Fit #1:	Fit #2:	Cursors: X	Y
None	None	0.00000	-0.58580u
***	***	0.00000	-7.96390n
***	***		
***	***		

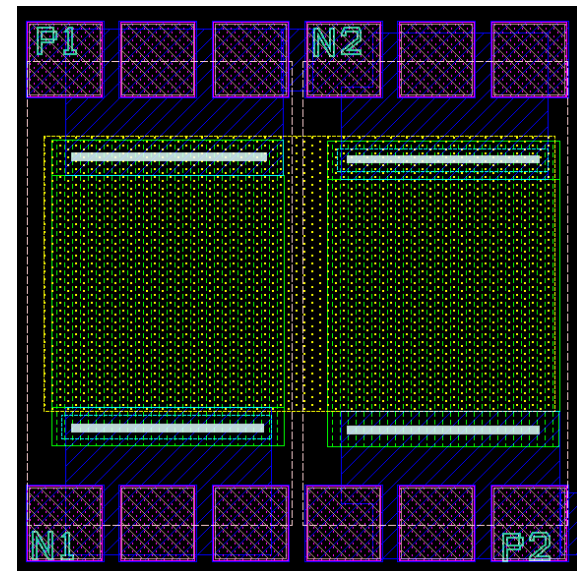
ICS 11:29:09
10/27/2009

Diode Characteristics
 Shifts Down with Light

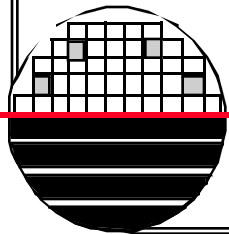
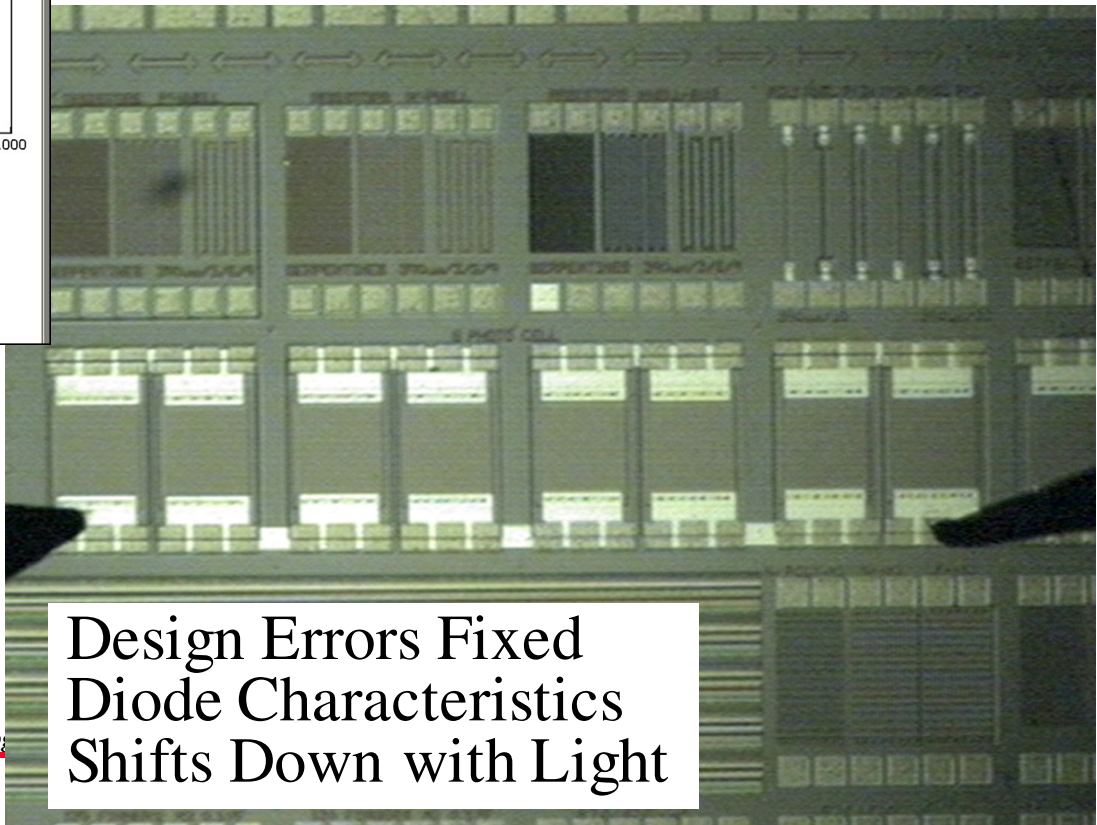
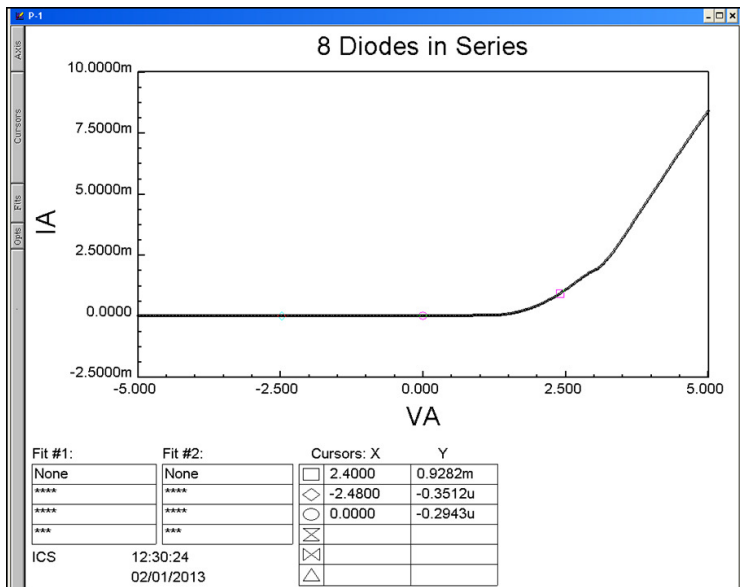
8-CELL PHOTO BATTERY – NOT CORRECT



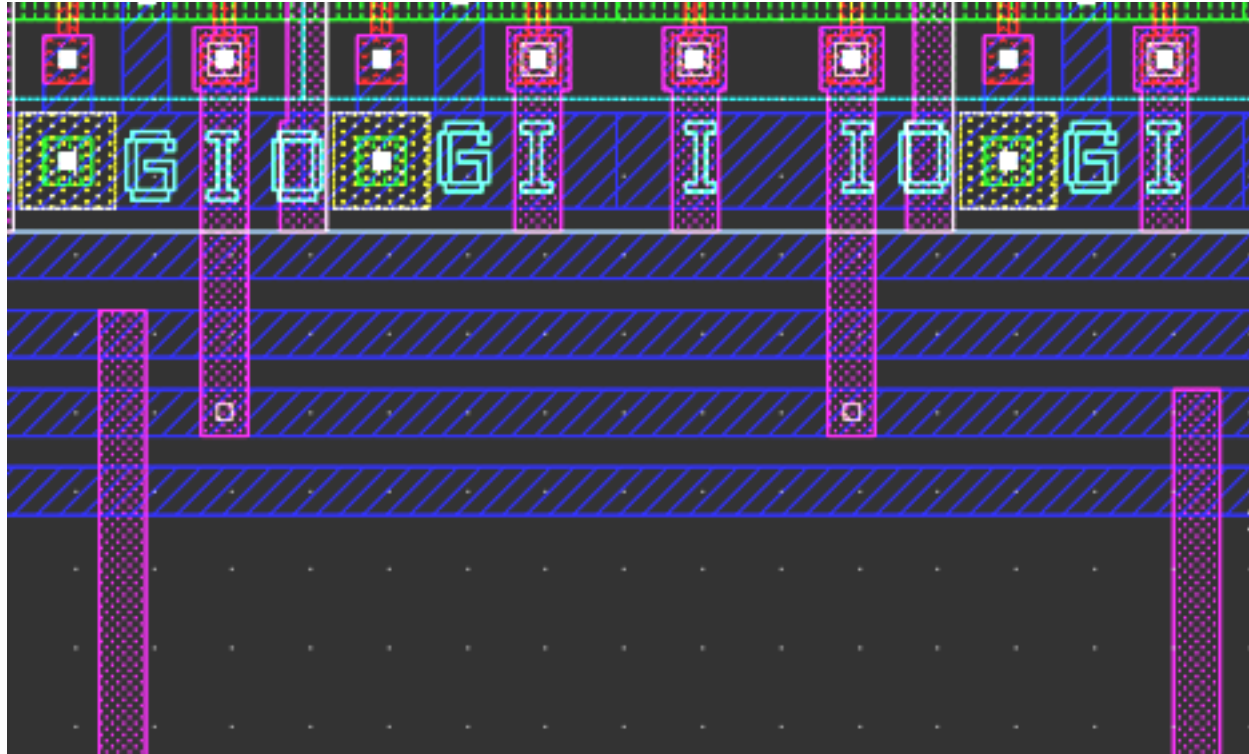
Design Errors
 N-Wells too close
 N+ and P+ not correct



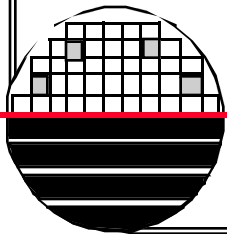
8-CELL PHOTO BATTERY



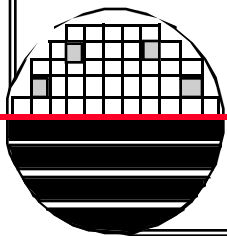
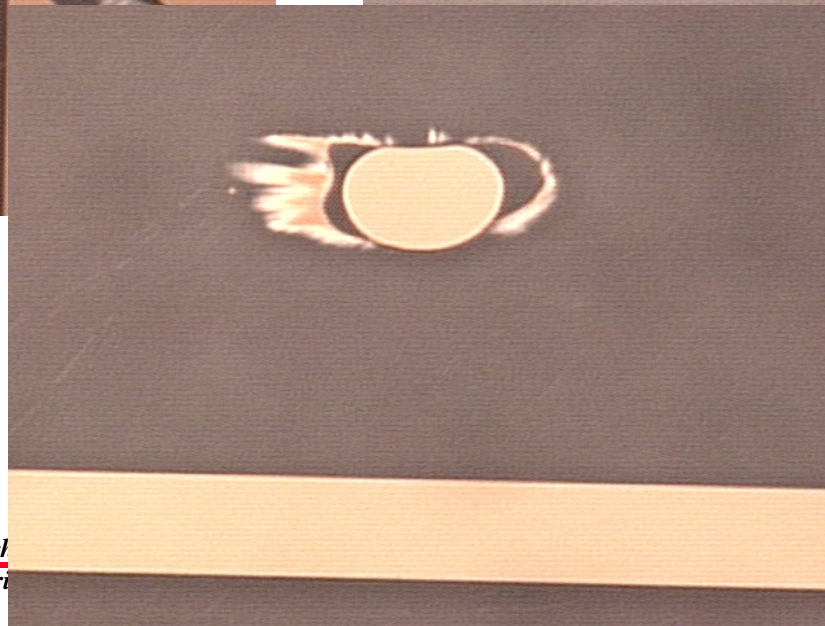
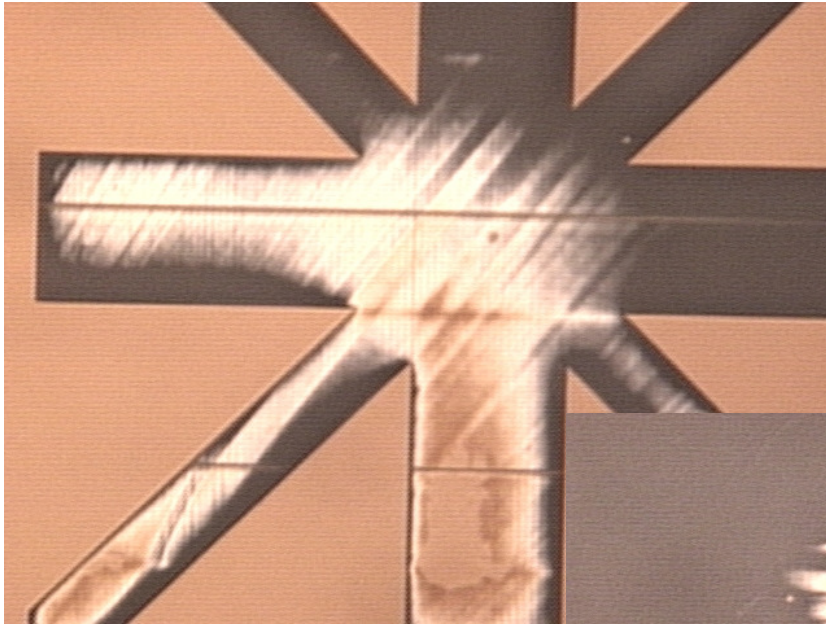
WHAT IS WRONG WITH THIS DIGITAL CIRCUIT



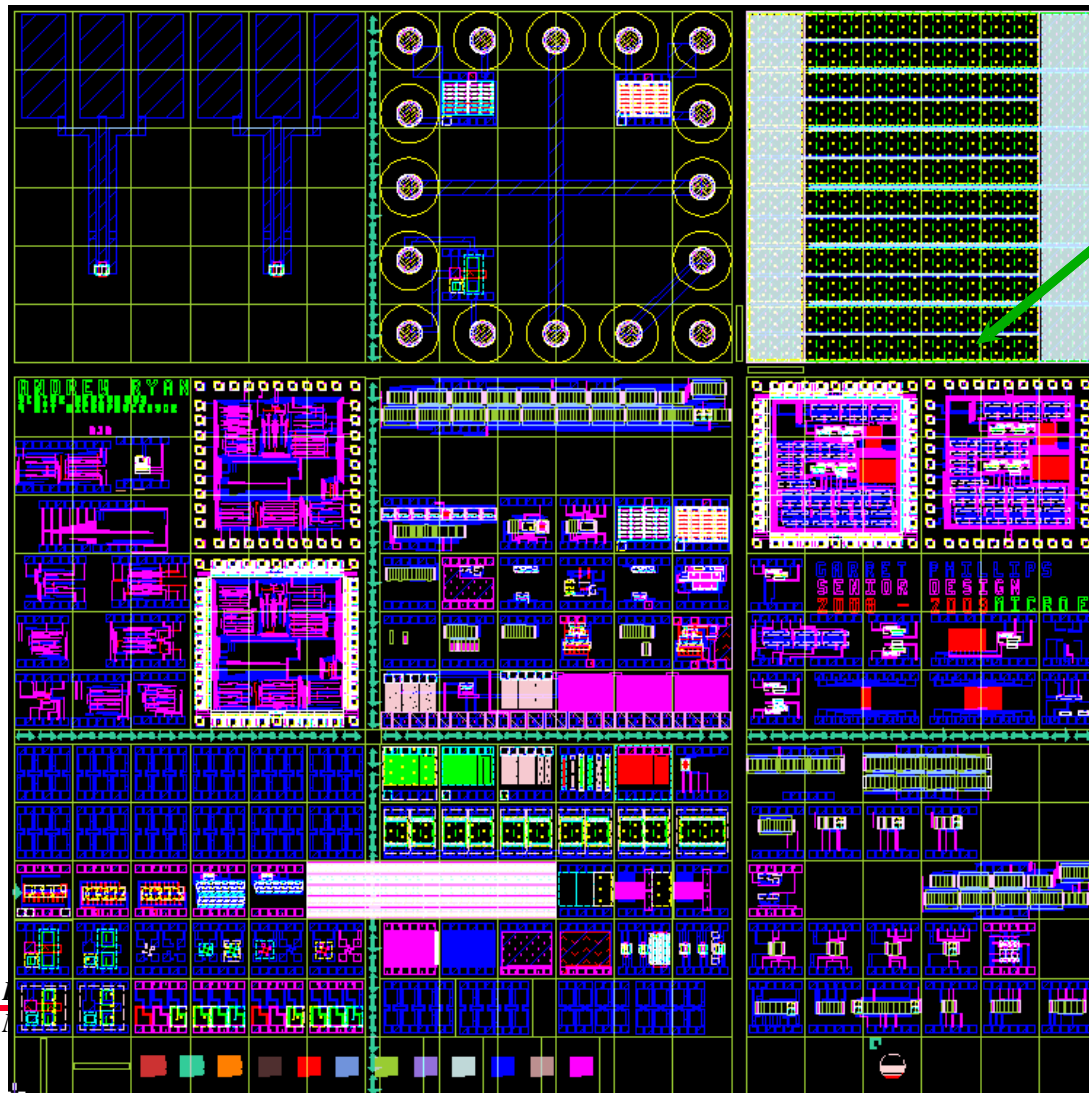
Design Errors – Missing Contact Cuts



MASK DEFECTS



JOHN GALT CMOS TESTCHIP

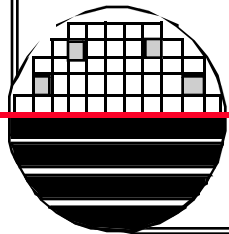
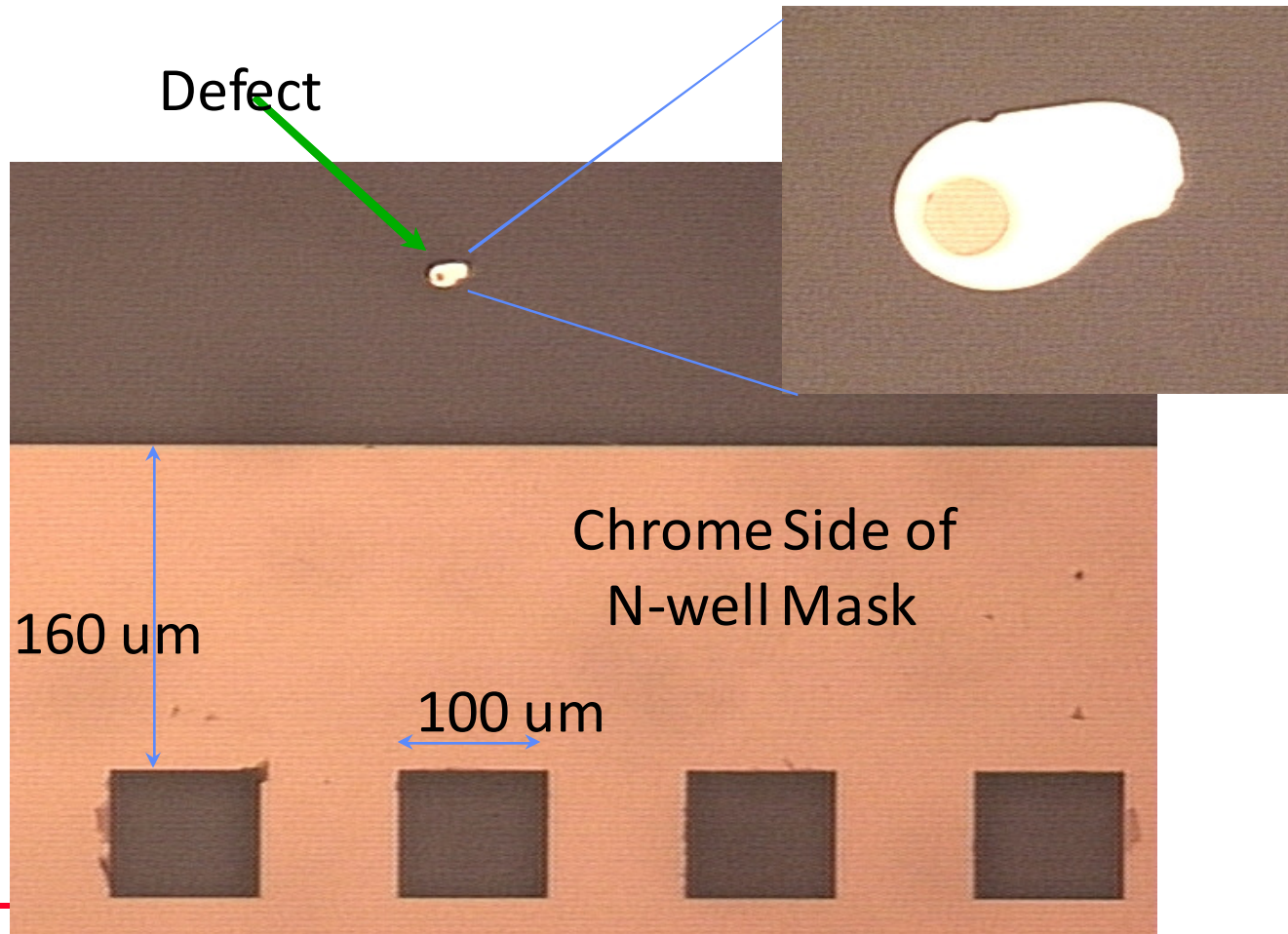


Defect

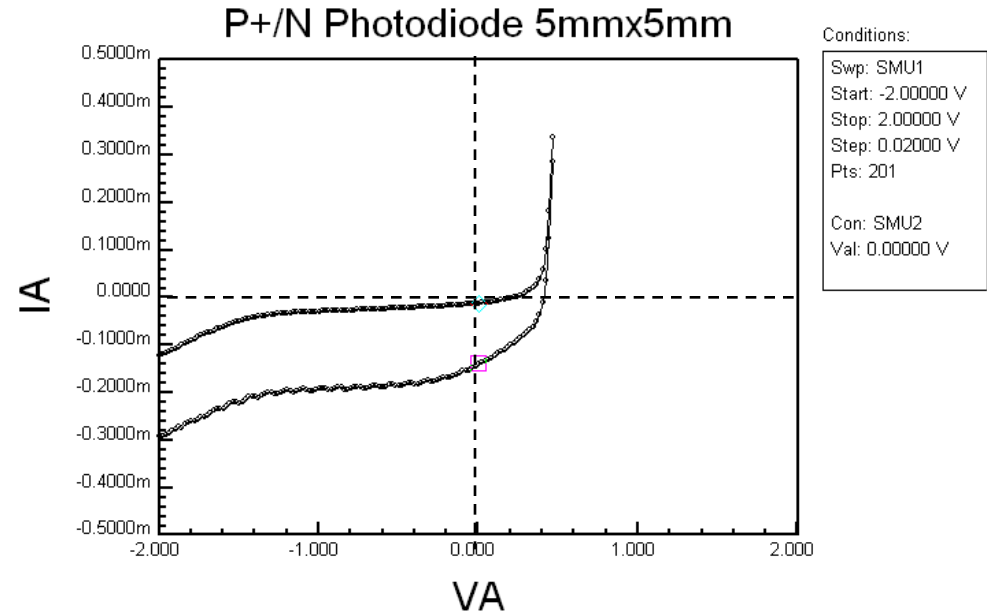
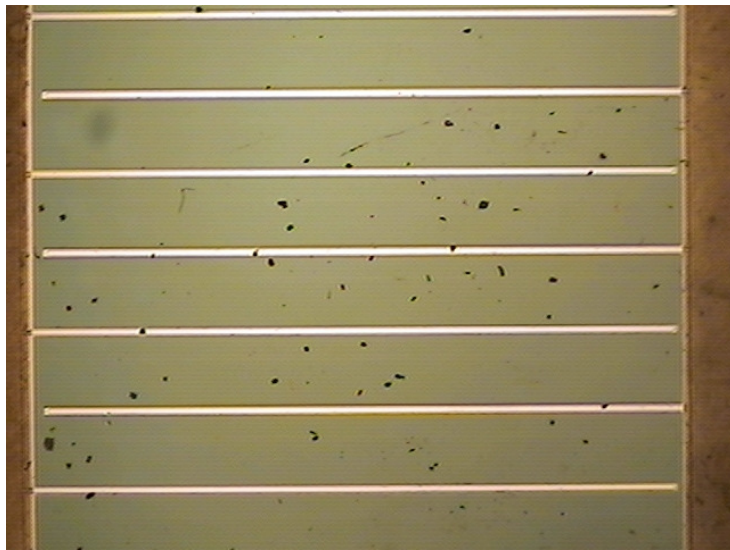
2010

MASK DEFECT

This defect will cause a short through the pn junction of our solar cell.



LARGE 5mm X 5mm PHOTODIODE

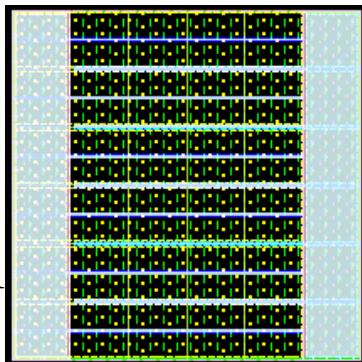


Conditions:
 Swp: SMU1
 Start: -2.00000 V
 Stop: 2.00000 V
 Step: 0.02000 V
 Pts: 201
 Con: SMU2
 Val: 0.00000 V

Fit #1:	Fit #2:	Cursors: X Y		
None	None	□	0.00000	-0.14080m
****	****	◇	0.00000	-0.01383m
****	****	○		
***	***	⊗		
		⊗		
		△		

ICS 13:46:58 11/18/2009

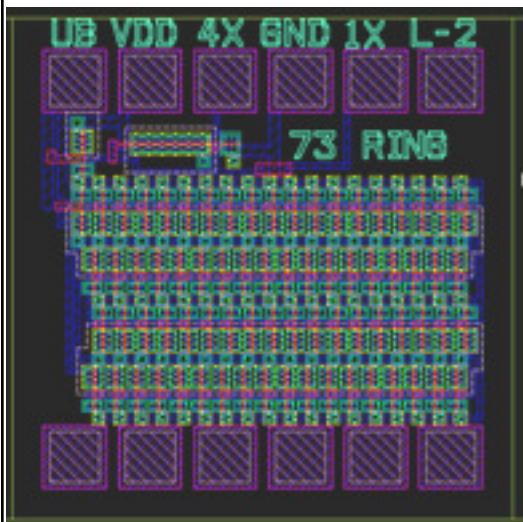
5mm
X
3.33mm



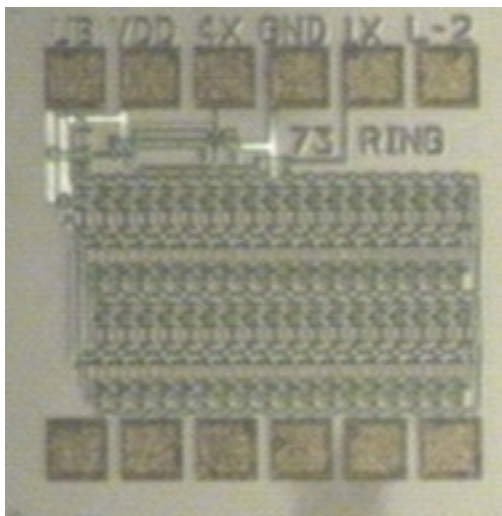
Isc = 0.15mA (short circuit current)
 or 9.09 A/m²

73 STAGE RING OSCILLATOR

The Ring Oscillator Works
Is It Working Correctly?

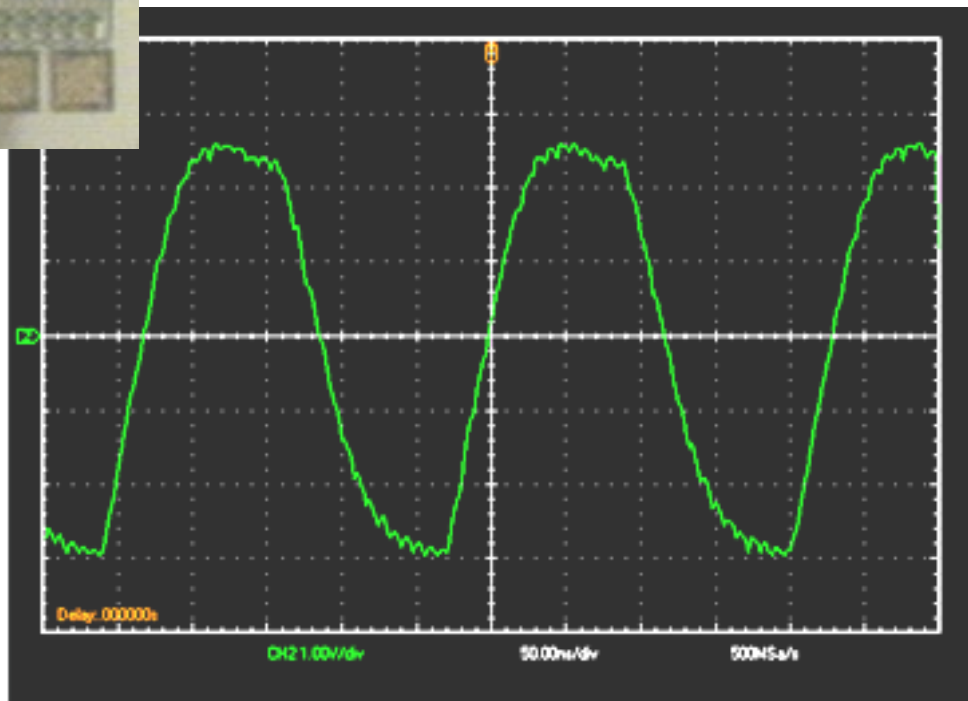


Design



Photo

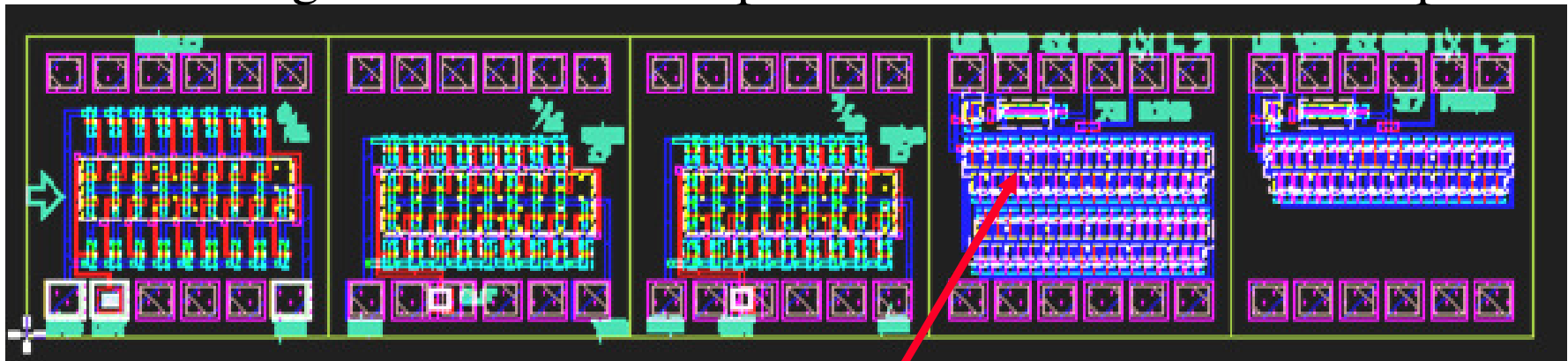
Electrical Test Results



73 Stage
4X Buffer
L=2 μ m
5Volt Supply
Frequency = 4.37MHz
Period = $T = 2 N t_d = 230$ ns
 $t_d = 1.58$ ns

RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output L/W=2/30 Buffered Output



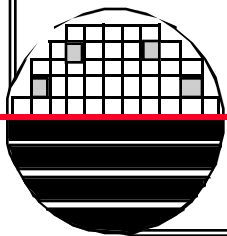
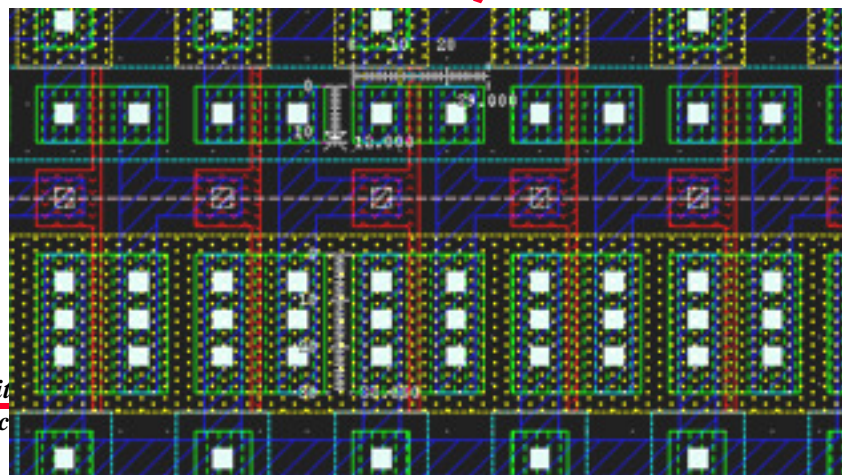
L/W 8/16

4/16

2/16

73 Stage

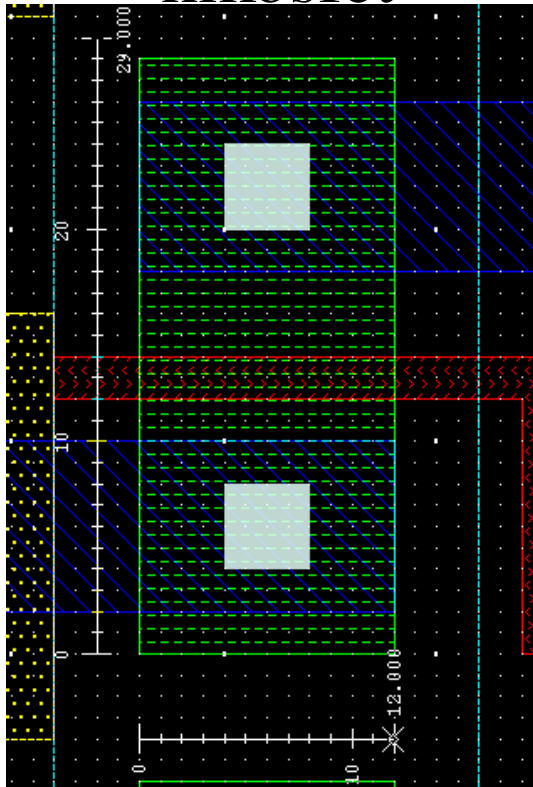
37 Stage



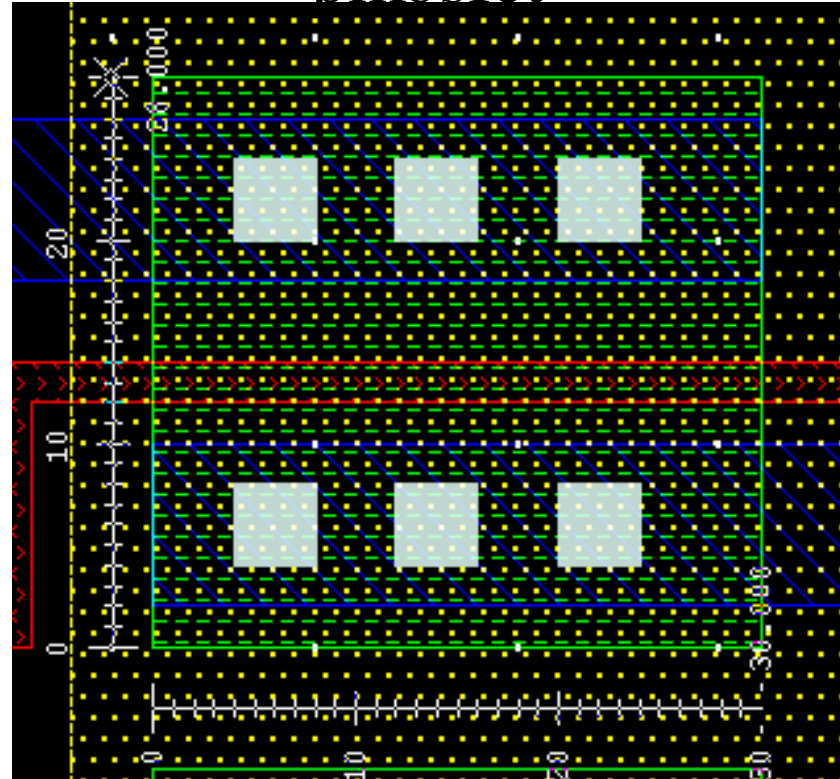
Rochester Institut
Microelectronic

MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

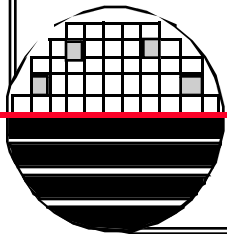
nmosfet



pmosfet



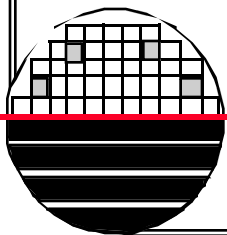
73 Stage Ring Oscillator



FIND DIMENSIONS OF THE TRANSISTORS

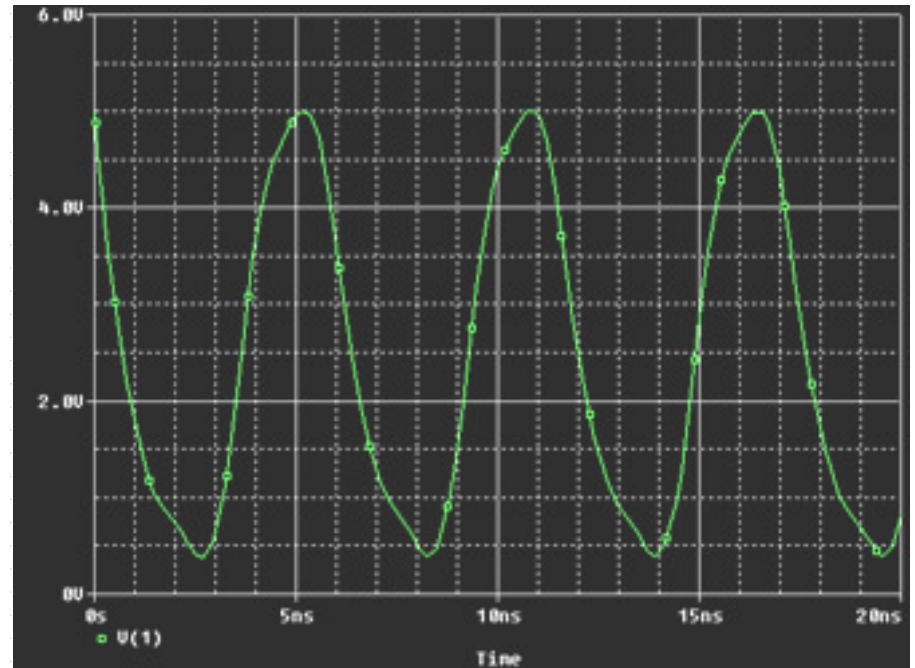
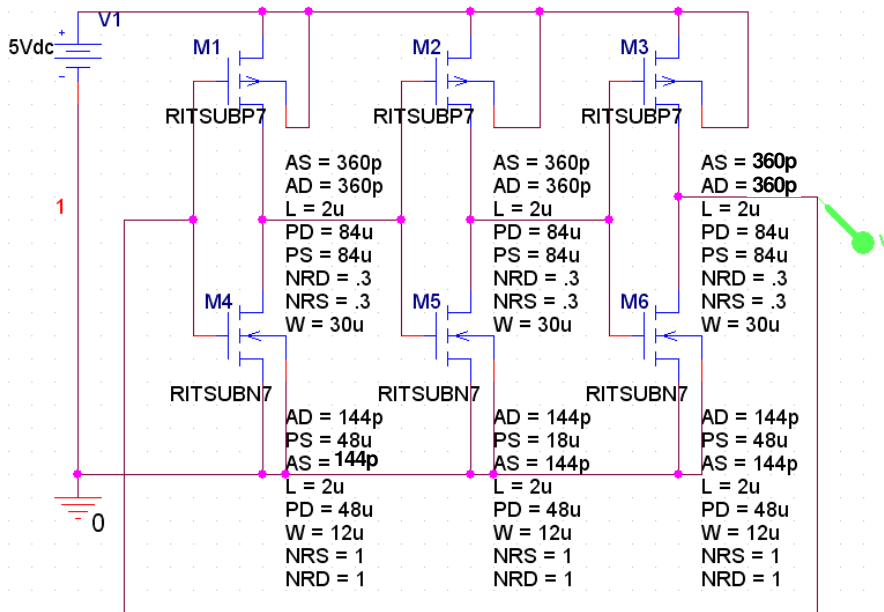
	NMOS	PMOS
L	2u	2u
W	12u	30u
AD	$12u \times 12u = 144p$	$12u \times 30u = 360p$
AS	$12u \times 12u = 144p$	$12u \times 30u = 360p$
PD	$2 \times (12u + 12u) = 48u$	$2 \times (12u + 30u) = 84u$
PS	$2 \times (12u + 12u) = 48u$	$2 \times (12u + 30u) = 84u$
NRS	1	0.3
NRD	1	0.3

73 Stage



Use Ctrl Click on all NMOS on OrCad Schematic
 Use Ctrl Click on all PMOS on OrCad Schematic
 Then Enter Dimensions

SIMULATED OUTPUT AT 5 VOLTS

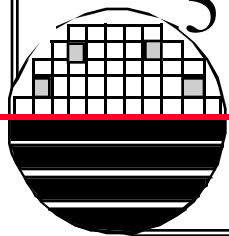


Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts

Measured $t_d = 1.580 \text{ nsec @ } 5 \text{ V}$

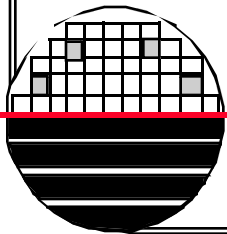
$$t_d = T / 2N = 5.5\text{nsec} / 2 / 3$$

$$t_d = 0.92 \text{ nsec}$$



REFERENCES

1. Dr Fuller's webpage on CMOS testing,
<http://people.rit.edu/lffeee/CMOS.htm>
2. other



HOMEWORK

1. Problem 1
2. other

