

**ROCHESTER INSTITUTE OF TECHNOLOGY  
MICROELECTRONIC ENGINEERING**

# Surface MEMS Fabrication Details

**Dr. Lynn Fuller, Adam Wardas**

Webpage: <http://people.rit.edu/lffeee>

Microelectronic Engineering  
Rochester Institute of Technology  
82 Lomb Memorial Drive  
Rochester, NY 14623-5604  
Tel (585) 475-2035

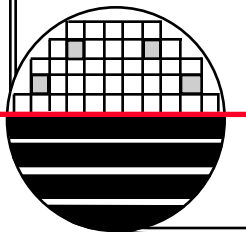
Email: [Lynn.Fuller@rit.edu](mailto:Lynn.Fuller@rit.edu)

Department webpage: <http://www.microe.rit.edu>

10-30-2014 SurfaceMEMsFabricationDetails.ppt

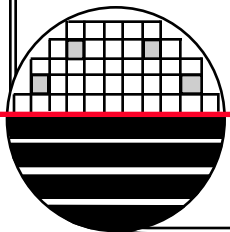
*OUTLINE*

Introduction  
Device Cross Section  
Maskmaking  
Stepper Jobs  
Fabrication Details  
Signal Processing  
Testing  
Summary  
References  
Homework



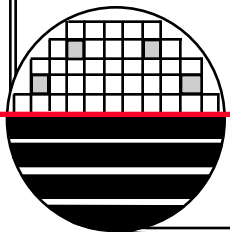
# *INTRODUCTION*

This document provides detailed information on RIT's surface micromachine process. This process is capable of making many different types of MEMS devices. This MEMS fabrication process is CMOS compatible (with some modifications) back end module that can be added to realize compact microsystems (CMOS plus MEMS).

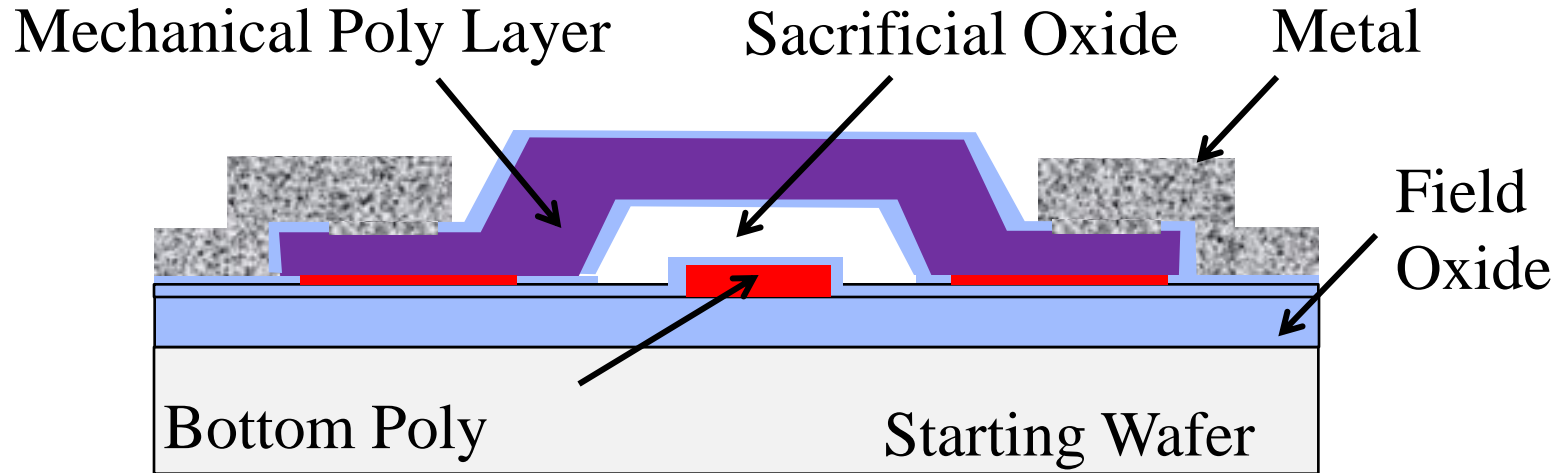


*LIST OF MEMS DEVICES MADE WITH THIS PROCESS*

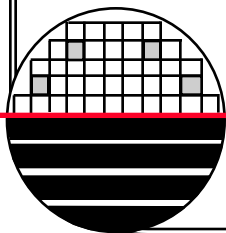
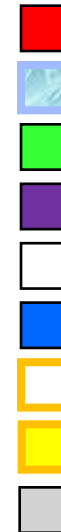
Resistors – Micro Bolometer  
Heaters – Chemical Sensors  
Micro Mirror - Two Axis Mirror  
Thermally Actuated Two Arm Cantilever  
Chevron Actuators  
Electrostatic Comb Drive  
MEMS Switch  
Accelerometer  
Gas Flow Sensor, Anemometer, Thermionic  
Light Modulator  
Bio Probes  
Speaker  
Humidity Sensors  
Pressure Sensors - Microphone  
Temperature Sensors – Thermopile, Resistor  
Inductors, Capacitors – Humidity Sensor  
Hall Effect Sensors – other Magnetic Field Sensors



***DEVICE CROSS SECTION***



- Bottom Poly 1 (Red) Layer 1
- Sacrificial Oxide (Blue Outline) Layer 2
- Anchor (Green) Layer 3
- Mechanical Poly 2 (Purple) Layer 4
- Contact Cut (White) Layer 6
- Metal (Blue) Layer 7
- Outline (Yellow Outline) Layer 9
- No Implant Yellow Layer 15
- Holes Layer 16 (combined with Poly 2)

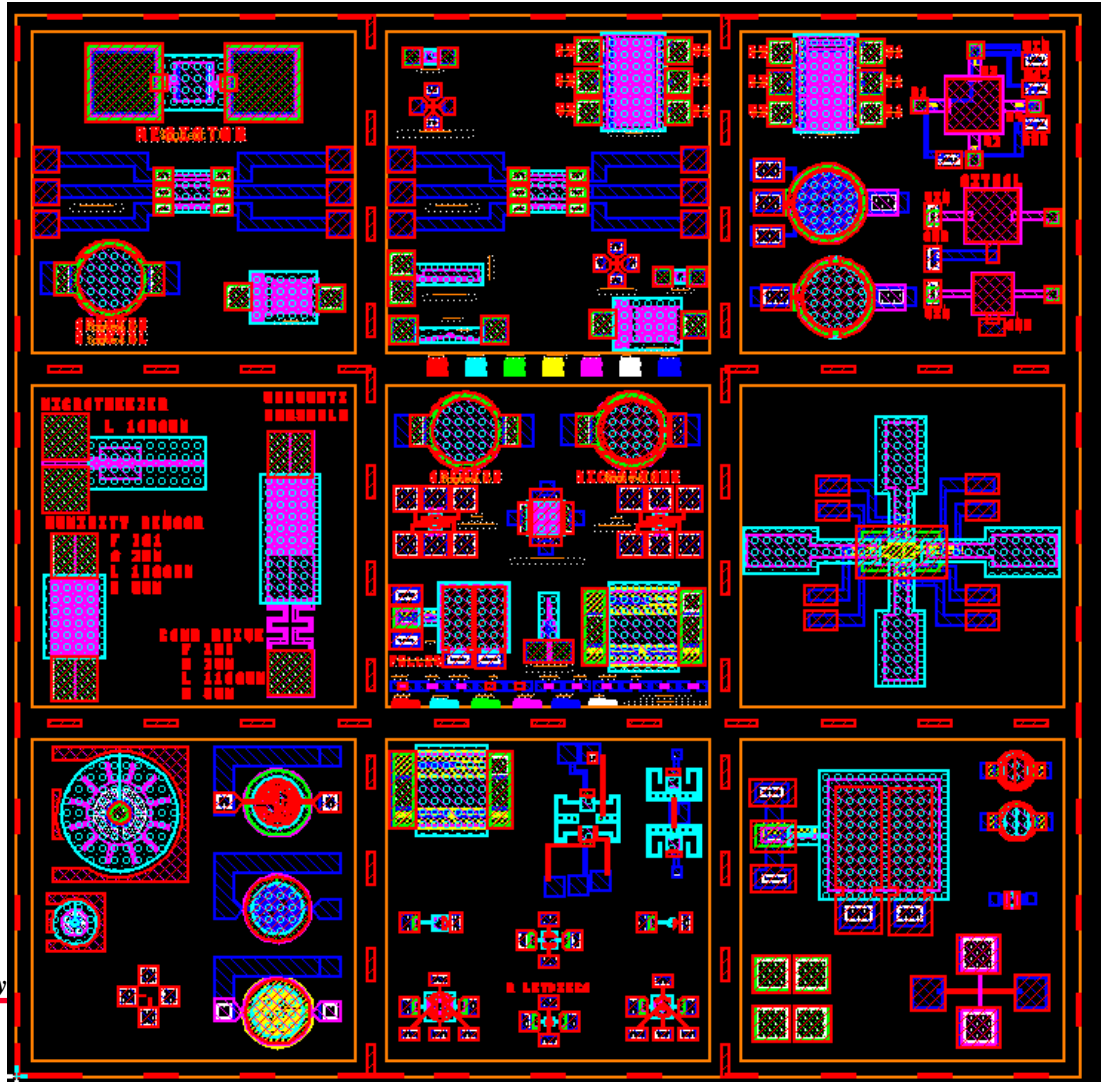


# 2014 MEMS MULTICHIP PROJECT DESIGN

Total 15 mm by 15 mm plus 500 um for sawing into 9 chips for overall 16.5mm by 16.5mm size.

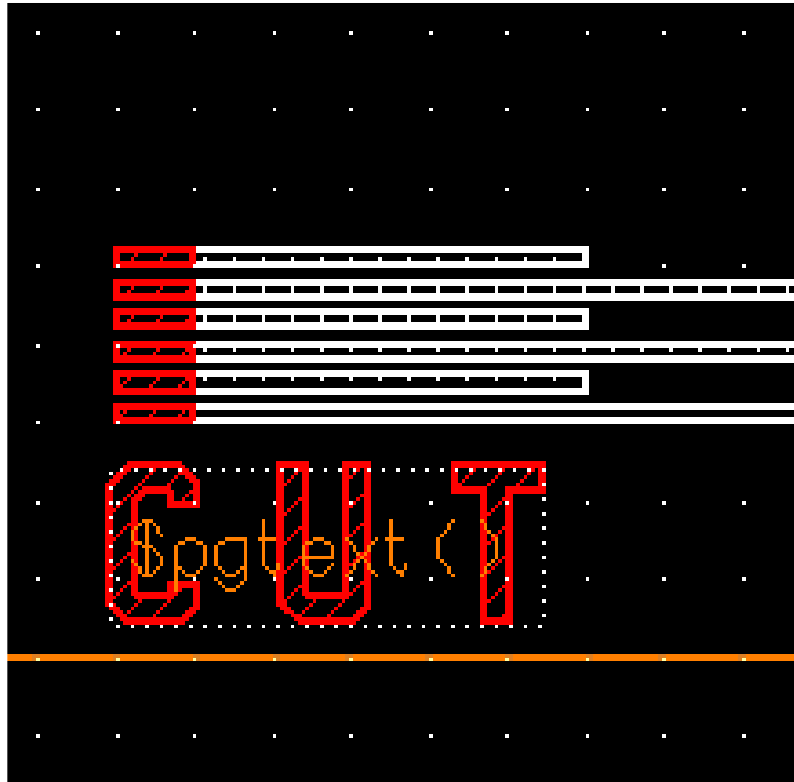
Wafer sawing is easier if all chips are the same size

5mm by 5mm design space for each project

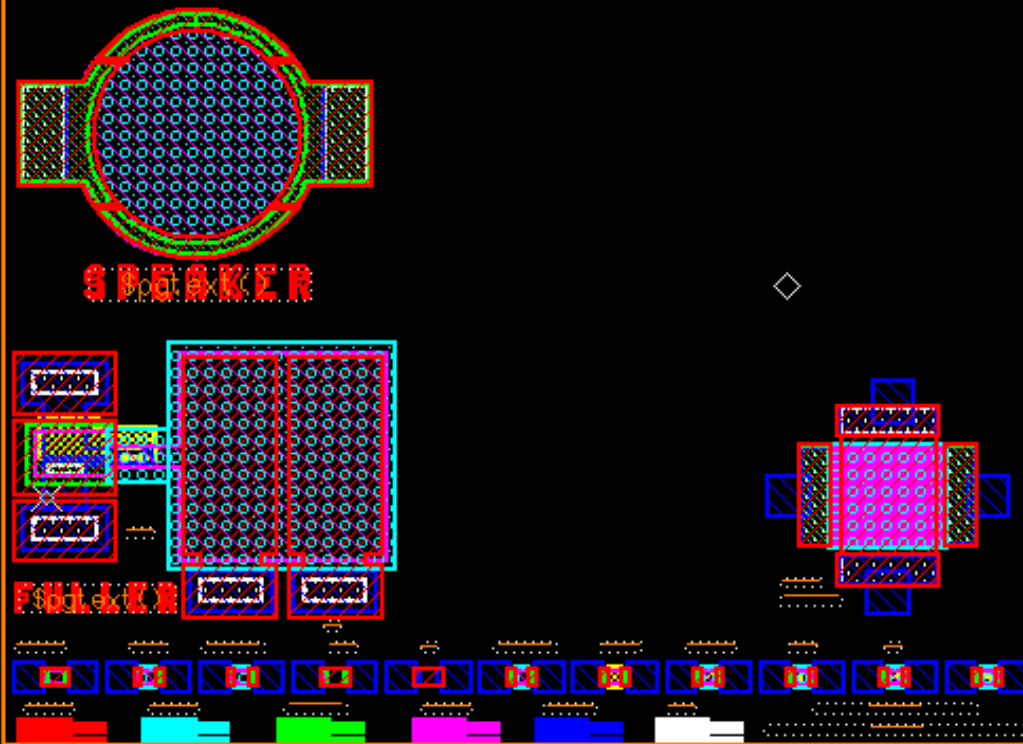


Rochester Institute of Technology  
Microelectronic Engineering

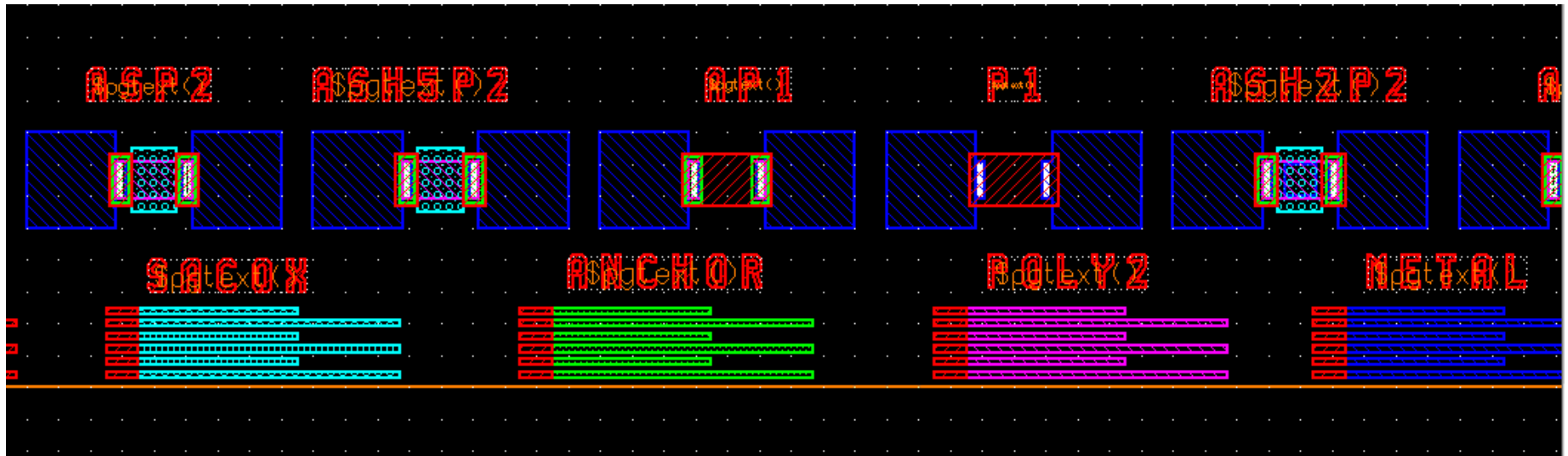
# TEST STRUCTURES



One of the cells will have test structures along the bottom edge for resolution/overlay, etc.



TEST STRUCTURES

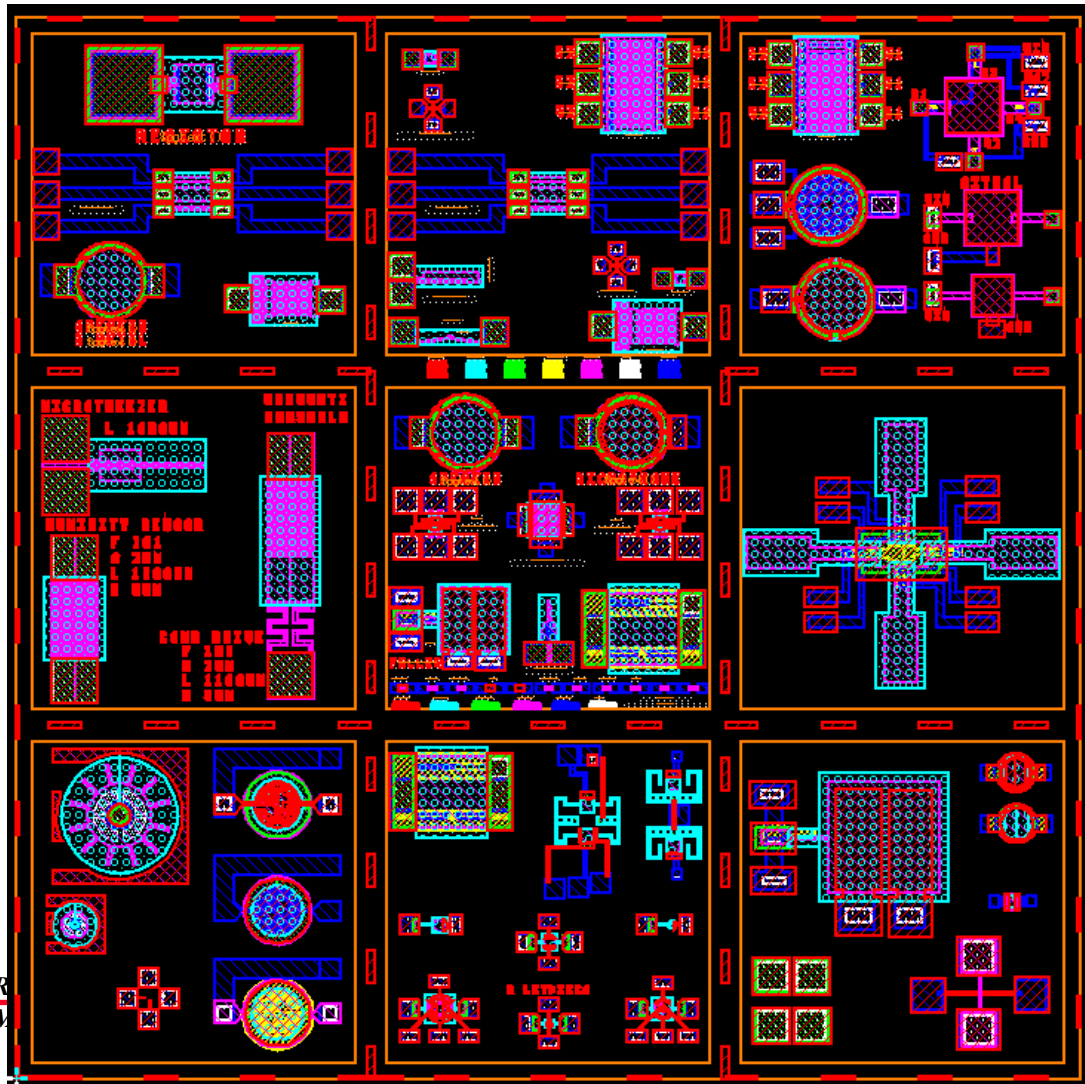


1. Poly1 in Parallel with Poly2
2. No Etch Holes Poly 2
3. 5um Etch Holes Poly2
4. Metal contact to Poly2 to Poly1
5. Metal contact to Poly1
6. 2um Etch Holes Poly2
7. Poly2 No Implant, No SacOx
8. Poly2 No Implant
9. Poly2 No Implant 5um Gap
10. Poly2 No Implant 5um Resistor
11. Poly 2 No Implant 10um Resistor

Starting from Left Resistors  
 $L = \sim 100\mu\text{m}$   $W = \sim 50\mu\text{m}$



# 2014 MEMS MULTICHIP PROJECT DESIGN



## GDS II LAYER NUMBERS

The design layer names and colors are lost when converting to GDS II. Only the layer number is kept.

Individual Student Designs are converted to GDS-II files and emailed to course instructor.

Layer	Layer Number	Prev	S	V	F
poly1	1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SacOx	2		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Anchor	3		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Poly2	4		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Metal	7		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Out	9		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Cut	6		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
No_Implant	15		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Holes	16		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

# MASK ORDER FORM

Rochester Institute of Technology  
Semiconductor & Microsystems Fabrication Laboratory

Maskmaking  
Order Request

Name  
Company  
Department  
Street Address  
City, State and Zip Code  
Phone Number  
SMFL Project Code  
Email Address  
  
Order Date  
Order Due Date

**Dr Fuller  
RIT**

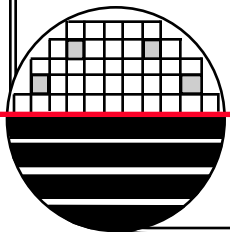
Design File Name (.gds)	<b>mems-2014-final.gds</b>
Number of Mask Levels to be Written	<b>7</b>
Cell Layout Size	<b>16.5mm x 16.5mm</b>
Name of Cell in Design File to be used	<b>mems-2014-final</b>

Mask Type Needed			
<input type="checkbox"/> Contact Aligner	Defaults	Scale:	1X
• Max field size - 105mm x 105mm		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror 90
		Fracture Resolution:	0.5um
<input type="checkbox"/> GCA Stepper	Defaults	Scale:	5X
• Max field size - 20mm x 20mm		Mask Size:	5" x 5" x 0.09" Soda Lime
		Orientation:	Mirror 135
		Fracture Resolution:	0.5um
<input checked="" type="checkbox"/> ASML Stepper	Defaults	Scale:	5X
Max field size - 22mm x 22mm		Mask Size:	6" x 6" x 0.12" Quartz
		Orientation:	Mirror 90
		Fracture Resolution:	0.5um

<input type="checkbox"/> Single Field Array Plate	<input type="checkbox"/> Yes
	<input type="checkbox"/> Array with _____ columns (x) and _____ rows (y)
Array element size	X: _____ um Y: _____ um

**Notes:**  
If multiple design files are to be incorporated into your array - please specify the array layout separately  
Your designs will be butted together to form the array unless otherwise specified

<input type="checkbox"/> Multiple Field Array Plate	<input type="checkbox"/> Yes
Numbers of Levels on Plate	_____
Please specify which levels are to be grouped together on which plate on the Details Sheet	



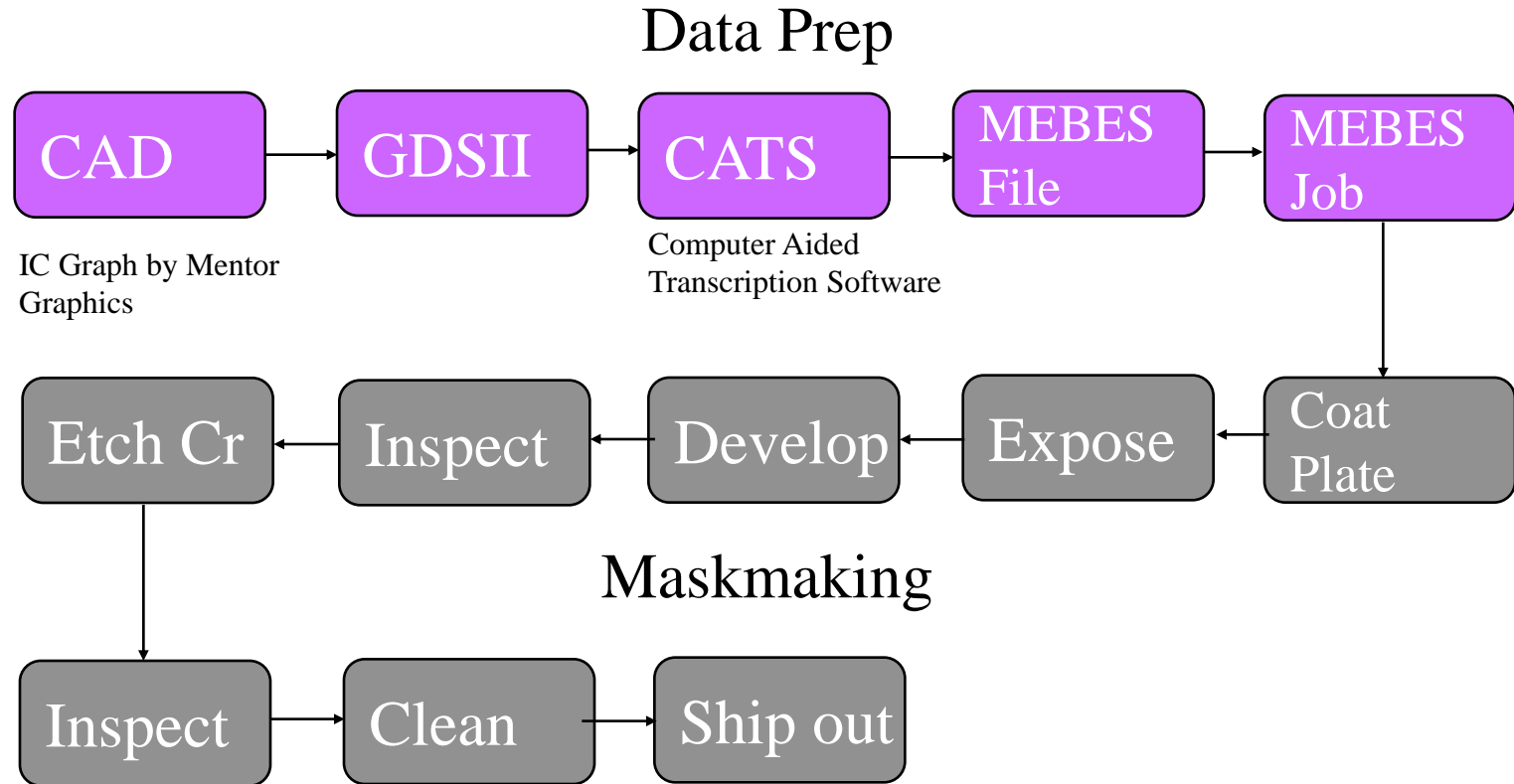
Rochester Institute of Technology  
Microelectronic Engineering

***MASK ORDER FORM DETAILS***

Reticle Number	Reticle Name	Design Layer #'s	Boolean Function	Dark/Clear	Comment
1	Poly1	1	None	Clear	
2	SacOx	2	None	Clear	
3	Anchor	3	3 Inverted	Dark	
4	No Implant	15	None	Clear	
5	Poly2	4,16	4 AND (16 Inverted)	Clear	
6	Cut	6	6 Inverted	Dark	
7	Metal	7	None	Clear	

Design Layer 9 Out (outline) is not used. It is only for placement of projects on the multi-project reticle template.

# MASK PROCESS FLOW



This process can take weeks and cost between \$1000 and \$20,000 for each mask depending on the design complexity.

*MEBES - Manufacturing Electron Beam Exposure System*



*Rochester Institute of Technology  
Microelectronic Engineering*



*ASML RETICLE*



Chrome Side  
Mirrored 90°  
Chip Bottom at Bottom



Non Chrome Side  
As loaded into Reticle Pod,  
Chrome Down, Reticle Pre-  
Alignment Stars Sticking out  
of Pod

***POSSIBLE NEW PROCESSES (NEED VERIFICATION)***

Can we make isolated poly resistors by ion implant?  
Sacrificial Oxide Etch Holes, Size, Spacing,

Sacrificial Oxide Etch Stop (poly) and Oxidation  
Mechanical Poly Layer Deposition

Mechanical Poly Layer Etch Recipe (STS Tool)

Thick Resist Coat, Develop, Expose Recipes

Use Stepper Job SMFL-ETM and Photomask

ETM Senior Test

1827 Resist, 2500 rpm, 110°C

4.1µm Thickness

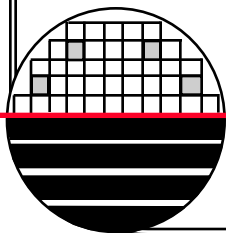
400mj/cm<sup>2</sup> Focus +2µm

Develop same as DEVCC no hard bake

Metal Lift-Off

Sawing Recipes....

Release Sequence, Details,





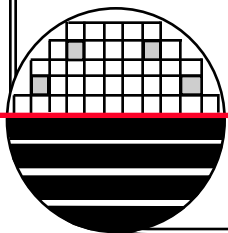
## *SURFACE MEMS 2014 PROCESS*

1. Starting wafer
2. PH03 – level 0, Marks
3. ET29 – Zero Etch
4. ID01-Scribe Wafer ID, D1...
5. ET07 – Resist Strip, Recipe FF
6. CL01 – RCA clean
7. OX04 – 6500Å Oxide Tube 4
8. CV01 – LPCVD Poly 5000Å
9. PH03 – level 1 Poly-1
10. ET08 – Poly Etch
11. ET07 – Resist Strip, Recipe FF
12. CL01- RCA clean 2 HF dips
13. CV01- LPCVD Poly 1000Å
14. IM01-P31 2E16 100KeV
15. OX04 – Anneal Recipe 119
16. CV03-TEOS SacOx Dep 1.5um
17. PH03-level 2 SacOx
18. ET06-wet etch SacOx
19. ET07- Resist Strip, Recipe FF
20. CV03-TEOS Etch Stop
21. PH03-Level 3 Anchor-Thick Resist
22. ET06-Wet Etch Oxide
23. ET07-Resist Strip Recipe FF
24. CV01-LPCVD Poly 1.5um
25. PH03-Level 4 No Implant
26. IM01-P31 2E16 100KeV
- 27; ET07 Resist Strip, Recipe FFF
28. OX04-Anneal Recipe 119
29. DE01 Four Point Probe
30. PH03-Level 5 Poly2
31. ET68-STs Etch
32. ET07 Resist Strip, Recipe FFF
33. ET66-SacOx Etch
34. OX05-Consume Etch Stop Poly
35. PH03-Level 6 CC
36. ET06- wet etch BOE
37. ET07 Resist Strip, Recipe FFF
38. CL01-Special
39. ME01 – Sputter Aluminum
40. PH03-Level 7, Metal
41. ET15 – plasma Al Etch
42. ET07 – Resist Strip, Recipe FFF
43. SI01 – sinter Tube 2, Recipe ???
44. SEM1 – SEM Pictures
45. TE01 - Testing

*STARTING WAFER – SCRIBE ID01*



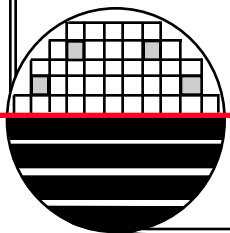
Starting Wafer



*SSI COAT AND DEVELOP TRACK FOR 6" WAFERS*



Use Recipe: MEMSCOAT.rcp and MEMSDEV.rcp

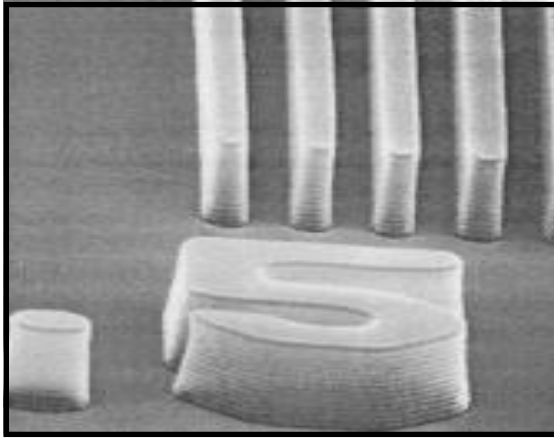


**RECIPES FOR RESIST COAT AND DEVELOP**

Level	Level Name	Resist	Coat Recipe	Develop Recipe	Resist Thickness
0	Zero	OIR-620	Coat	Develop	1.0um
1	Poly 1	OIR-620	Coat	Develop	1.0um
2	Sac Ox	OIR-620	Coat	Develop	1.0um
3	Anchor	S1827	MEMS-COAT	MEMS-DEV	4.5um
4	Poly 2	S1827	MEMS-COAT	MEMS-DEV	4.5um
5	CC	S1827	MEMS-COAT	MEMS-DEV	4.5um
6	Metal 1	S1827	MEMS-COAT	MEMS-DEV	4.5um

MEMSCOAT.rcp 2500rpm, 30sec, Hand Dispense, 110°C, 1min  
 Exposure for S1827, 400mj/cm<sup>2</sup>, Focus +2.0, NA=0.46,  $\sigma=0.45$   
 MEMSDEV.rcp has 200 second develop time, no hardbake

*ASML 5500/200*

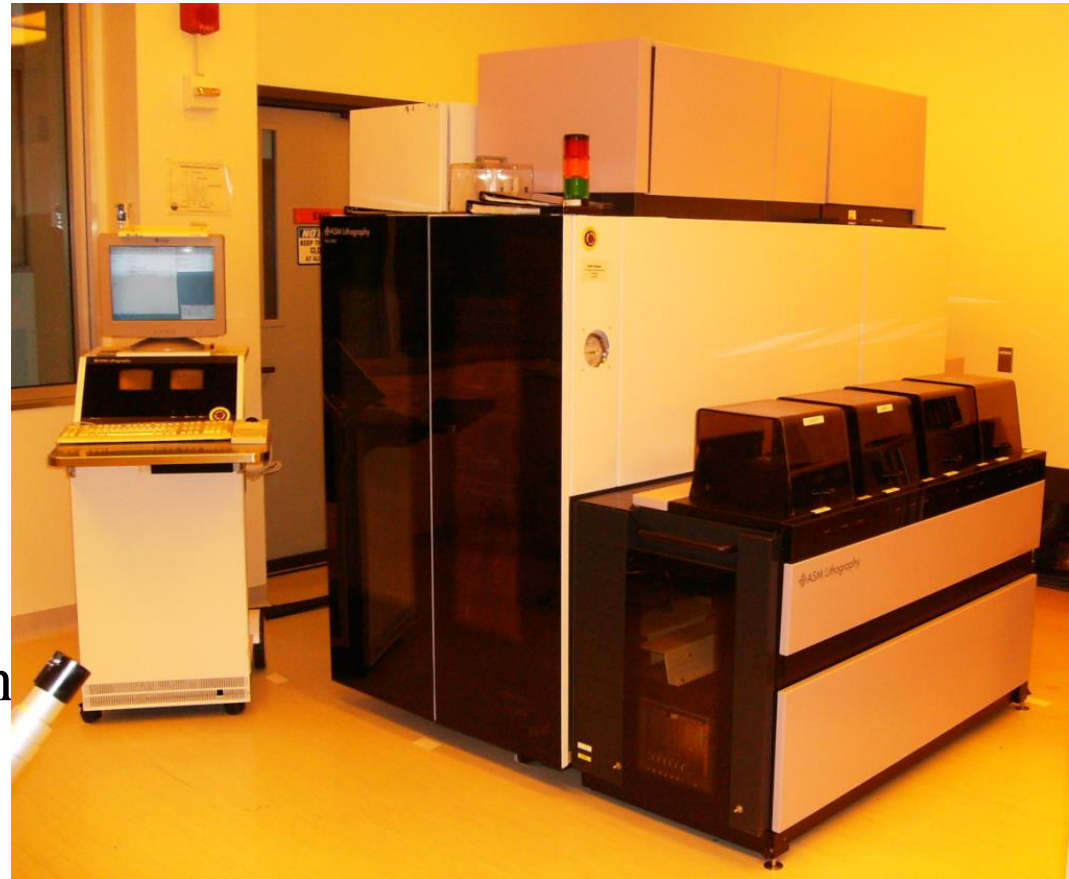


NA = 0.48 to 0.60 variable  
 $\sigma = 0.35$  to  $0.85$  variable  
With Variable Kohler, or  
Variable Annular illumination

$$\text{Resolution} = K_1 \lambda / \text{NA}$$
$$= \sim 0.35 \mu\text{m}$$

for NA=0.6,  $\sigma = 0.85$

$$\text{Depth of Focus} = k_2 \lambda / (\text{NA})^2$$
$$= 1.0 \mu\text{m for NA} = 0.6$$



i-Line Stepper  $\lambda = 365 \text{ nm}$   
22 x 27 mm Field Size

***STEPPER JOB***

Mask Barcode:

Stepper Jobname: MCEE770-MEMS

Level 0 (combi reticle)

Level Clearout (combi reticle)

Level SacOx

Level Poly 1

Level Anchor

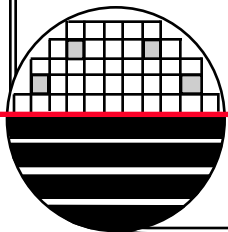
Level Poly 2

Level CC

Level Metal

Level No Implant

Level MEMS-Test (no alignment)





*DRYTEK QUAD RIE TOOL*

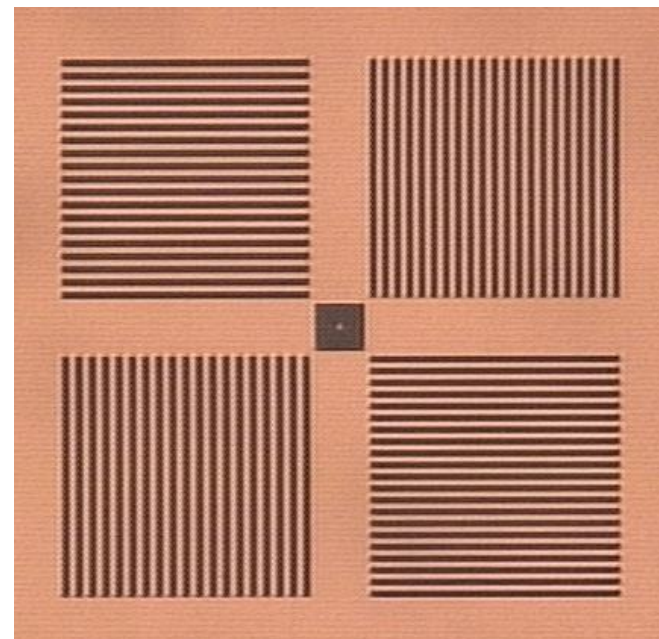


# ZERO ETCH FOR ASML ALIGNMENT MARKS

Recipe Name: ZEROETCH  
Chamber 3  
Power 200W  
Pressure 100 mTorr  
Gas 1 CHF3 50 sccm  
Gas 2 CF4 25 sccm  
Gas 3 Ar 0 sccm  
Gas 4 O2 10 sccm

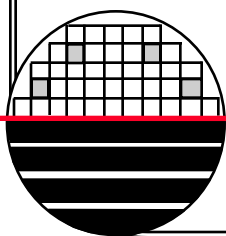
Max Time = 120 seconds

Silicon Etch Rate 650 Å/min



8.8 um L/S

8 um L/S





# ASHER, SCRIBE, RCA CLEAN & SRD

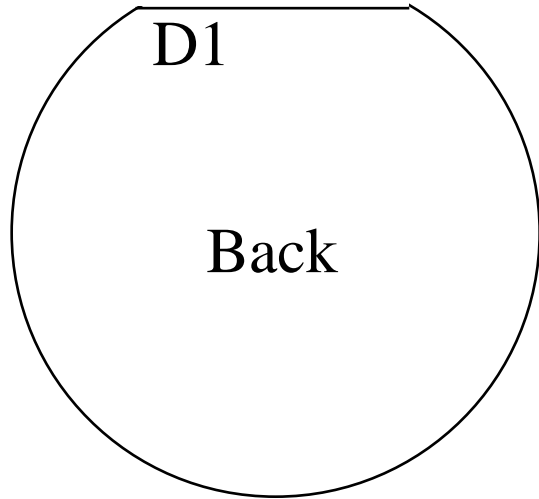
$O_2 + \text{Energy} = 2 O$   
O is reactive and will combine  
with plastics, wood, carbon,  
photoresist, etc.



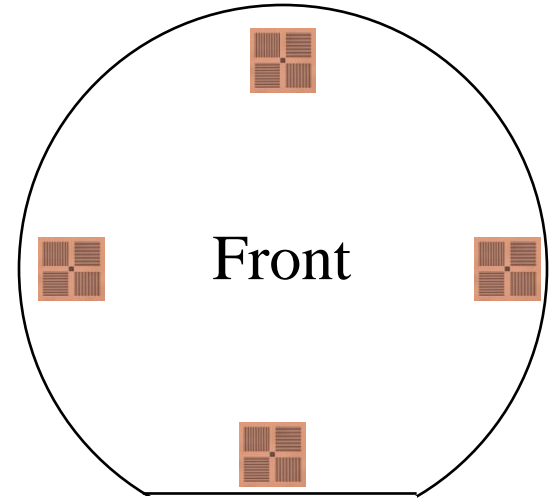
Gasonics Asher  
Recipe FFF

RCA Clean Bench

***SCRIBE WAFER WITH ID NUMBER***



Scribe on back of wafer  
near the wafer flat  
ID numbers D1, D2...etc.



Wafer has alignment marks etched in four locations

**RCA CLEAN**

**APM**

NH<sub>4</sub>OH - 1part  
H<sub>2</sub>O<sub>2</sub> - 1parts  
H<sub>2</sub>O - 17parts  
70 °C, 15 min.

DI water  
rinse, 5 min.

H<sub>2</sub>O - 50  
HF - 1  
30 sec.

**HPM**

HCL - 1part  
H<sub>2</sub>O<sub>2</sub> - 1parts  
H<sub>2</sub>O - 17parts  
70 °C, 15 min.

DI water  
rinse, 5 min.

DI water  
rinse, 5 min.

SPIN/RINSE  
DRY

## USING EXCEL SPREADSHEET FOR OXIDE GROWTH CALCULATIONS

A	B	C	D	E	F	G	H	I	J
1	ROCHESTER INSTITUTE OF TECHNOLOGY				OXIDE.XLS				
2	MICROELECTRONIC ENGINEERING				7/4/2014				
3									
4	CALCULATION OF OXIDE THICKNESS				Dr. Lynn Fuller / Jamie Wasiewicz				
5									
6	To use this spreadsheet change the values in the white boxes. The rest of the sheet is								
7	protected and should not be changed unless you are sure of the consequences. The								
8	calculated results are shown in the purple boxes. O2 bubbled through warm water is "wet",								
9	burning H2 with O2 is called "steam"								
10									
11	CONSTANTS			VARIABLES			CHOICES		
12	K	1.38E-23 J/K					1=yes, 0=no		
13	(Bo/Ao) dry	6230000 μm/hr		Temp =	1100 °C		wet	0	
14	Ea (dry)	2 eV		time =	65 min		dry	0	
15	(Bo/Ao) wet	89500000 μm/hr		Partial Pressure, p =	1.00 Atm		steam	1	
16	Ea (wet)	2.05 eV					<100>	1	
17	(Bo/Ao) steam	1.63E+08 μm/hr					<111>	0	
18	Ea (steam)	2.05 eV							
19	Bo dry	7.72E+02 μm <sup>2</sup> /hr		Xint =	0 Å				
20	Ea (dry)	1.23 eV							
21	Bo wet	2.14E+02 μm <sup>2</sup> /hr		Silicon VLSI Technology, Plummer, Deal, Griffin					
22	Ea (wet)	0.71 eV		Prentice Hall, 2000, pg 319-369					
23	Bo steam	3.86E+02 μm <sup>2</sup> /hr							
24	Ea (steam)	0.78 eV		(Bo/Ao)/1.68 for <100>					
25									
26	CALCULATIONS:								
27									
28	Xox (Oxide thickness)=(A/2){[1+(t+Tau)4B/A^2]^0.5 - 1} =				6765 Å				
29									
30	B = [Bo exp (-Ea/KTemp)]*p	0.5338344 μm <sup>2</sup> /hr							
31	B/A = [(Bo/Ao) exp (-Ea/KTemp)]*p	2.99E+00 μm/hr							
32	A	0.1784766 μm							
33	Tau = (Xi2+AXi)/B	0 hr							
34									
35									
36	Xox	↑ ↓		Oxide SiO2		←		Original Silicon Surface Prior to Oxide Growth	
37			Silicon				↑		0.46 Xox (silicon consumed)
38									
39									
40									
41									

These spreadsheets are available on Dr. Fullers webpage.

**BRUCE FURNACE RECIPE 406 – WET OXIDE 6,500Å**

**Recipe #406**

1100°C

Boat Out Load

Boat In Push

Stabilize

Ramp-Up

Soak

Anneal

Ramp-Down

Boat Out Pull

800 °C

800 °C

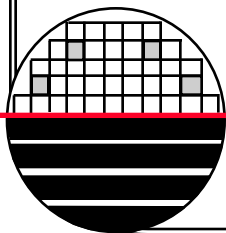
25 °C

Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7	Interval 8
Any	12 min	15 min	30 min	5 min	65 min	5 min	60 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	5 lpm	3.6/2 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	N2	O2	O2/H2	N2	N2	N2

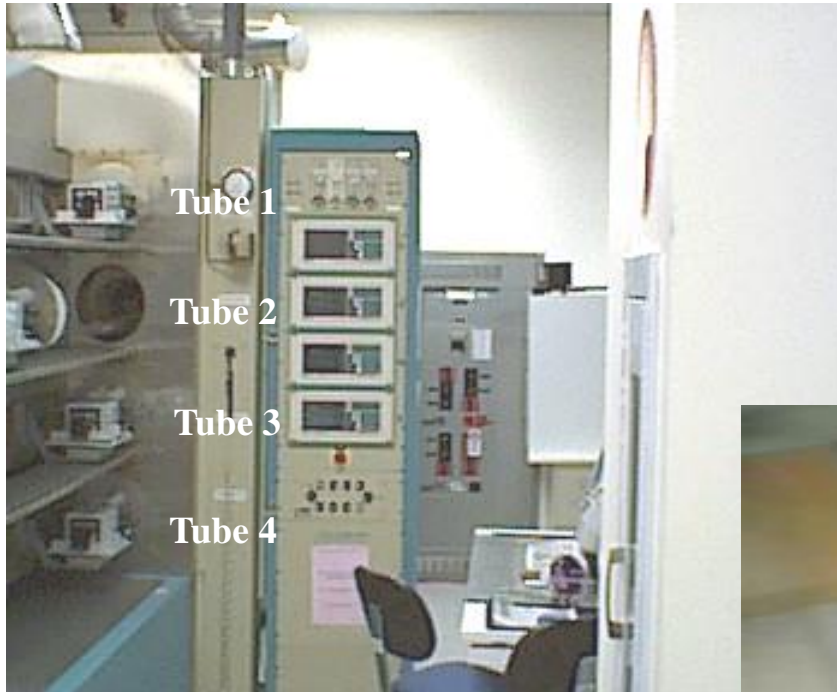
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

**Wet Oxide Growth, Target 6,500 Å**

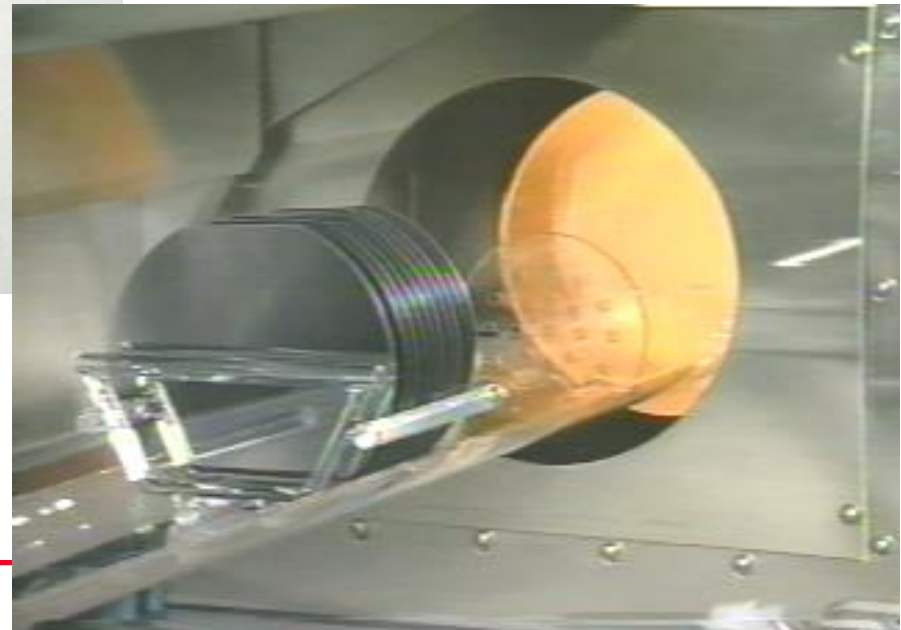
Rochester Institute of Technology  
Microelectronic Engineering



***BRUCE FURNACE***

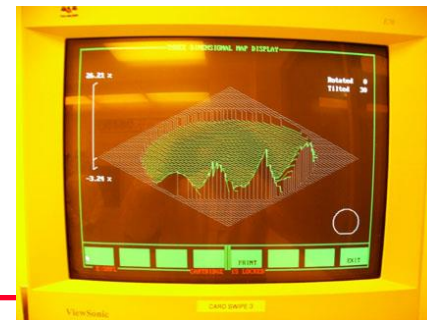
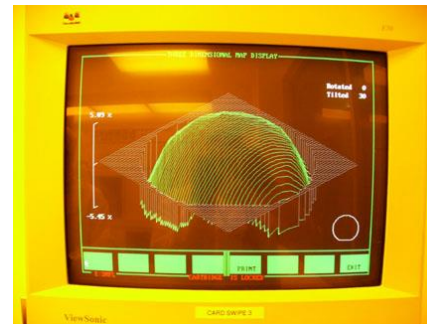


Tube 1 Steam Oxides  
Tube 2 P-type Diffusion  
Tube 3 N-type Diffusion  
Tube 4 Dry Oxides and Gate Oxides





*TENCORE FT-300 SPECROMAP*



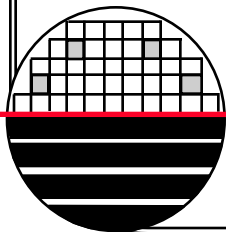
Record:

- Mean
- Std Deviation
- Min
- Max
- No of Points

*AFTER 6500Å OXIDE GROWTH*



Starting Wafer





*DEPOSIT POLYSILICON*

Poly Target 5000A  
LPCVD, 610C, Rate  $\sim 64\text{\AA}/\text{min}$   
Time  $\sim 78$  min

Recipe POLY 610  
Temp =  $610^{\circ}\text{C}$   
Pressure = 300 mTorr  
Silane Flow = 90 sccm

Substrate



*SSI COAT AND DEVELOP TRACK FOR 6" WAFERS*



Use Recipe: Coat.rcp and Develop.rcp

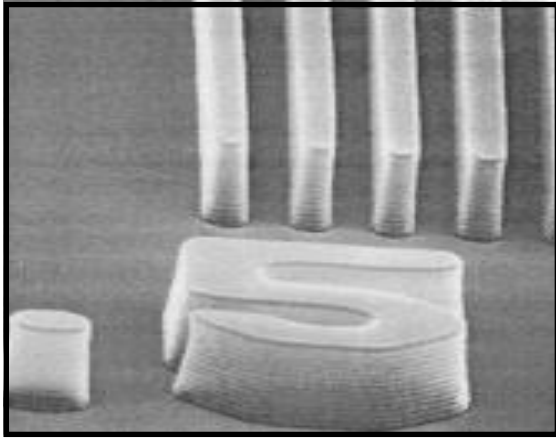
*Rochester Institute of Technology*  
*Microelectronic Engineering*

**RECIPES FOR RESIST COAT AND DEVELOP**

Level	Level Name	Resist	Coat Recipe	Develop Recipe	Resist Thickness
0	Zero	OIR-620	Coat	Develop	1.0um
1	Poly 1	OIR-620	Coat	Develop	1.0um
2	Sac Ox	OIR-620	Coat	Develop	1.0um
3	Anchor	S1827	MEMS-COAT	MEMS-DEV	4.5um
4	Poly 2	S1827	MEMS-COAT	MEMS-DEV	4.5um
5	CC	S1827	MEMS-COAT	MEMS-DEV	4.5um
6	Metal 1	S1827	MEMS-COAT	MEMS-DEV	4.5um

MEMSCOAT.rcp 2500rpm, 30sec, Hand Dispense, 110°C, 1min  
 Exposure for S1827, 400mj/cm<sup>2</sup>, Focus +2.0, NA=0.46,  $\sigma=0.45$   
 MEMSDEV.rcp has 200 second develop time, no hardbake

*ASML 5500/200*



NA = 0.48 to 0.60 variable  
 $\sigma = 0.35$  to 0.85 variable  
With Variable Kohler, or  
Variable Annular illumination  
Resolution =  $K_1 \lambda / \text{NA}$   
 $= \sim 0.35 \mu\text{m}$   
for NA=0.6,  $\sigma = 0.85$   
Depth of Focus =  $k_2 \lambda / (\text{NA})^2$   
 $= 1.0 \mu\text{m}$  for NA = 0.6



i-Line Stepper  $\lambda = 365 \text{ nm}$   
22 x 27 mm Field Size

***STEPPER JOB***

Mask Barcode:

Stepper Jobname: MCEE770-MEMS

Level 0 (combi reticle)

Level Clearout (combi reticle)

Level SacOx

Level Poly 1

Level Anchor

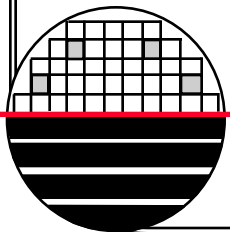
Level Poly 2

Level CC

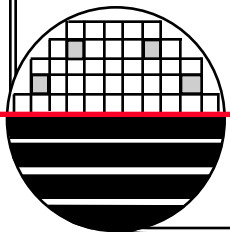
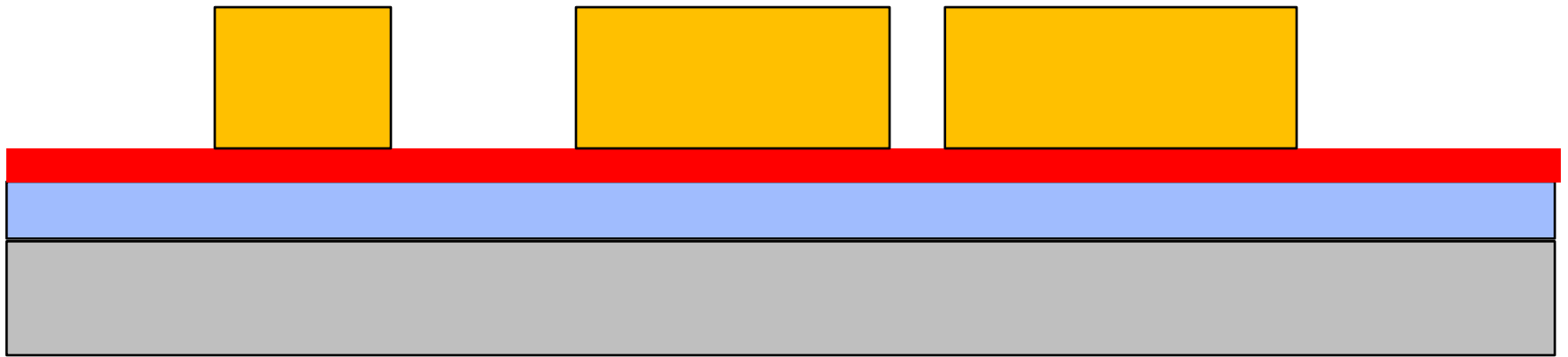
Level Metal

Level No Implant

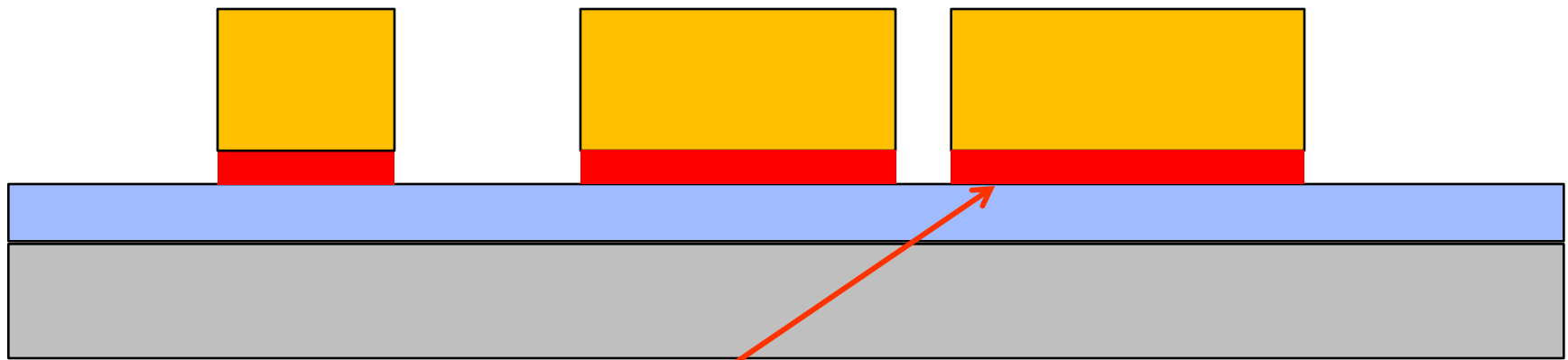
Level MEMS-Test (no alignment)



*AFTER PHOTORESIST COAT, EXPOSE & DEVELOP*



*AFTER POLY1 ETCH*

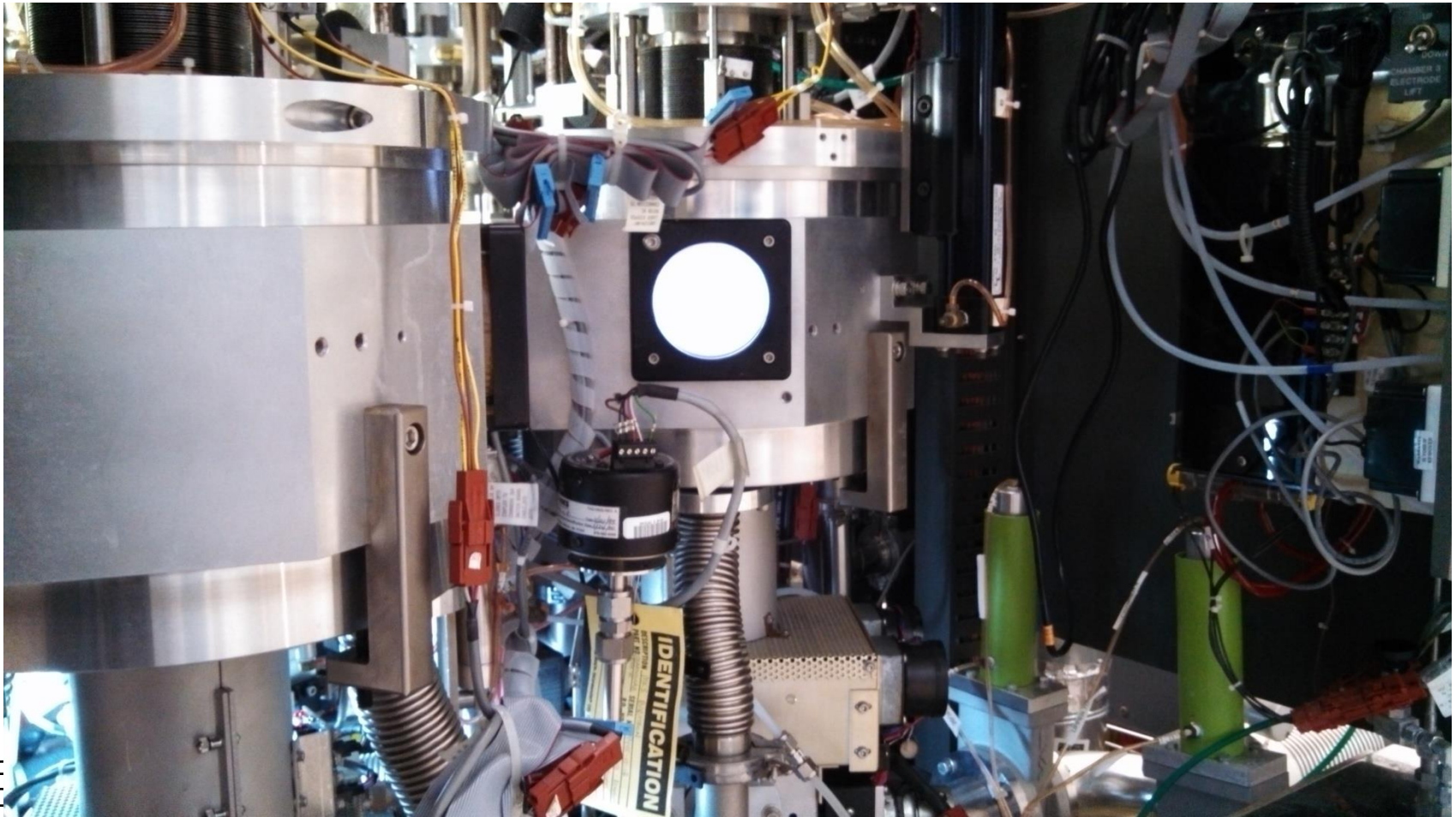


5000Å Poly

Drytek Quad  
Recipe FACPOLY  
Etch Rate  $\sim 1150\text{\AA}/\text{min}$



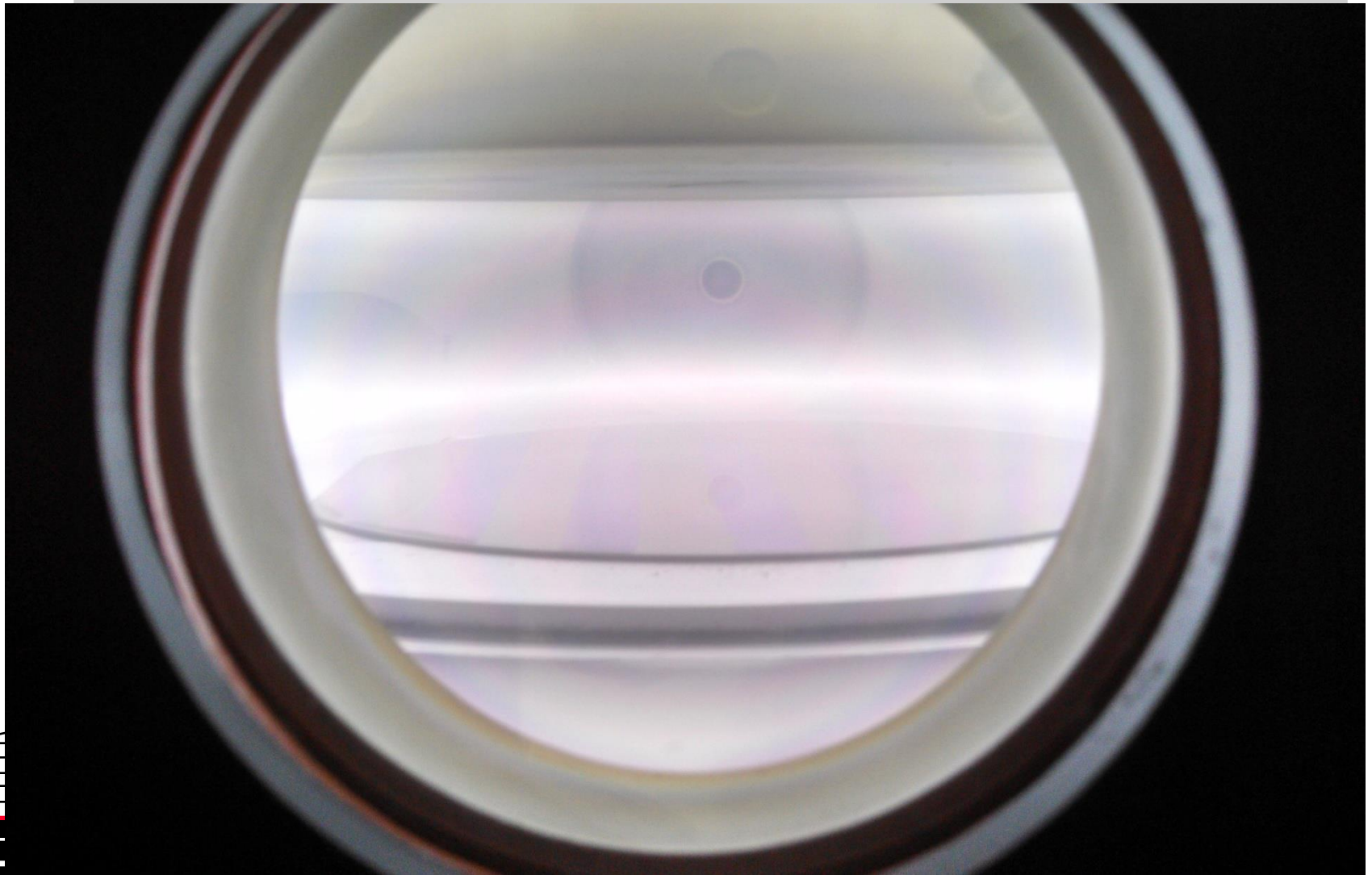
***2 OF 4 CHAMBERS IN THE DRYTEK QUAD RIE TOOL***



*Rochester Institute of Technology  
Microelectronic Engineering*



*PLASMA ETCHING IN THE DRYTEK QUAD*



***ANISOTROPIC POLY GATE ETCH RECIPE*****Anisotropic Poly Gate Etch Recipe**

SF6 30 sccm, CHF3 30 sccm, O2 5 sccm, RF Power 160 w, Pressure 40 mTorr, 1900 Å/min (Anisotropic), Resist Etch Rate 300 Å/min, Oxide Etch Rate 200 Å/min

Recipe Name: FACPOLY Step 2

Chamber 2

Power 160 watts

Pressure 40 mTorr

Gas SF6

Flow 30 sccm

Gas CHF3

Flow 30 sccm

Gas O2

Flow 5 sccm

Poly Etch Rate 1150 Å/min

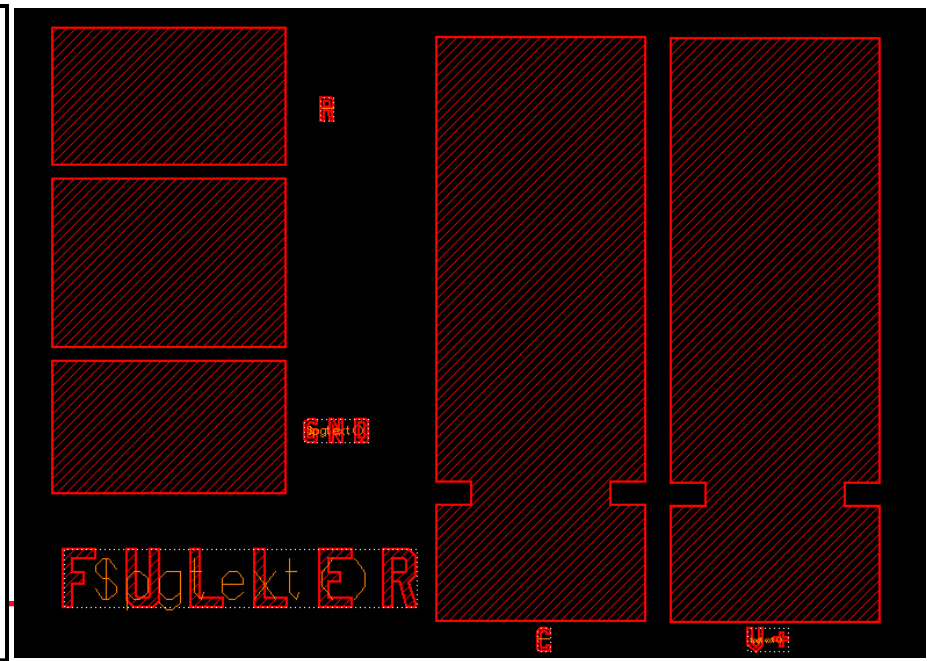
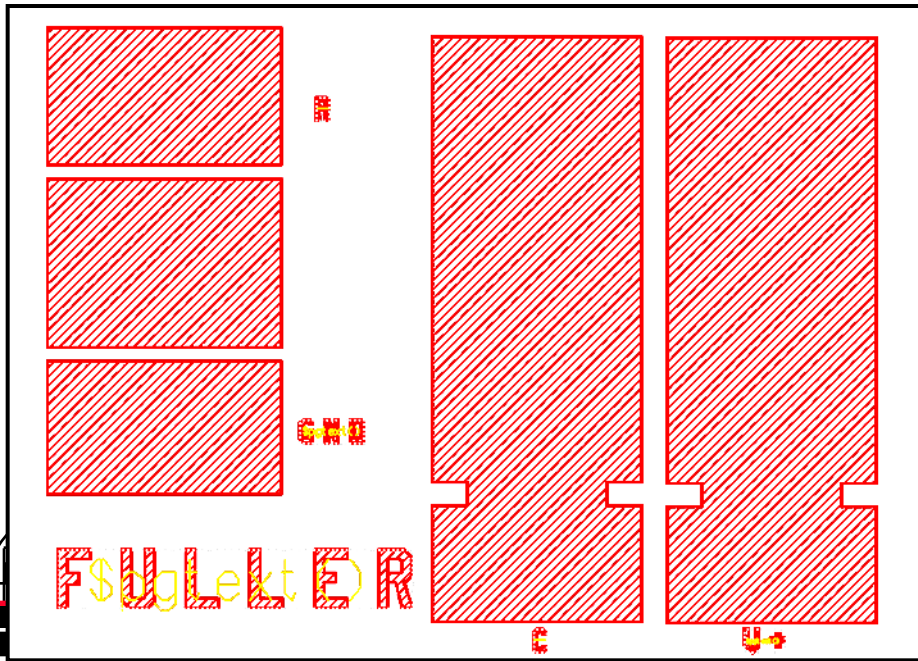
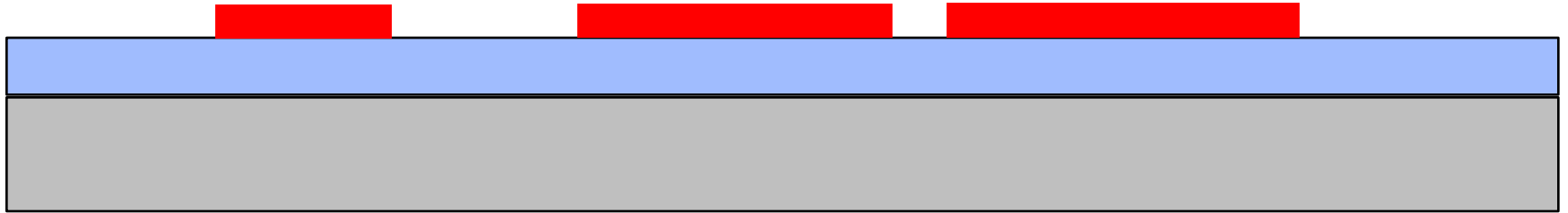
Photoresist Etch Rate: 300 Å/min

Oxide Etch Rate: 200 Å/min

**Endpoint See Video**

**<http://people.rit.edu/lffeee/videos.htm>**

*STRIP RESIST, RCA CLEAN*



**SPECIAL RCA CLEAN (TWO 50:1 HF STEPS)**

**PLAY**

**APM**

NH<sub>4</sub>OH - 1part  
H<sub>2</sub>O<sub>2</sub> - 3parts  
H<sub>2</sub>O - 15parts  
70 °C, 15 min.

DI water  
rinse, 5 min.

H<sub>2</sub>O - 50  
HF - 1  
60 sec.

**HPM**

HCL - 1part  
H<sub>2</sub>O<sub>2</sub> - 3parts  
H<sub>2</sub>O - 15parts  
70 °C, 15 min.

DI water  
rinse, 5 min.

DI water  
rinse, 5 min.

H<sub>2</sub>O - 50  
HF - 1  
60 sec.

DI water  
rinse, 5 min.

SPIN/RINSE  
DRY

*DEPOSIT POLYSILICON*

Poly Target 1000A  
LPCVD, 610C, Rate  $\sim 67\text{\AA}/\text{min}$   
Time  $\sim 15$  min

Recipe POLY 610  
Temp =  $610^{\circ}\text{C}$   
Pressure = 300 mTorr  
Silane Flow = 90 sccm

Substrate



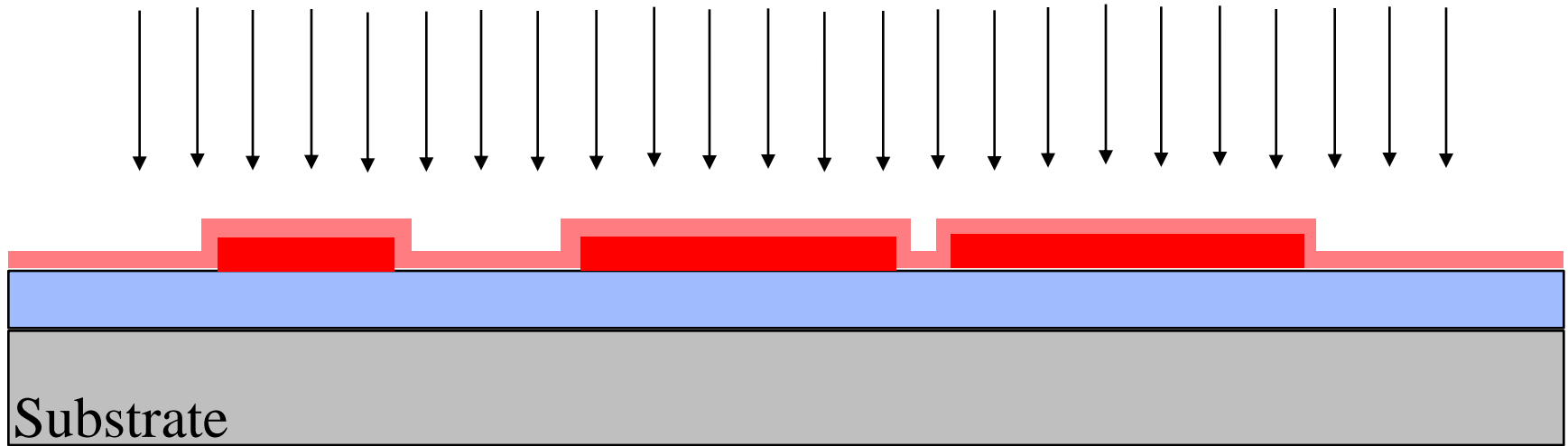
***VARIAN 350 D ION IMPLANTER (4" AND 6" WAFERS)***



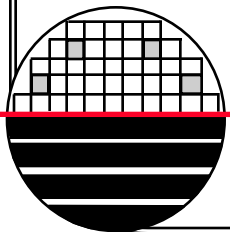
*Rochester Institute of Technology  
Microelectronic Engineering*



*POLYSILICON DOPING*



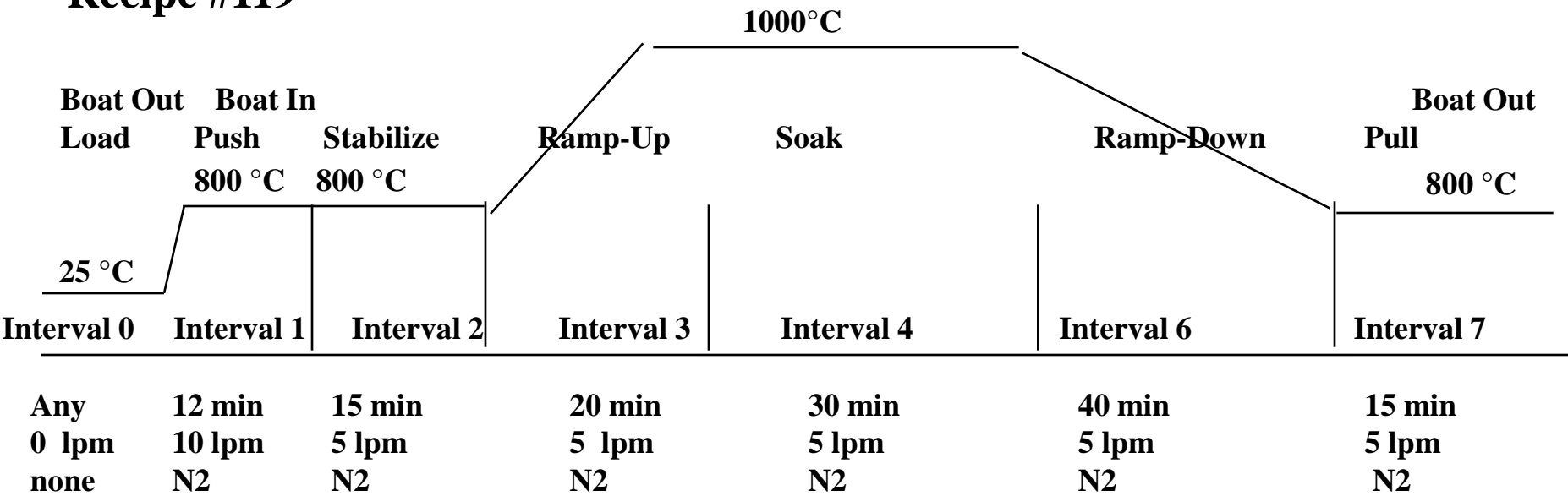
Ion Implant P31  
Dose =  $2E16 \text{ cm}^{-2}$   
Energy = 100KeV  
Time ~?? min at 400  $\mu\text{A}$   
Anneal Tube 2 Recipe 119





**BRUCE RECIPE 119 – N++ POLY DOPE/ANNEAL**

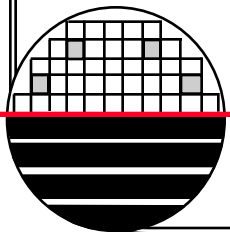
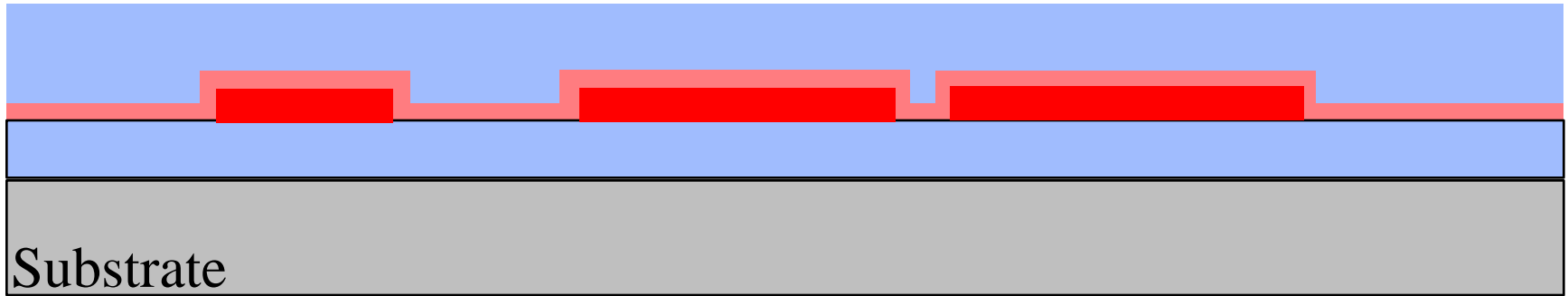
**Recipe #119**



At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

**N+ Poly Doping/Anneal, Thick Poly, > 1 μm, No Oxide Growth**

*SAC OX DEPOSITION*



## PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)

Step 1

Setup Time = 15 sec

Pressure = 9 Torr

Susceptor Temperature = 390 C

Susceptor Spacing = 220 mils

RF Power = 0 watts

TEOS Flow = 400 scc

O<sub>2</sub> Flow = 285 scc

Step 2 – Deposition

Dep Time = 55 sec (5000 Å)

Pressure = 9 Torr

Susceptor Temperature = 390 C

Susceptor Spacing = 220 mils

RF Power = 205 watts

TEOS Flow = 400 scc

O<sub>2</sub> Flow = 285 scc

Step 3 – Clean

Time = 10 sec

Pressure = Fully Open

Susceptor Temperature = 390 C

Susceptor Spacing = 999 mils

RF Power = 50 watts

TEOS Flow = 0 scc

O<sub>2</sub> Flow = 285 scc



*SSI COAT AND DEVELOP TRACK FOR 6" WAFERS*



Use Recipe: Coat.rcp and Develop.rcp

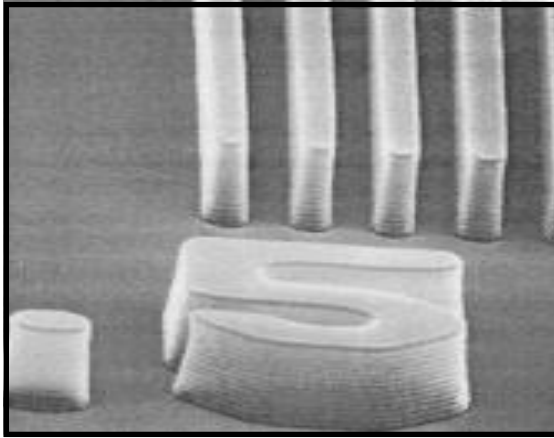
*Rochester Institute of Technology*  
*Microelectronic Engineering*

**RECIPES FOR RESIST COAT AND DEVELOP**

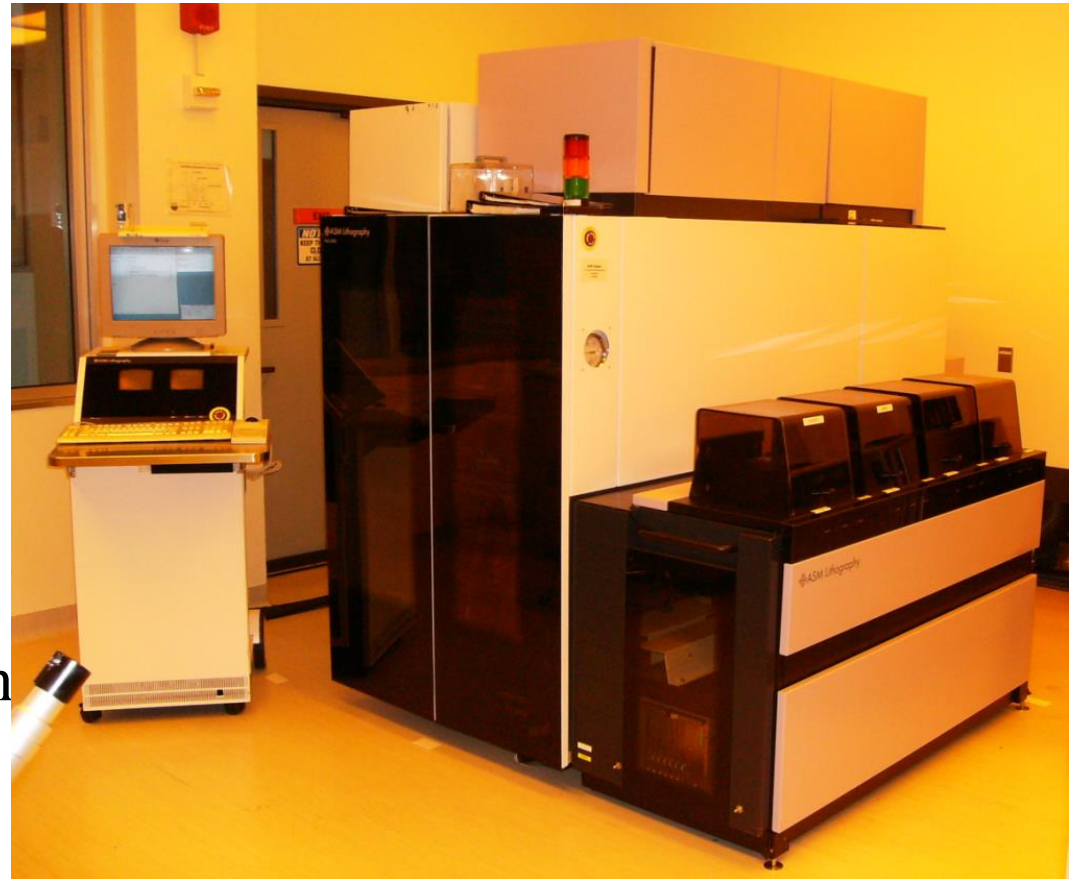
Level	Level Name	Resist	Coat Recipe	Develop Recipe	Resist Thickness
0	Zero	OIR-620	Coat	Develop	1.0um
1	Poly 1	OIR-620	Coat	Develop	1.0um
2	Sac Ox	OIR-620	Coat	Develop	1.0um
3	Anchor	S1827	MEMS-COAT	MEMS-DEV	4.5um
4	Poly 2	S1827	MEMS-COAT	MEMS-DEV	4.5um
5	CC	S1827	MEMS-COAT	MEMS-DEV	4.5um
6	Metal 1	S1827	MEMS-COAT	MEMS-DEV	4.5um

MEMSCOAT.rcp 2500rpm, 30sec, Hand Dispense, 110°C, 1min  
 Exposure for S1827, 400mj/cm<sup>2</sup>, Focus +2.0, NA=0.46,  $\sigma=0.45$   
 MEMSDEV.rcp has 200 second develop time, no hardbake

*ASML 5500/200*



NA = 0.48 to 0.60 variable  
 $\sigma = 0.35$  to 0.85 variable  
With Variable Kohler, or  
Variable Annular illumination  
Resolution =  $K_1 \lambda / NA$   
 $= \sim 0.35 \mu\text{m}$   
for NA=0.6,  $\sigma = 0.85$   
Depth of Focus =  $k_2 \lambda / (NA)^2$   
 $= 1.0 \mu\text{m}$  for NA = 0.6



i-Line Stepper  $\lambda = 365 \text{ nm}$   
22 x 27 mm Field Size

***STEPPER JOB***

Mask Barcode:

Stepper Jobname: MCEE770-MEMS

Level 0 (combi reticle)

Level Clearout (combi reticle)

Level SacOx

Level Poly 1

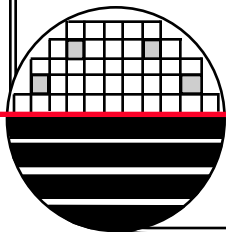
Level Anchor

Level Poly 2

Level CC

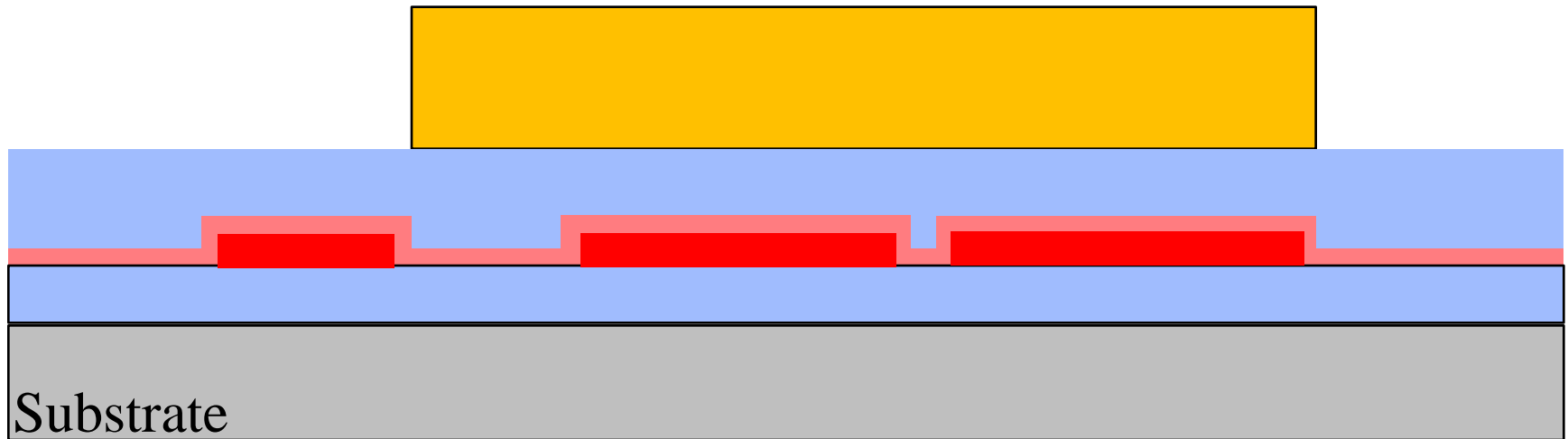
Level Metal

Level No Implant





*AFTER SAC OX PHOTO AND ETCH*



Etch SacOx

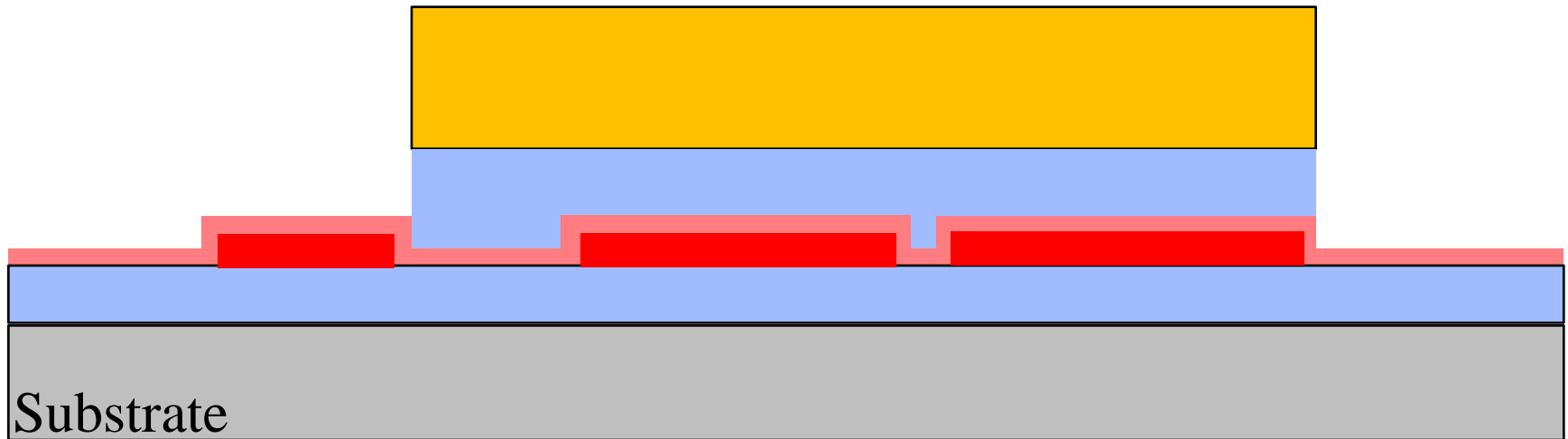
Etch Rate =  $2633\text{\AA}/\text{min}$

Using 5:1BOE

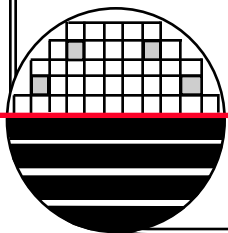
~6min. For  $1.4\mu\text{m}$  TEOS

Rinse 5 min. SRD

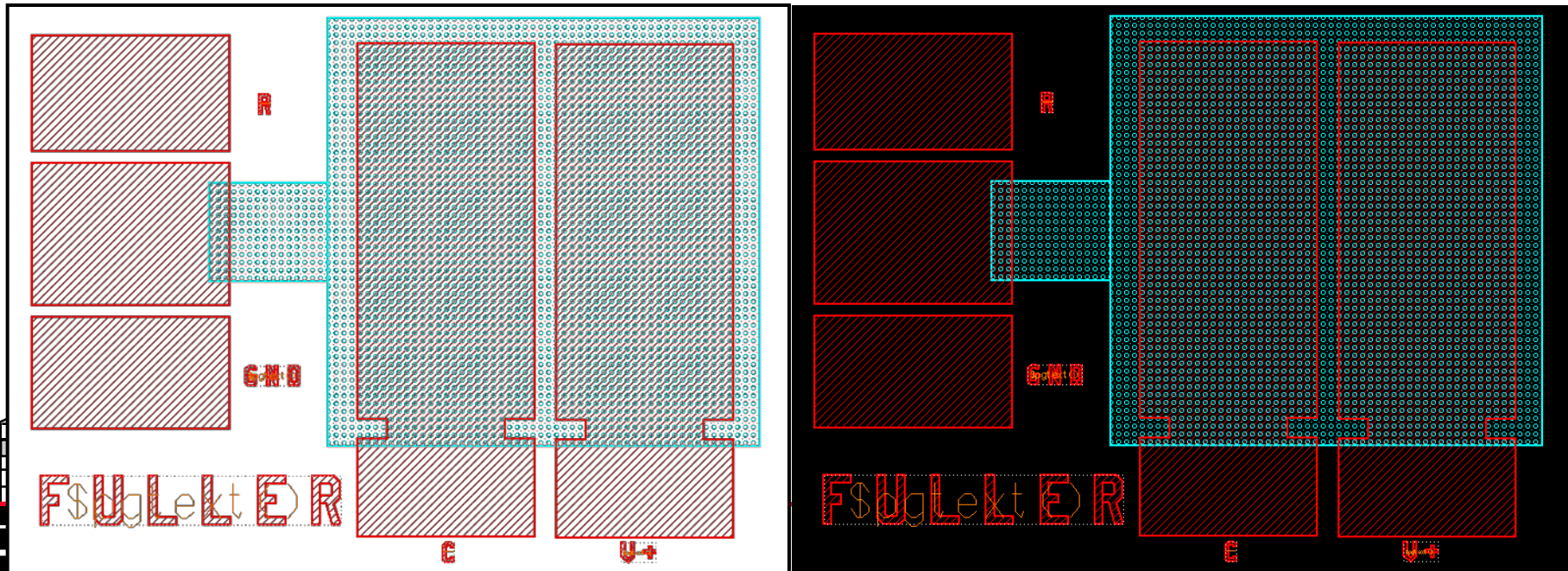
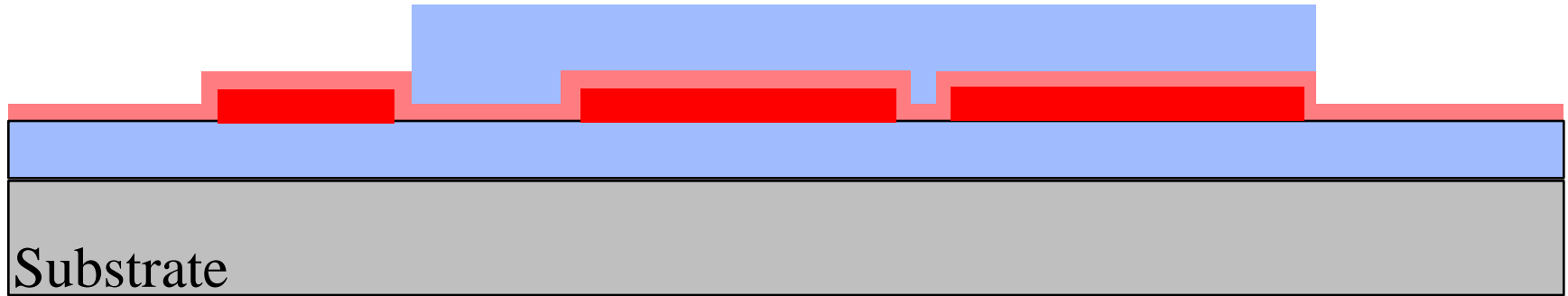
*AFTER SAC OX PHOTO AND ETCH*



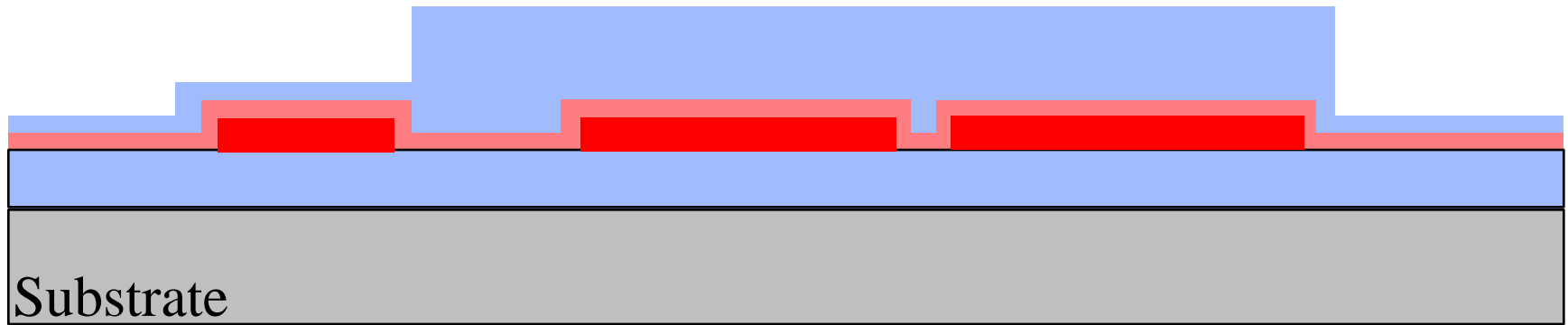
Substrate



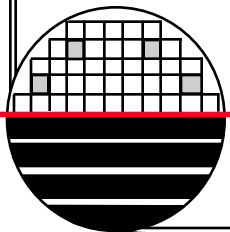
*RESIST STRIP*



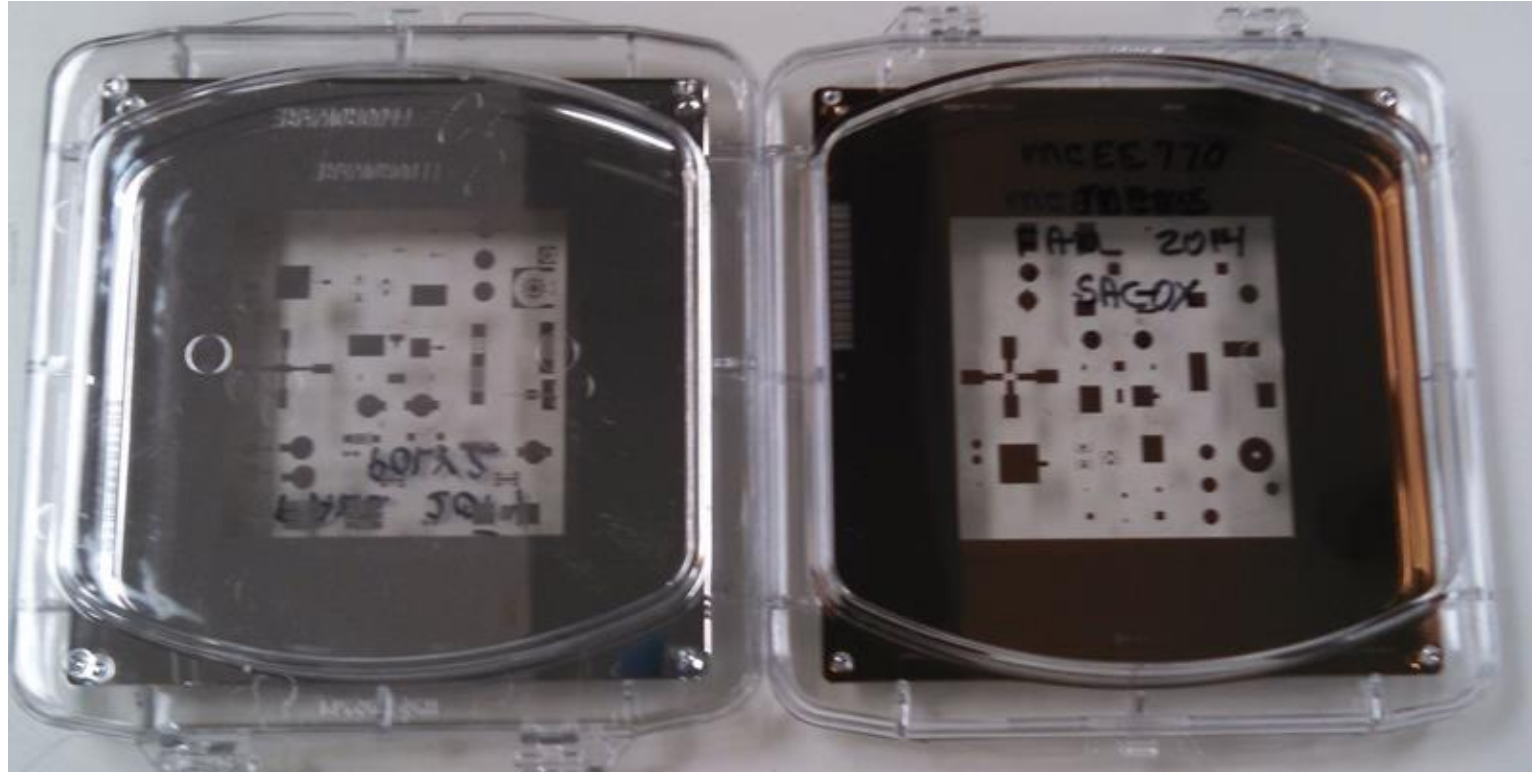
*DEPOSIT ETCH STOP*



TEOS Oxide  
2000Å



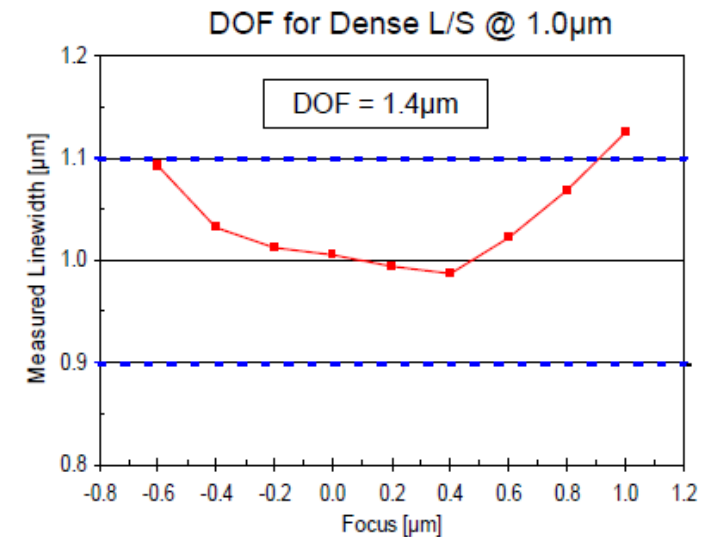
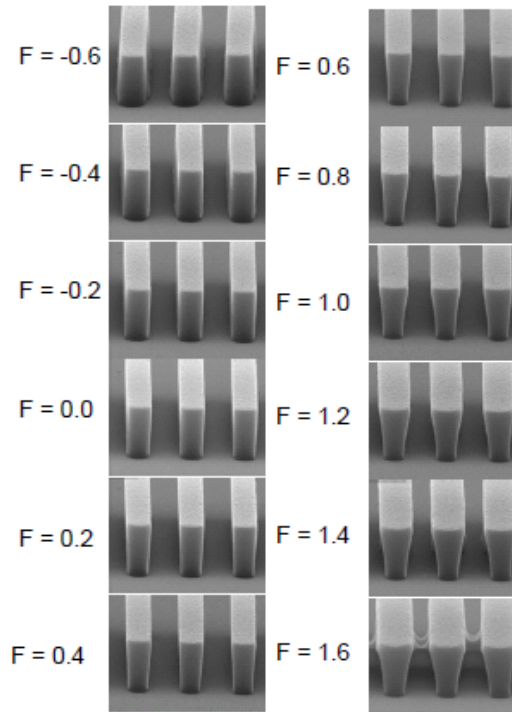
*CLEAR FIELD MASKS*



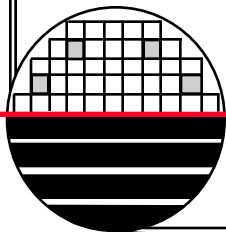
**USING IMAGE REVERSAL RESIST**

**AZ nLOF 2020  
Depth of Focus @ 1.0 μm CD**

FT = 2.0μm, DTP = 66 mJ/cm<sup>2</sup>



FT = 2.0μm, SB 110°C/ 60 sec, PEB 110°C/ 60 sec,  
60 sec single puddle in AZ 300 MIF Developer @ 23°C  
Nikon 0.54 NA I-line



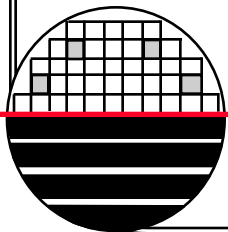
Rochester Insti  
Microelectronic



AZ, the AZ logo, BARLi, Aquatar, nLOF, Kwik Strip, Klebosol, and Spinfil are registered trademarks and AX, DX, HERB, HiR, MiR, NCD, PLP, Signiflow, SWG, and TARP are trademarks of AZ Electronic Materials.

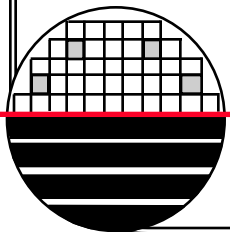
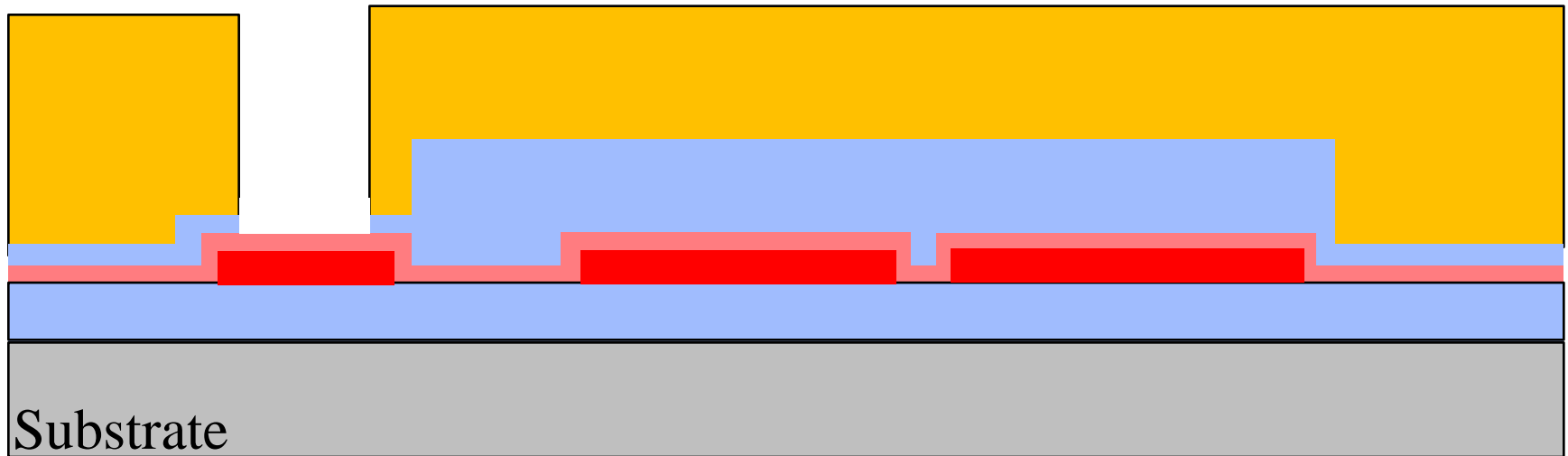
## *LIFT-OFF USING IMAGE REVERSAL RESIST*

1. Coat wafers with n-LOF-2020 Image Reversal Resist, Use COATNLOF recipe on the SSI track  
HMDS prime: 140C, Dispense for 30s, Prime for 60s  
Manually dispense photoresist  
Spin at 2500 RPM, Spin for 60s, Thickness ~2500nm  
Soft Bake at 110C, Bake for 60s
2. Expose on the ASML Stepper – use same mask as for etch process (clear field mask)  
Dose = 66 mJ/cm<sup>2</sup> i-line (365nm), Focus = 1.5, NA = 0.60, Sigma=0.625
3. Develop on SSI Track using recipe DEVNLOF  
PEB (Image Reversal Bake) at 110C for 60s  
Spin and dispense developer for 5s, Dispense developer for 5s, Puddle develop for 70s  
Spin and rinse for 30s at 1000 RPM. Spin dry for 30s at 3750 RPM  
Do not hard bake. It can damage the sidewall profile. Hard Bake time = 0s
4. Etch
5. Remove Photoresist

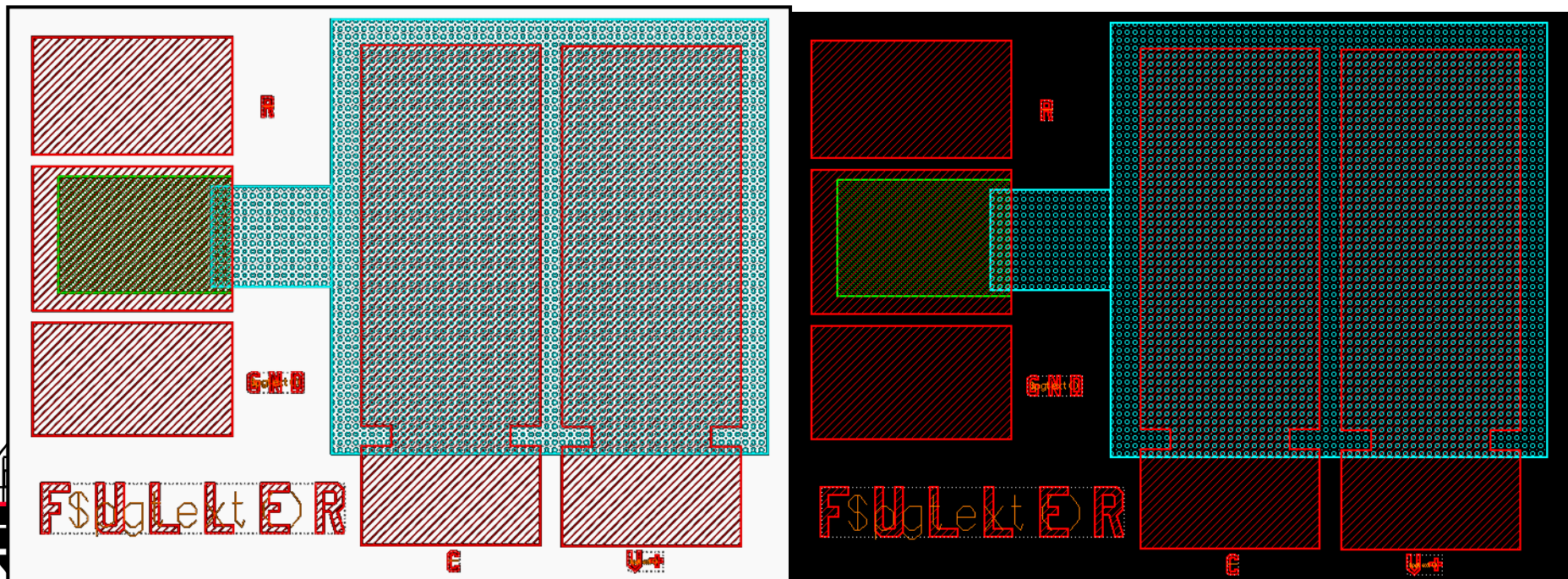
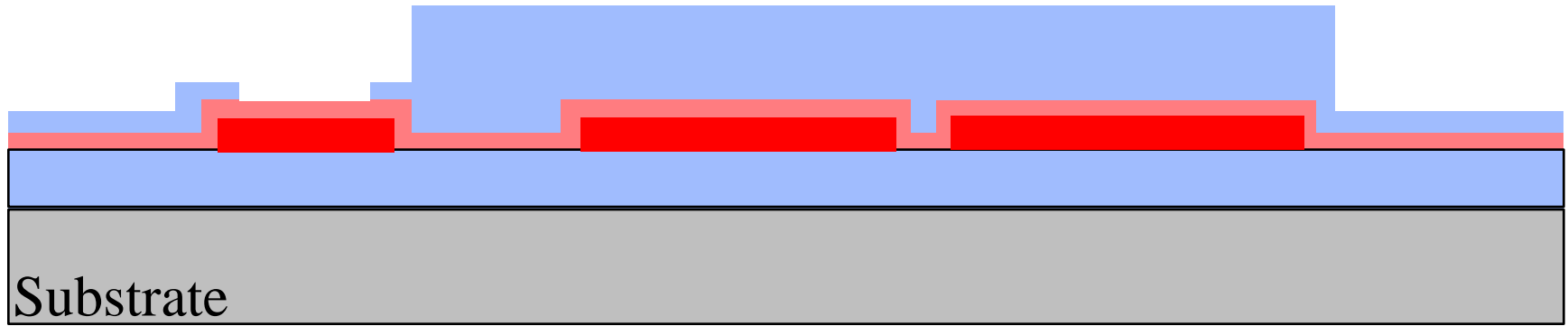




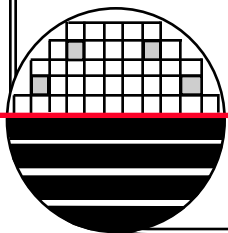
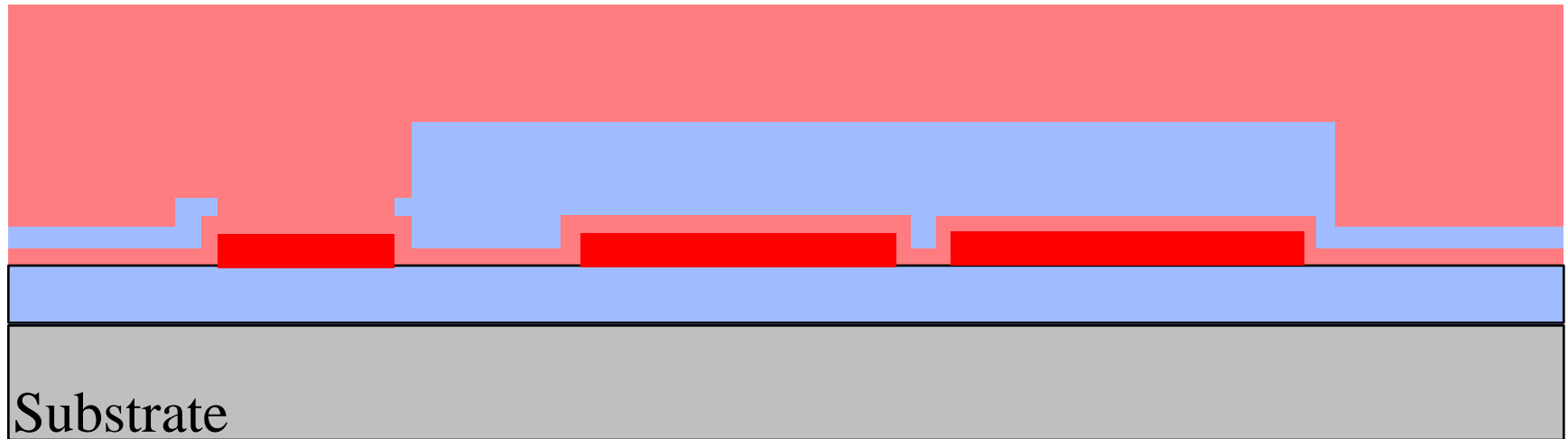
*AFTER ANCHOR PHOTO AND ETCH*



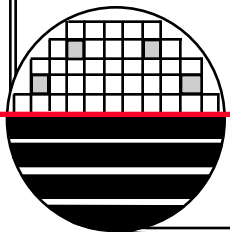
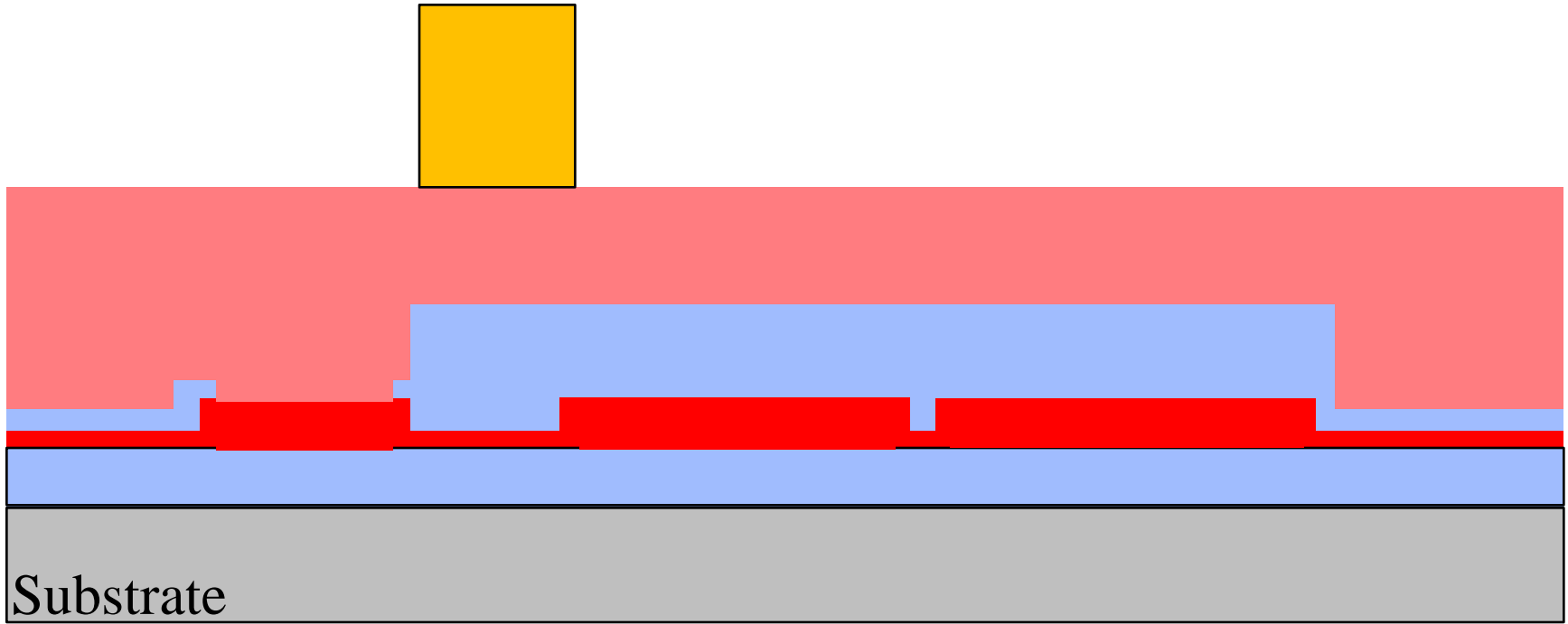
*RESIST STRIP*



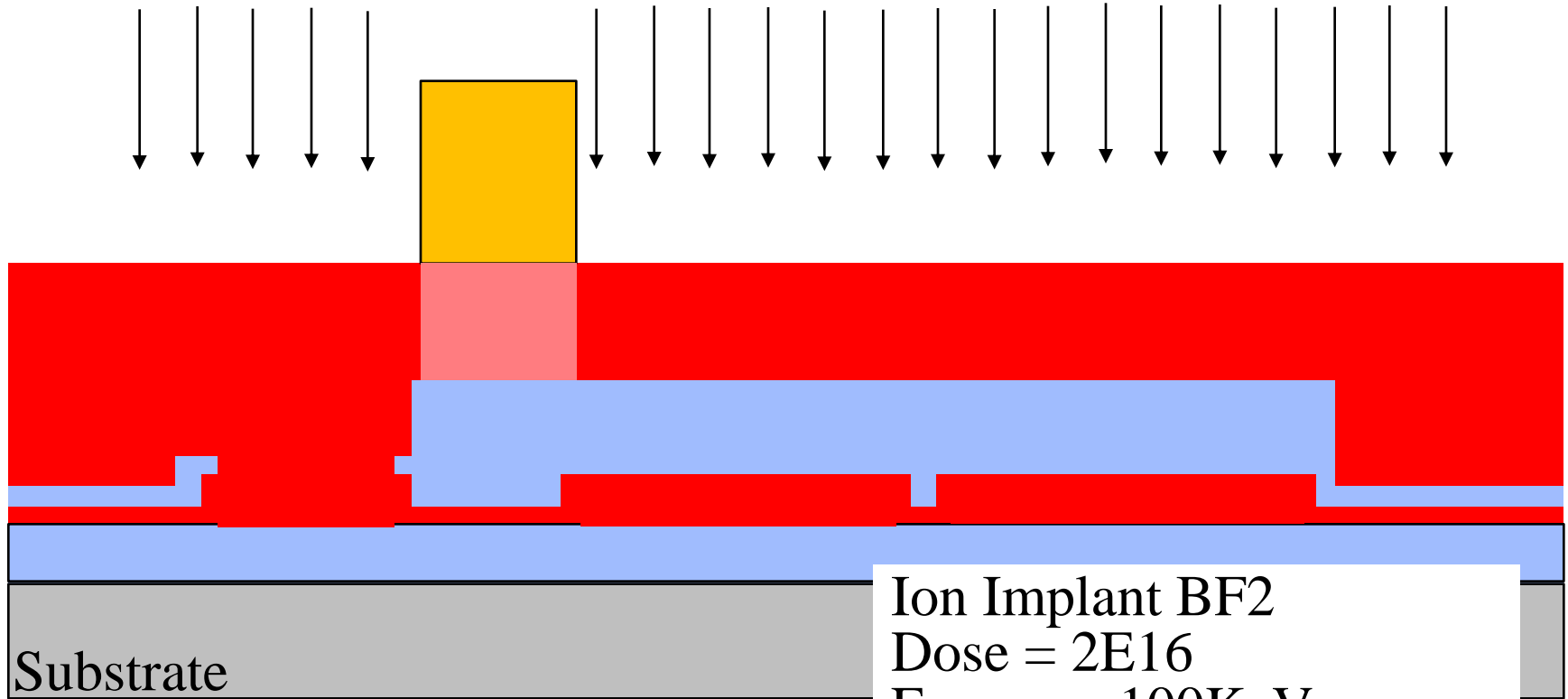
*DEPOSIT POLY 2 – MECHANICAL POLY*



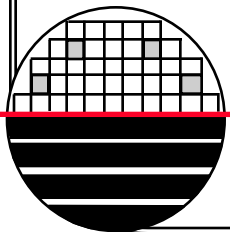
*PHOTO – NO IMPLANT*



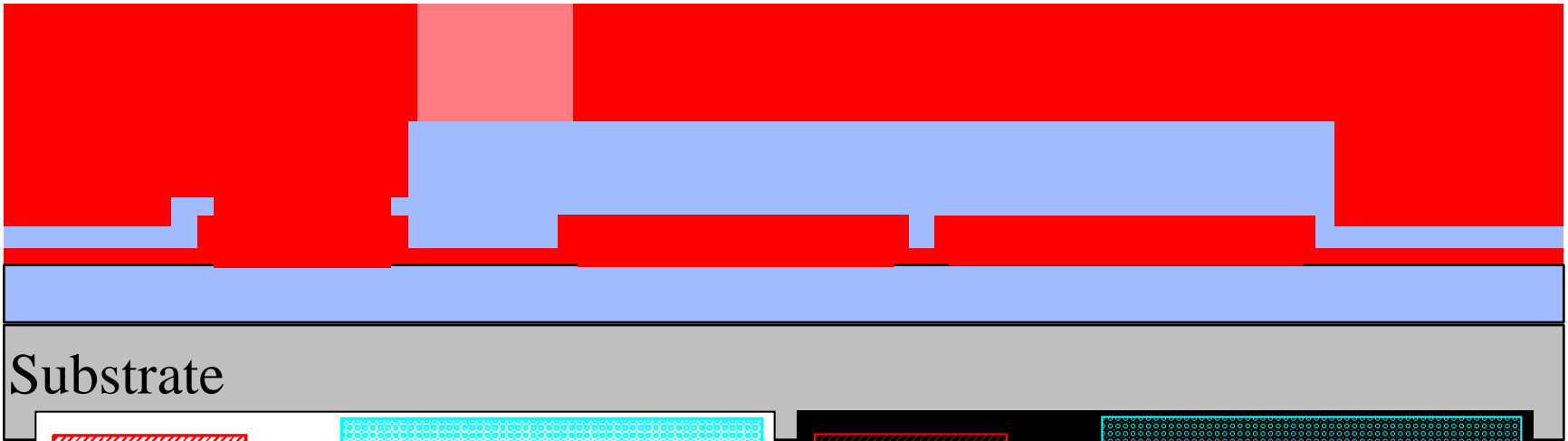
*ION IMPLANT*



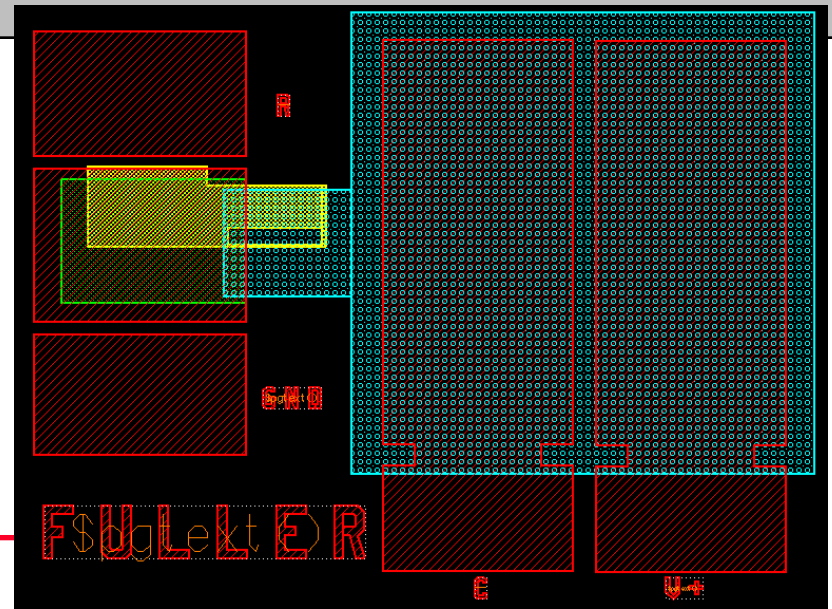
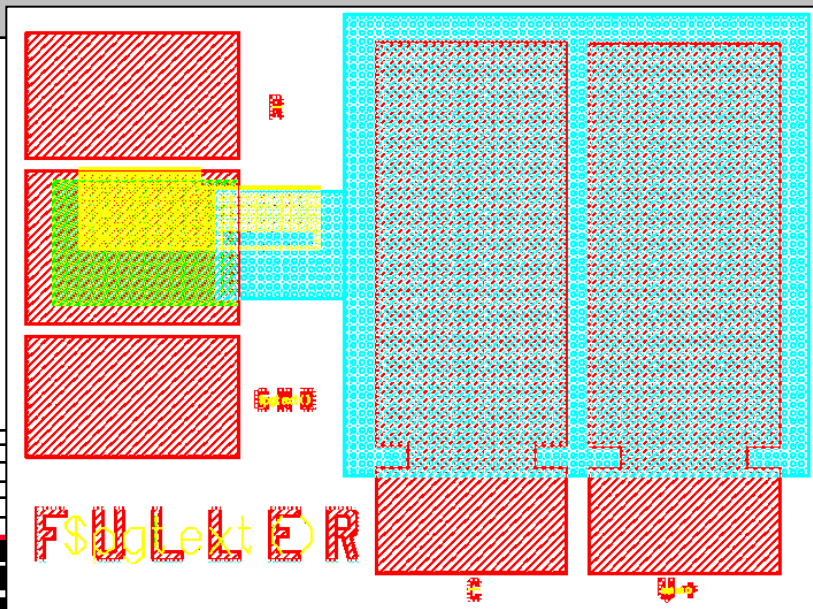
Ion Implant BF2  
Dose =  $2E16$   
Energy = 100KeV  
Time ~?? min at 400  $\mu$ A  
Anneal Tube 2 Recipe ???



*STRIP RESIST*

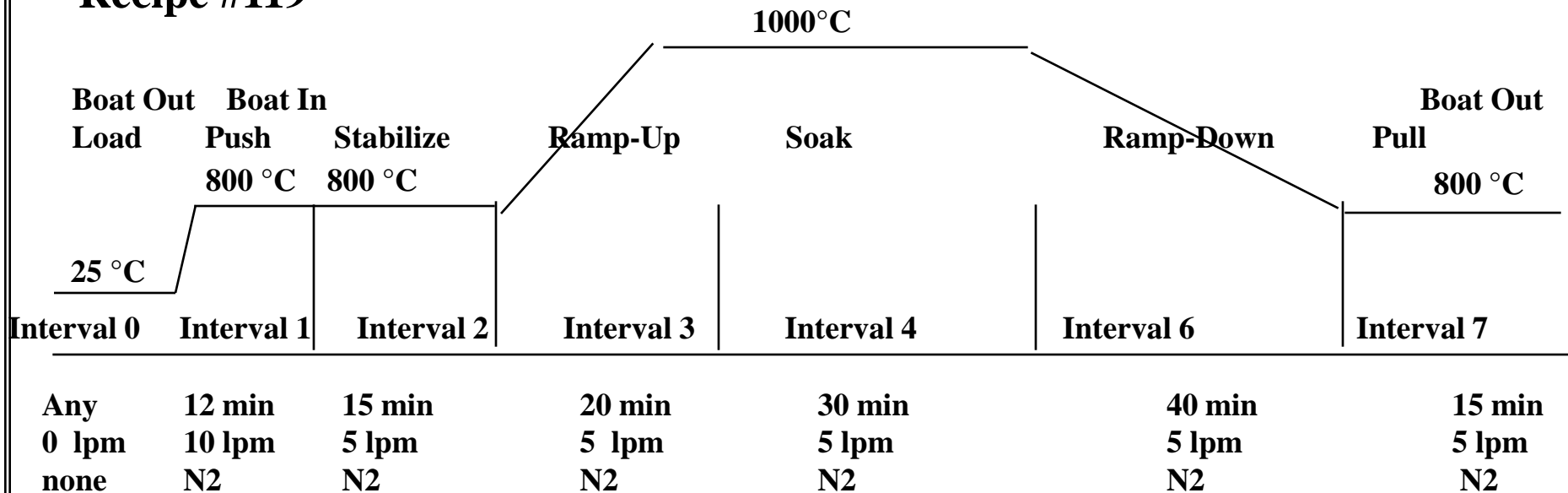


Substrate



**BRUCE RECIPE 119 – N++ POLY DOPE/ANNEAL**

**Recipe #119**



At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

**N+ Poly Doping/Anneal, Thick Poly, > 1 μm, No Oxide Growth**



## MEASURE POLY SHEET RESISTANCE



CDE Resistivity Mapper

**CDE** CDE ResMap      FileName: C:\4P\CDE\_Demo.prj\6in49pt.rcp\3220K051.RaM  
RunTitle                      CDE ResMap Demo Recipes

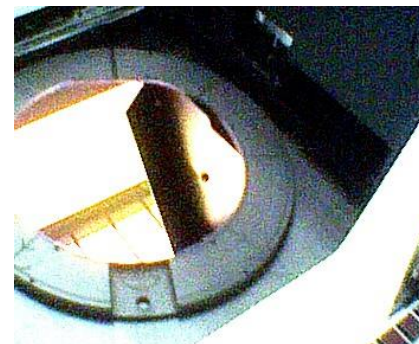
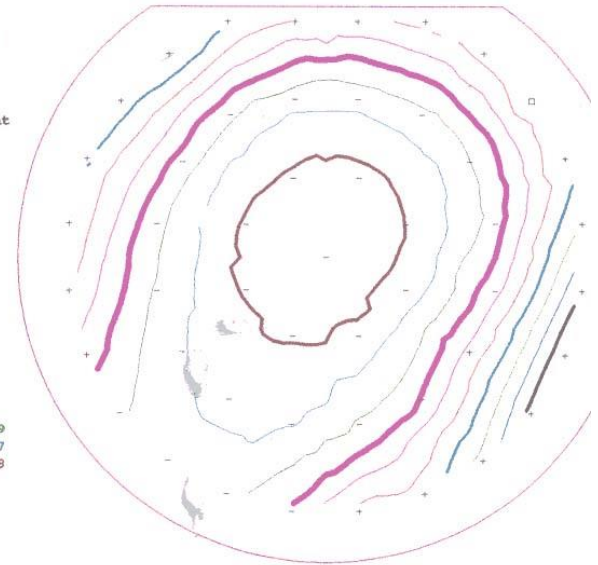
LotID,WaferID                F021111D1 MyWafer  
RunDate                      10:05 02/20/03  
Recip Name                    CDE\_Demo 6in49pt  
Oper|Engr[Equip]:            CDE|Customer [ResMap]

Wafer No.                      DualPrbCnfg  
WaferDia                      100            Flat  
EdgeExclusn                    8.0           FollowMajorFlat

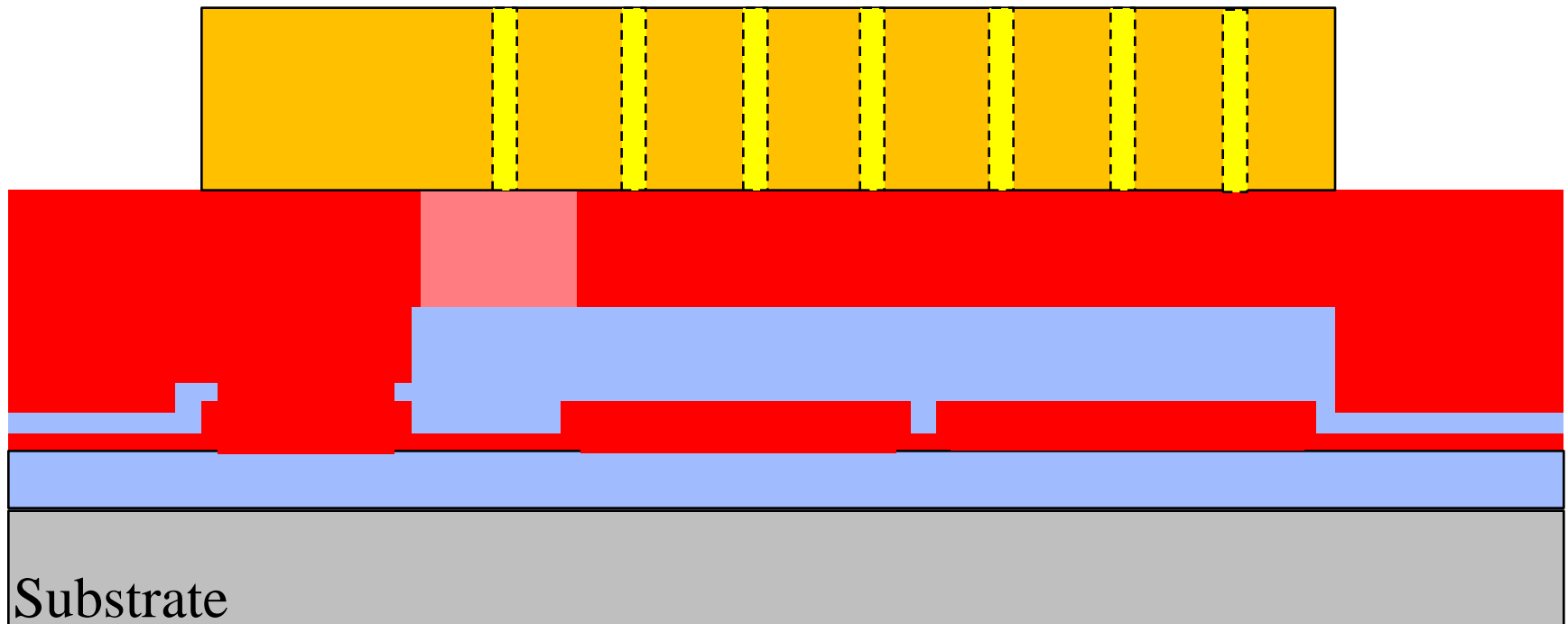
ProbePoints: 49    #Good: 48  
Rs Avg 105.301 Ohms/sq  
StdDev 10.5959 10.063%    3Sigma=30.188%  
Min 90.039    Max 130.19    Range 40.156  
(Mx-Mn)/(Mx+Mn) 18.23%    (-)/2Av 19.07%  
Lmin:14.49%    Lmax:23.64%    (-)/Av 38.13%  
Gradients: R/2=7.652%    ~R=22.245%  
Merit:    61.6    21%    42.6    89.6  
Rms 10.0K    IdvMx 0.74m    VsnMx 14.3m  
DataRejectSigma: 3.0

#data=49    Rs    Spacing = 1/3 Sigma

—	126.493	—	101.769
—	122.961	—	98.2367
—	119.429	—	94.7048
—	115.897		
—	112.365		
—	108.833		
—	105.301		

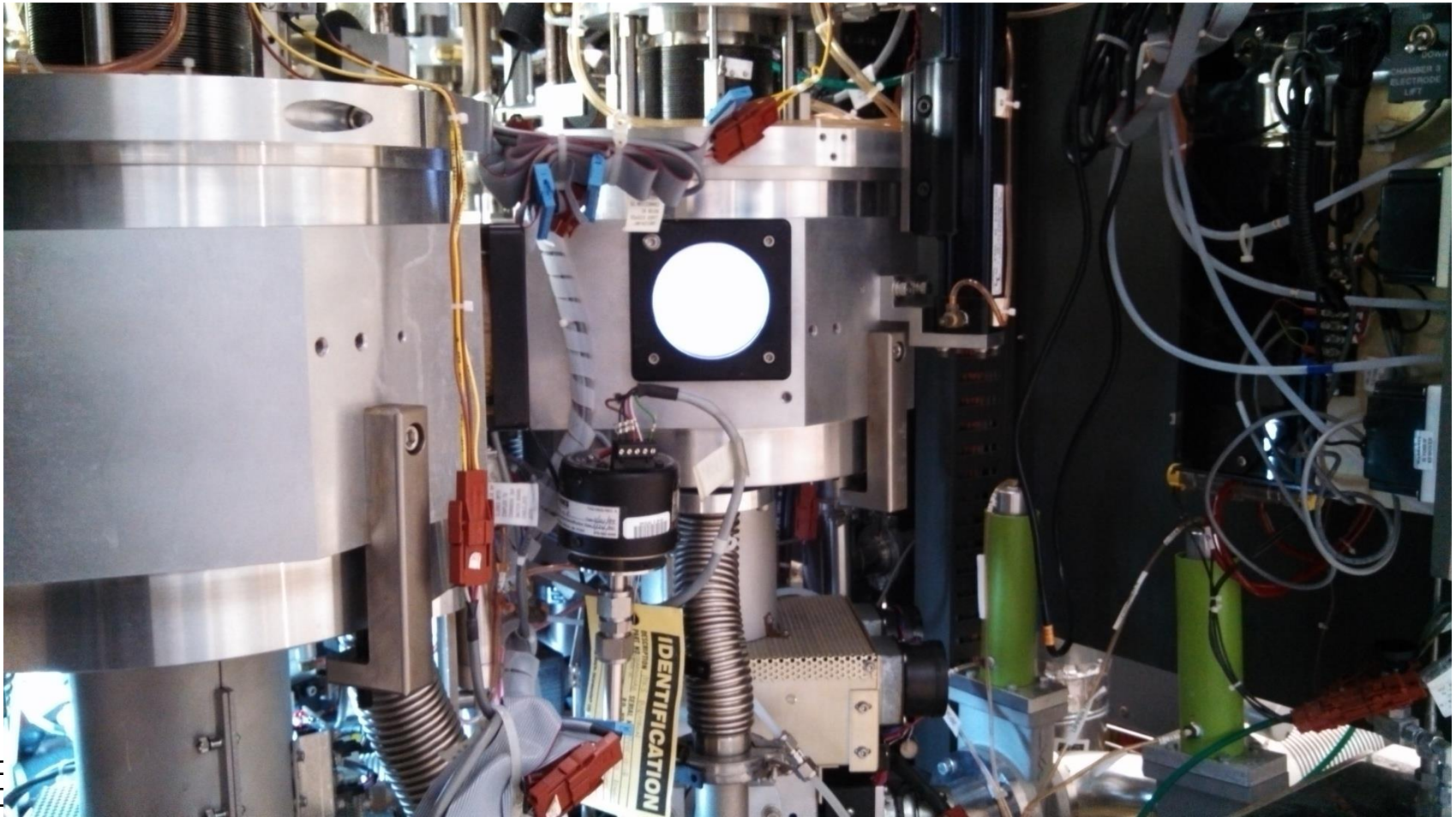


*PHOTO FOR POLY 2*



Substrate

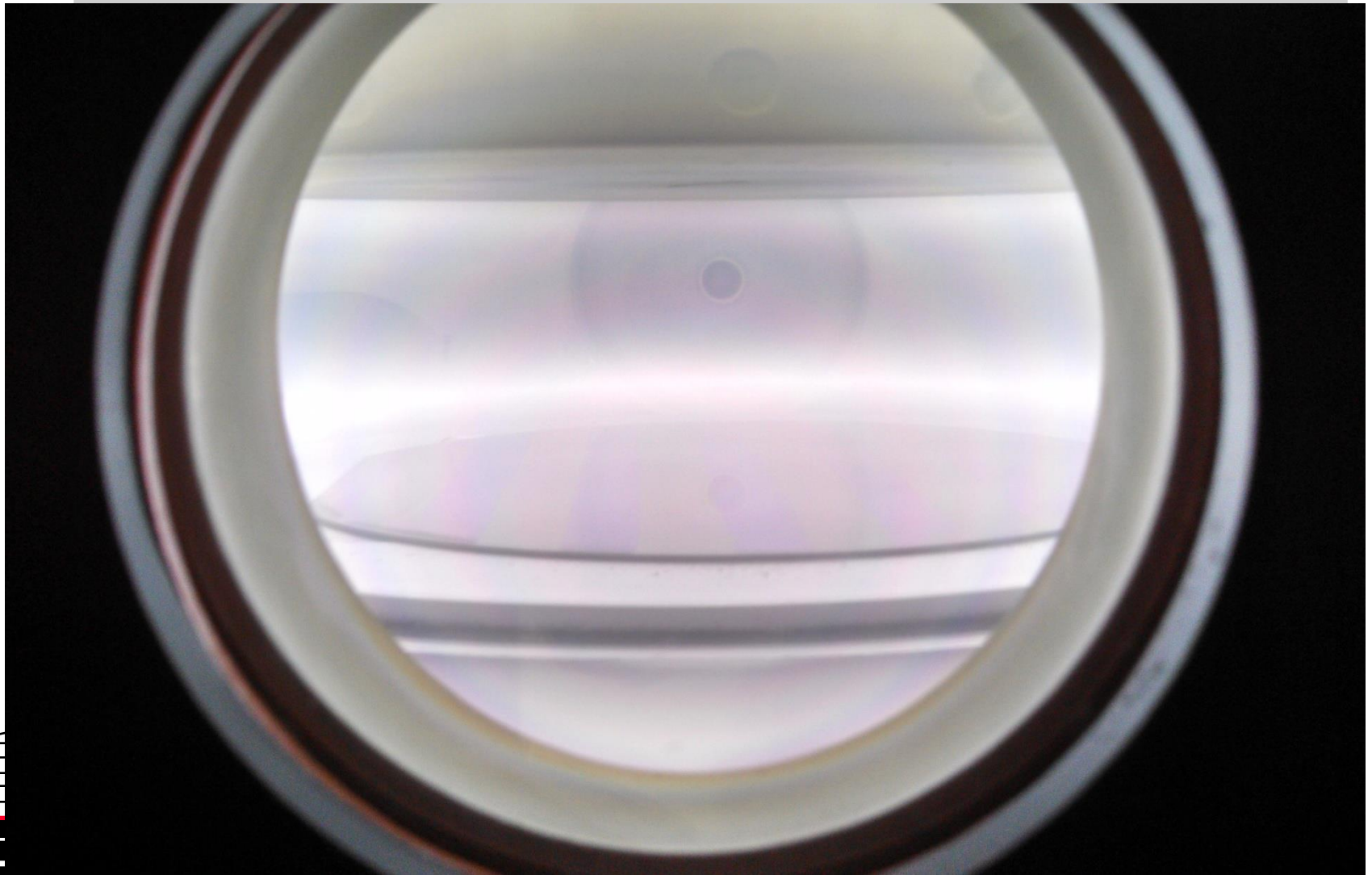
***2 OF 4 CHAMBERS IN THE DRYTEK QUAD RIE TOOL***



*Rochester Institute of Technology  
Microelectronic Engineering*



*PLASMA ETCHING IN THE DRYTEK QUAD*



***ANISOTROPIC POLY GATE ETCH RECIPE*****Anisotropic Poly Gate Etch Recipe**

SF6 30 sccm, CHF3 30 sccm, O2 5 sccm, RF Power 160 w, Pressure 40 mTorr, 1900 Å/min (Anisotropic), Resist Etch Rate 300 Å/min, Oxide Etch Rate 200 Å/min

Recipe Name: FACPOLY Step 2

Chamber

2

Power

160 watts

Pressure

40 mTorr

Gas

SF6

Flow

30 sccm

Gas

CHF3

Flow

30 sccm

Gas

O2

**Endpoint See Video**

Flow

5 sccm

**<http://people.rit.edu/lffeee/videos.htm>**

Poly Etch Rate

1150 Å/min

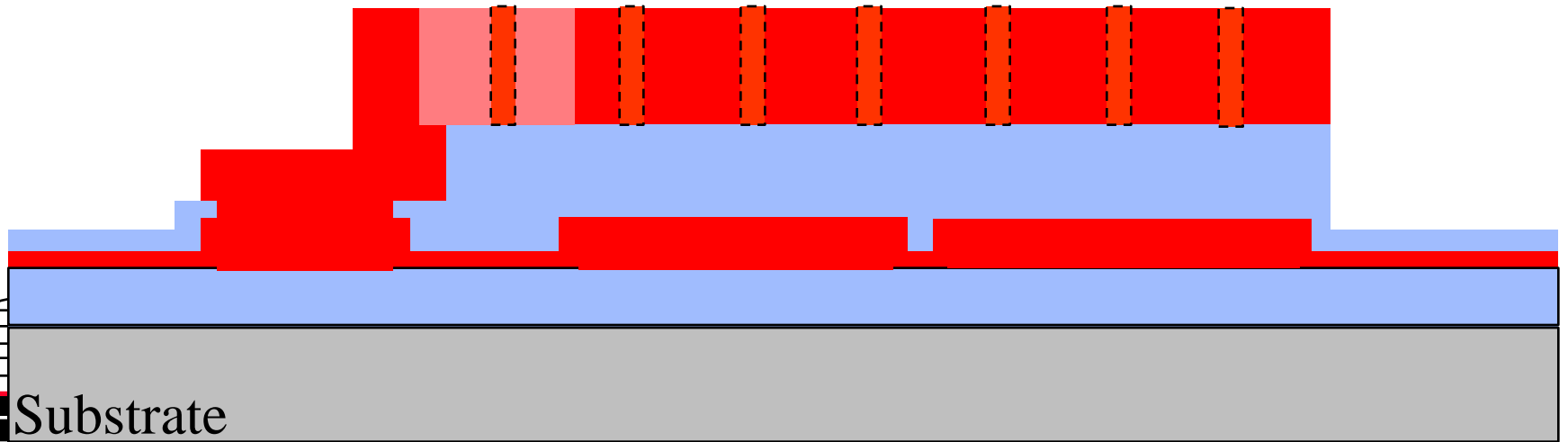
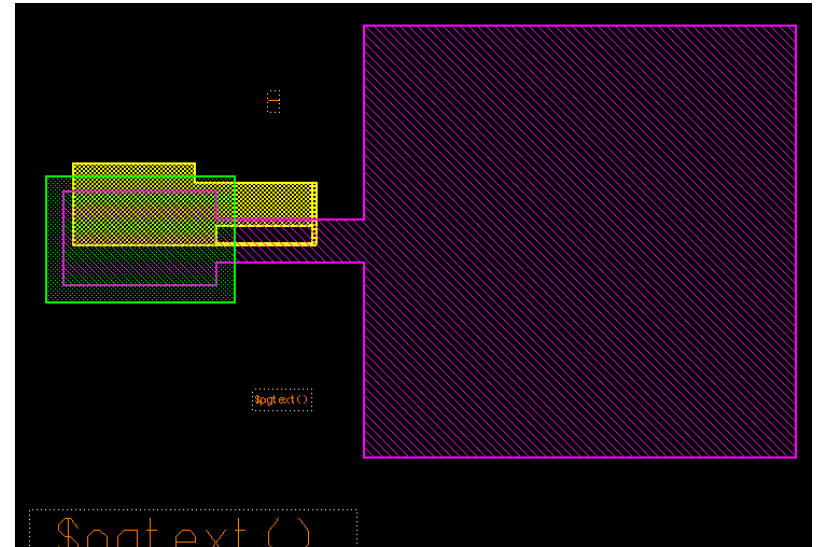
Photoresist Etch Rate:

300 Å/min

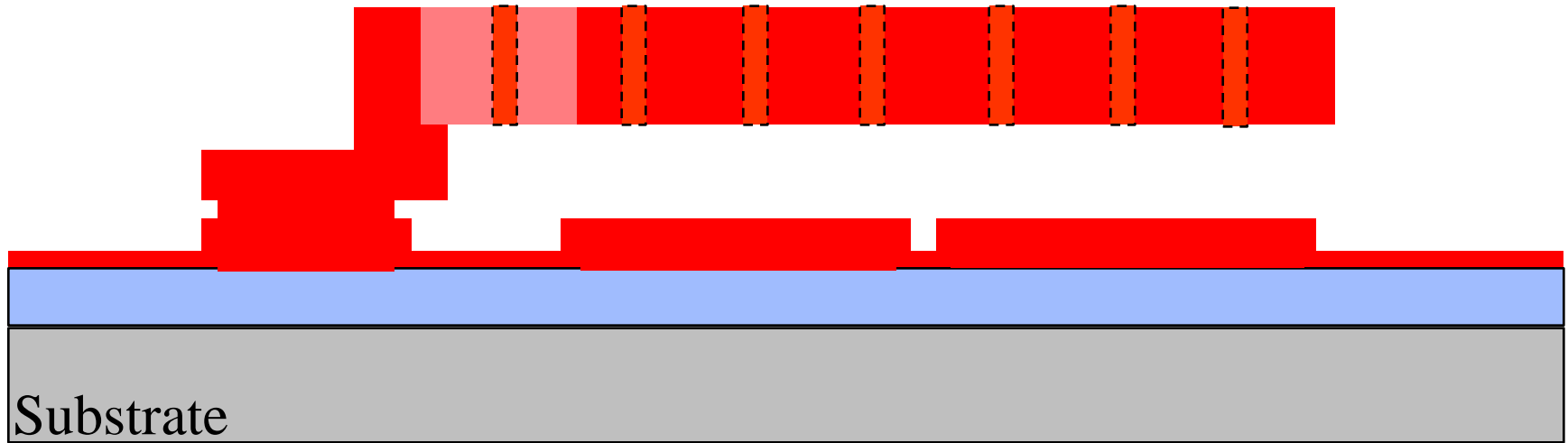
Oxide Etch Rate:

200 Å/min

*AFTER POLY 2 ETCH AND RESIST STRIP*



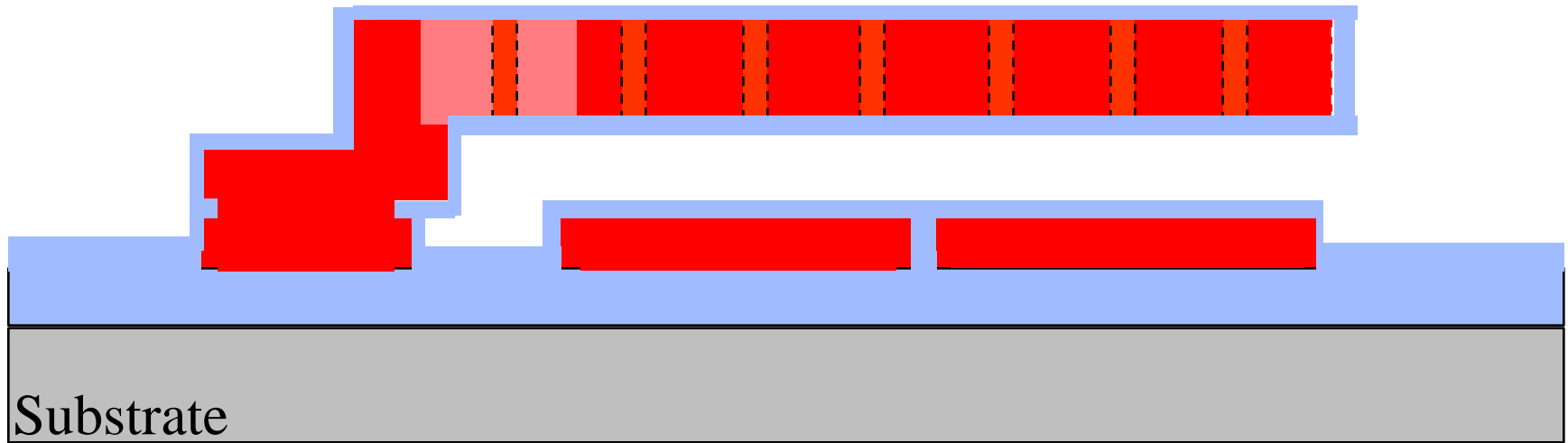
*AFTER SAC OX ETCH*



Substrate

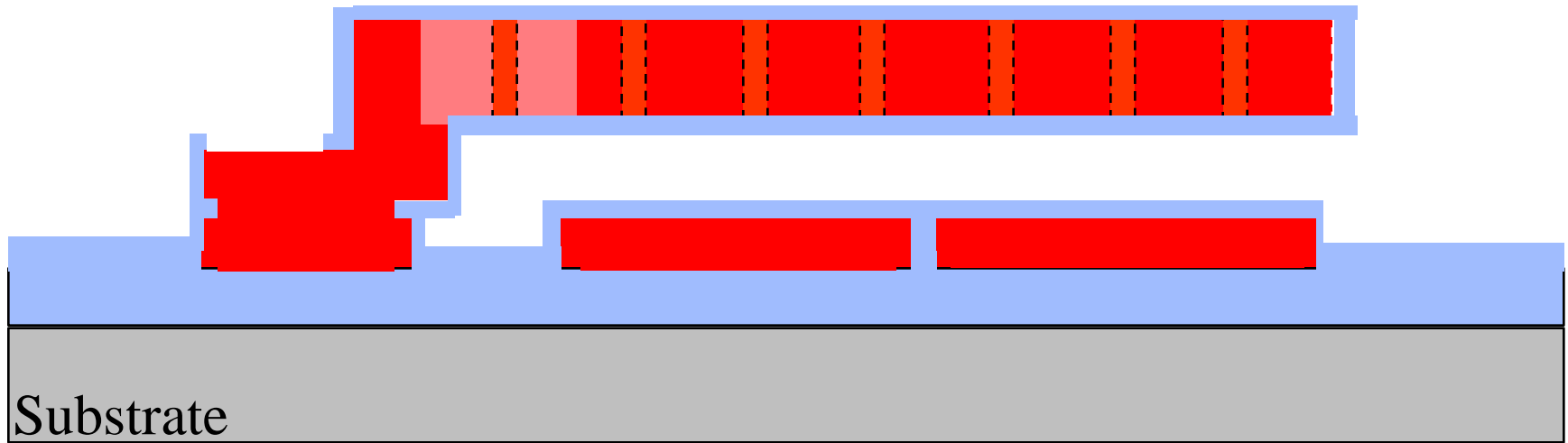


*AFTER POLY REOX*



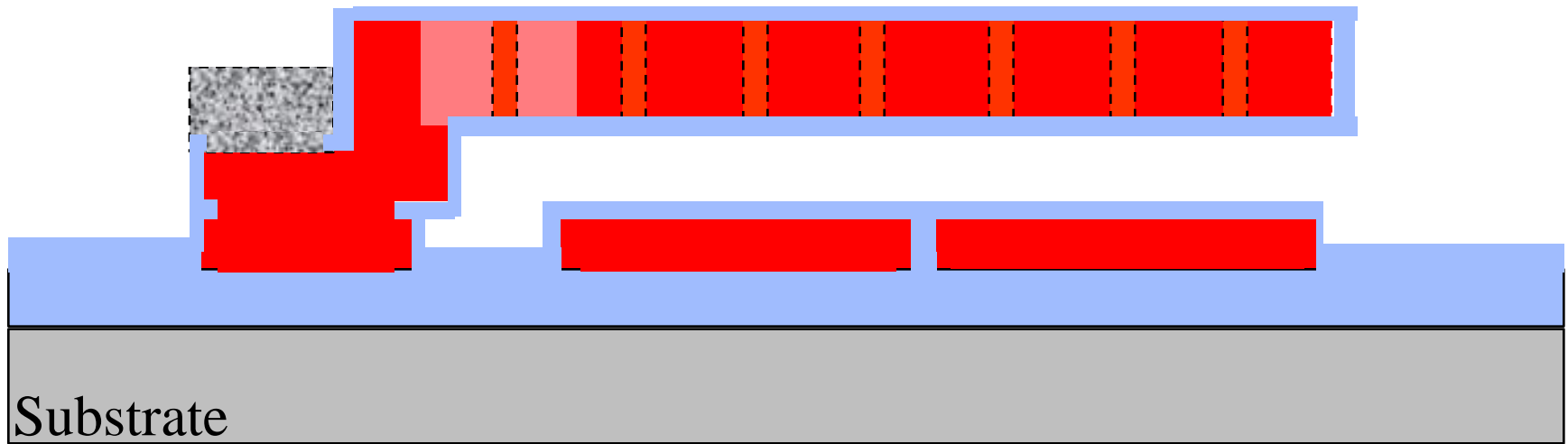
Substrate

CC



Substrate

*CANTILEVER, MIRROR OR ACCELEROMETER*

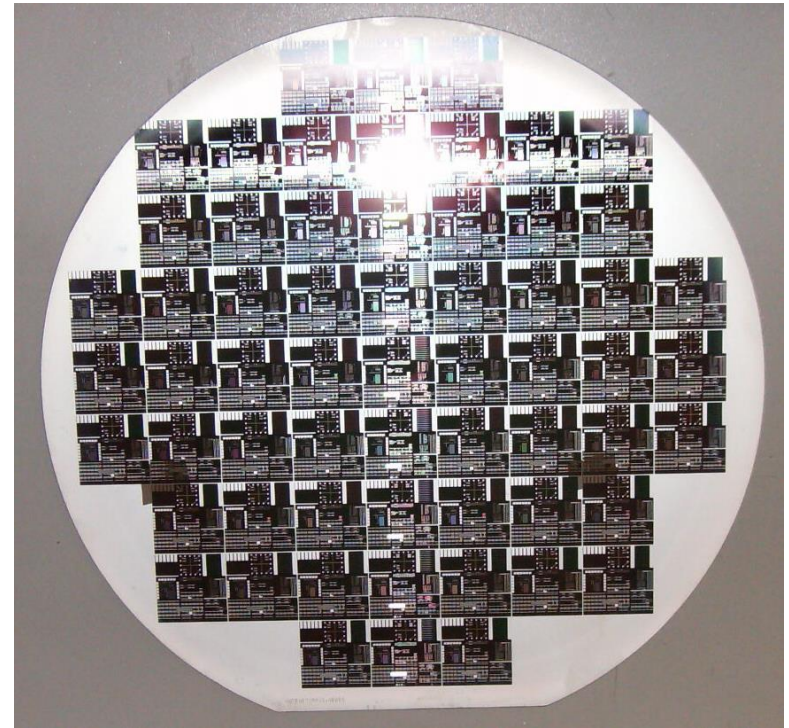


Substrate

*ALUMINUM ETCH USING LAM4600*



LAM4600



*Rochester Institute of Technology  
Microelectronic Engineering*

# LAM4600 ANISOTROPIC ALUMINUM ETCH

Step	1	2	3	4	5
Pressure	100	100	100	100	0
RF Top (W)	0	0	0	0	0
RF Bottom	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
O2 111	0	0	0	0	0
N2 222	13	13	20	25	25
BCI 333	50	50	25	25	0
Cl2 444	10	10	30	23	0
Ar 555	0	0	0	0	0
CFORM666	8	8	8	8	8
Complete	Stabl	Time	Time	Oetch	Time
Time (s)	15	8	230	10%	15

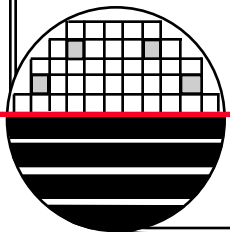


Channel	B
Delay	130
Normalize	10 s
Norm Val	5670
Trigger	105%
Slope	+

Fuller, May 2010

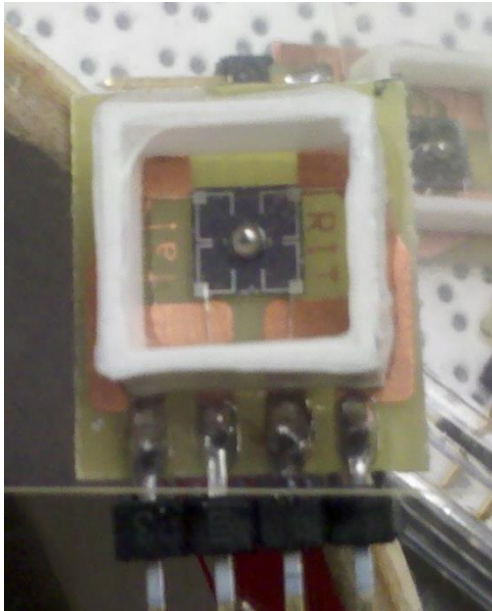
Rochester Institute of Technology  
Microelectronic Engineering

*SINTER*

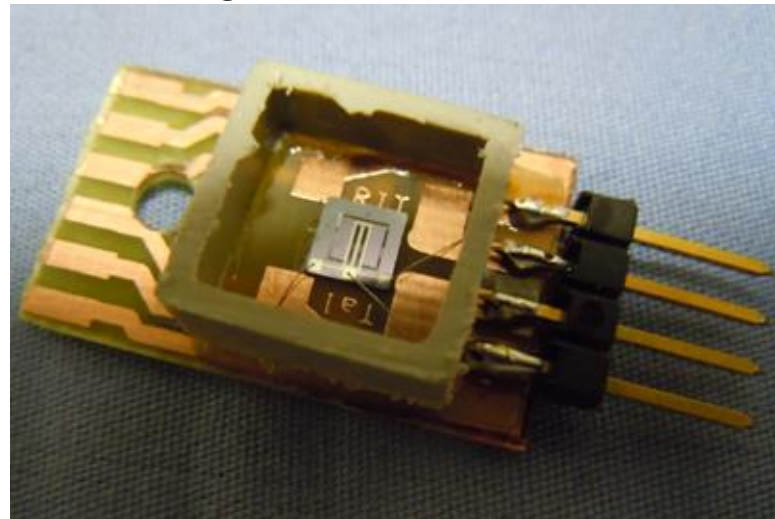


# *SOME EXAMPLES OF PACKAGED DEVICES*

## Magnetic Proximity Sensor

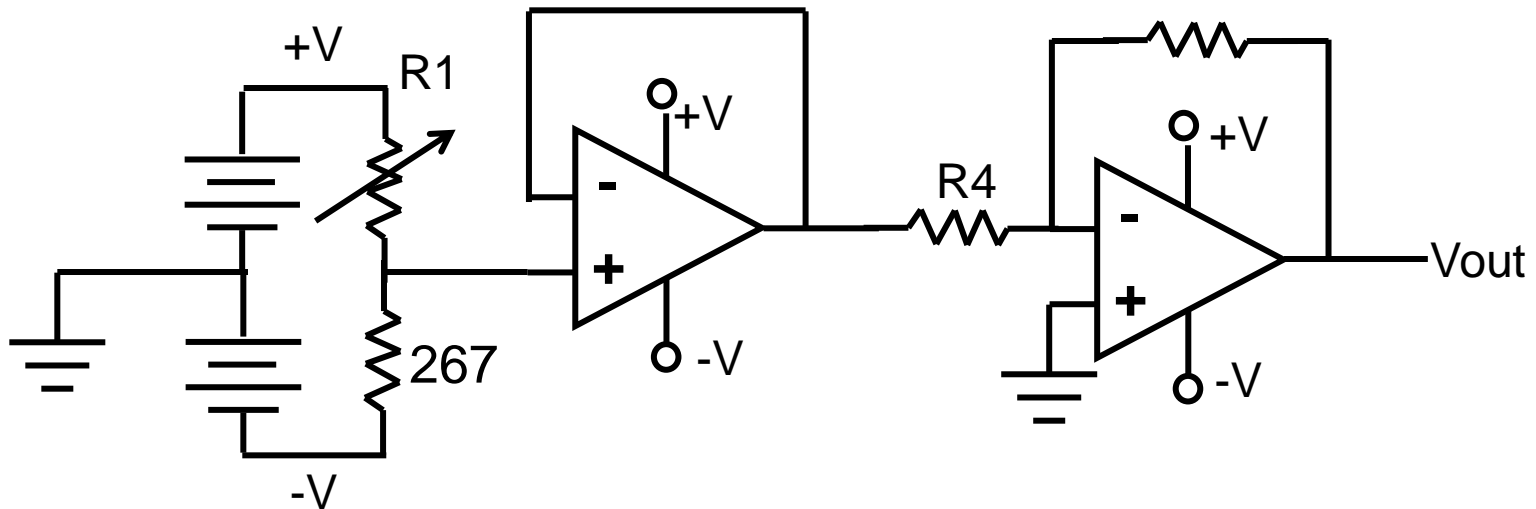


## Packaged Accelerometer





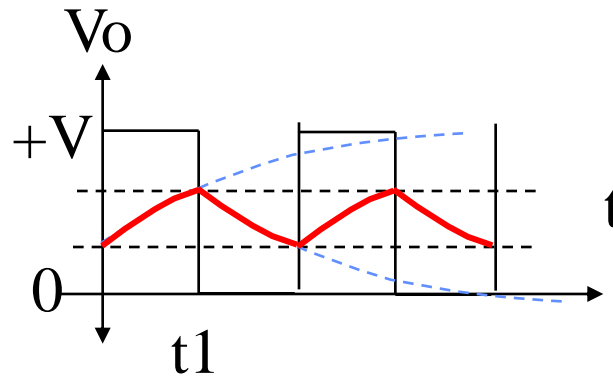
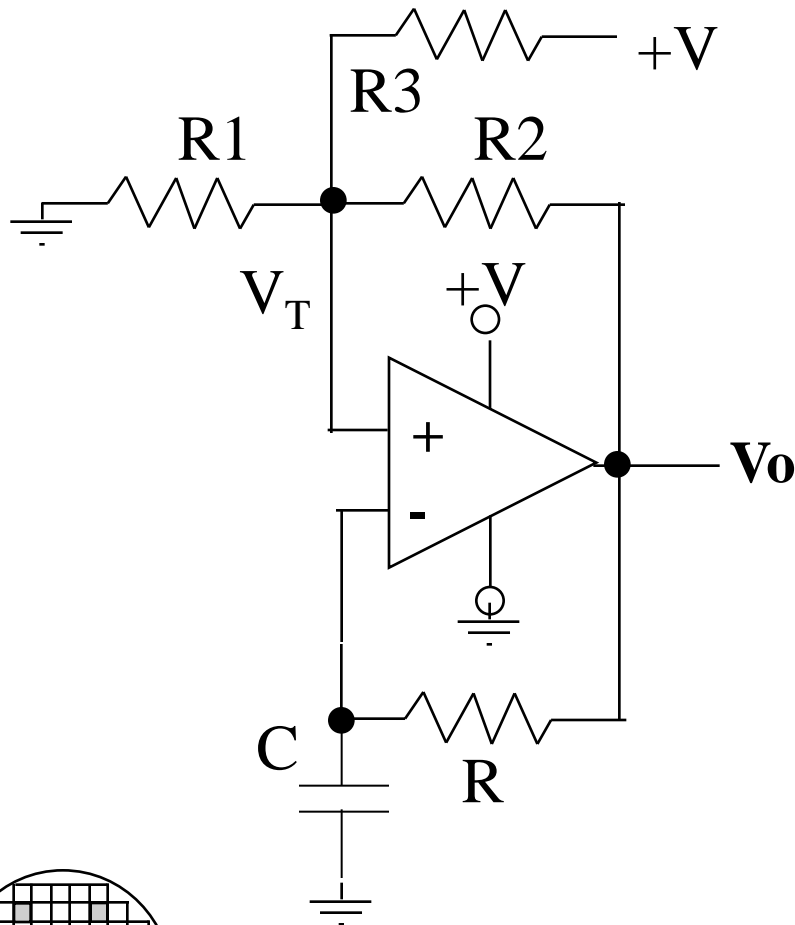
**SINGLE RESISTOR SENSOR AMPLIFIER DESIGN**



0.00004%/° C with gain of 1000 and 100C

$$V_{out} = \frac{V(1.004)}{(2.004 - 1/2)} = 3mV$$

# SINGLE SUPPLY OSCILLATOR (MULTIVIBRATOR)



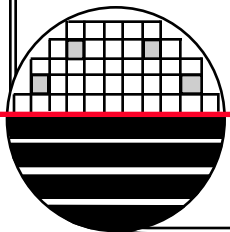
Let  $R1 = 100K$ ,  $R2=R3=100K$   
and  $+V = 3.3$

Then  $V_T = 2.2$  when  $V_o = 3.3$

$V_T = 1.1$  when  $V_o = 0$

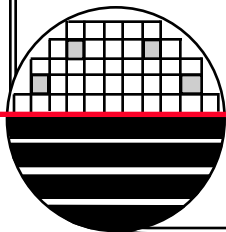
*SUMMARY*

CMOS Compatible?



## *REFERENCES*

1. Dr. Lynn Fuller's webpage
2. more



## ***HOMEWORK – FABRICATION DETAILS***

1. Draw a series of pictures that show the crosssection and layout for your design project. From starting wafer to sinter. Not all of the 43 steps but for most of the steps.
2. Provide a list of all recipes and a short description.
3. What data should be collected ie. at step 7 record oxide thickness, at step 9 take picture of resolution, at step ? .....
4. Discuss how your device will be packaged.
5. Discuss how the devices you make will be tested. Describe any electronic circuits

