RIT’s Sub-CMOS Process
(Leff < 1.0 µm)

Dr. Lynn Fuller
Suraj Bhaskaran and Ivan Puchades
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
Email: Lynn.Fuller@rit.edu
Webpage: http://people.rit.edu/lffeee

8-17-14 SubCmos2014.ppt

ADOBE PRESENTER

This PowerPoint module has been published using Adobe Presenter. Please click on the Notes tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the play arrow or pressing the page down key.

OUTLINE

Introduction

Process Description

Well Doping Calculations

Layout Design Layers and Masks

Subμ CMOS Process Details

INTRODUCTION

RIT is supporting two different CMOS process technologies. The older p-well CMOS and SMFL-CMOS have been phased out. The SUB-CMOS process is used for standard 3 Volt Digital and Analog integrated circuits. This is the technology of choice for teaching circuit design and fabricating CMOS circuits at RIT. The ADV-CMOS process is intended to introduce our students to process technology that is close to industry state-of-the-art. This process is used to build test structures and develop new technologies at RIT.

RIT p-well CMOS	$\lambda = 4\ \mu m$	Lmin = 8 μm
RIT SMFL-CMOS	$\lambda = 1\ \mu m$	Lmin = 2 μm
RIT Subμ-CMOS	$\lambda = 0.5\ \mu m$	Lmin = 1.0 μm
RIT Advanced-CMOS	$\lambda = 0.25\ \mu m$	Lmin = 0.5 μm

MAJOR CONSIDERATIONS

Well Doping
Substrate Doping and Type
Well Formation
Channel Stop
Isolation Technology
Gate Oxide Thickness
Gate Doping
Threshold Voltages
Side Wall Spacers and Low Doped Drain (LDD)
Drain/Source Junction Depth
Well Contacts
Silicides
Metal Technology

WELL/JUNCTION CALCULATIONS

Built in Voltage: $\Psi_o = 0.55 + KT/q \ \ \ln (N/ni)$

Width of Space Charge Layer, W on lightly doped side: $Wsc = [\,(2\varepsilon/q)\,(\Psi_o + V_R)\,(1/N\,)]^{1/2}$

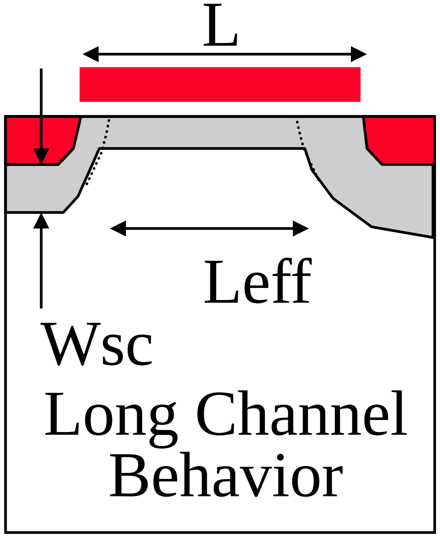
Maximum Electric Field: $E_o = -\ [(2q/\varepsilon)\,(\Psi_o + V_R)\,(N\,)]^{1/2}$

Example:

$\Psi_o = 0.55 + 0.026 \ln (3E16/1.45E10) = 0.96$

$Wsc = [\,(2(11.7)(8.85E{-}14)/1.6E{-}19)\,(0.96)\,(1/3E16\,)]^{1/2}$
$= 0.20\ \mu m$ or $0.43\mu m$ @ $V_R=3.3V$

Leff = 1.0-0.20-0.43 = ~ 0.37 µm



$Eo = -\ [(2(8.85E{-}14(11.7))(0.96+3.3)(3E16)]^{1/2}$
$= -1.99E5\ V/cm$

$\varepsilon = \varepsilon_o\,\varepsilon_r = 8.85E{-}12\ \ (11.7)\ F/m$
$8.85E{-}14\ (11.7)\ F/cm$

Note: Eomax = 3E5 V/cm

WELL/JUNCTION CALCULATIONS FOR LDD

Built in Voltage: $\Psi_o = KT/q \ln (Na\ Nd/ni^2)$

Width of Space Charge Layer: $Wsc = [(2\varepsilon/q)(\Psi_o + V_R)(1/Na + 1/Nd)]^{1/2}$

Electric Field: $E_o = - [(2q/\varepsilon)(\Psi_o + V_R)(NaNd/(Na+Nd))]^{1/2}$

Example:

$\Psi_o = 0.026 \ln (3E16\ 3E16/1.45E10^2) = 0.75$

$Wsc\ @\ 0V = [(2(11.7)(8.85E{-}14)/1.6E{-}19)(0.75)(1/3E16+1/3E16)]^{1/2}$

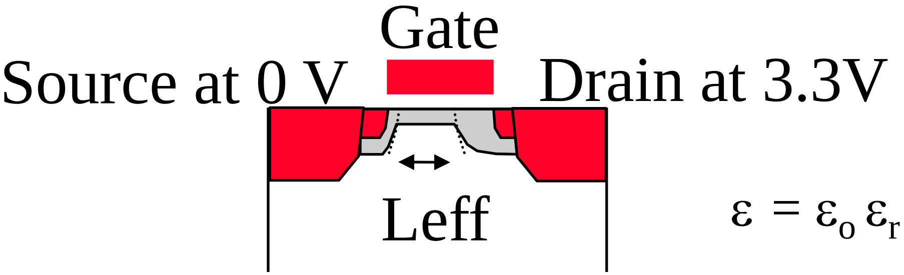
= 0.26 µm and 0.13 µm on each side of the junction

$Wsc\ @\ 3.3V = [(2(11.7)(8.85E{-}14)/1.6E{-}19)(0.75+3.3)(1/1.5E16)]^{1/2}$

= 0.60 µm and 0.30 µm on each side of the junction

$Eo = - [(2(8.85E{-}14(11.7))(0.75+3.3)(1.5E16)]^{1/2}$

=-1.37E5V/cm



$\varepsilon = \varepsilon_o\, \varepsilon_r = 8.85E{-}12\ (11.7)\ F/m$

Leff = 1.0-0.13-0.30 = ~ 0.57µm

Quiz 1 Question 1: Increasing the well surface concentration will

○ **A) result in larger space charge layer in the MOSFET**

● **B) allow for smaller MOSFET's**

○ **C) not change Leff of the MOSFET**

Your answer:

You did not answer this question completely

The correct ans

You must answer the question before continuing

Correct - Click anywhere to continue

Incorrect - Click anywhere to continue

Submit

Clear

Quiz 1 Question 2: Low Doped Drain/Source provides

○ **A) larger space charge layer widths, lower electric field, smaller Leff**

○ **B) smaller space charge layer widths, larger electric field, smaller Leff**

● **C) larger space charge layer widths, lower electric field, Larger Leff**

○ **D) smaller space charge layer widths, larger electric field, smaller Leff**

Correct - Click anywhere to cont

Incorrect - Click anywhere to

Your answer:

You did not answer this question

You must answer the question before continuing

Submit

Clear

Quiz1

Your Score	{score}
Max Score	{max-score}
Number of Quiz Attempts	{total-attempts}

Question Feedback/Review Information Will Appear Here

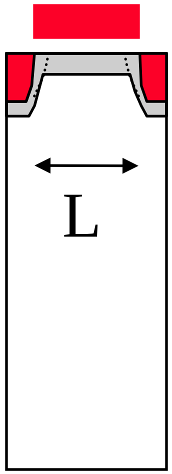
Continue

Review Quiz

RIT SUBμ CMOS

RIT Subμ CMOS

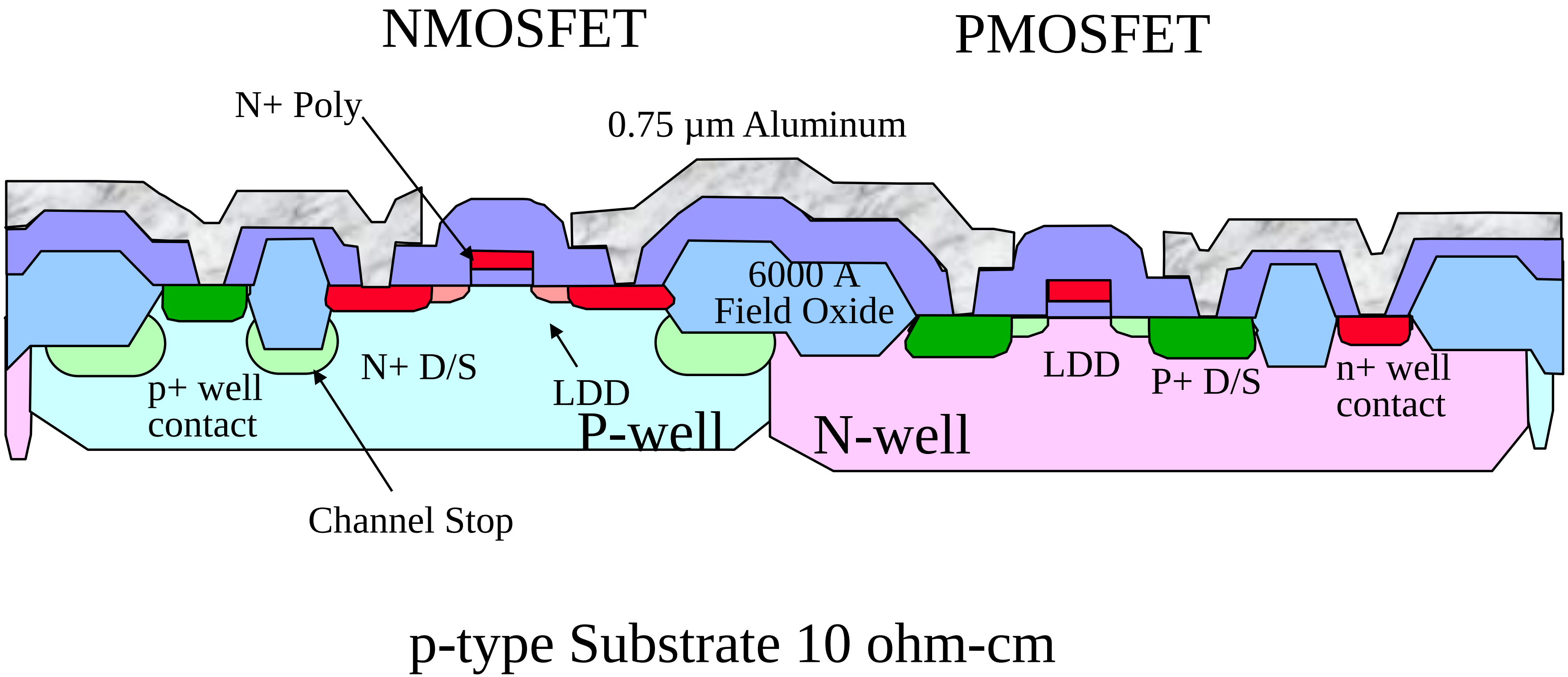
150 mm wafers – p-type
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 μm
Np-well = 1E16 cm-3
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
n-type Poly on both transistors
Lmin= 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum



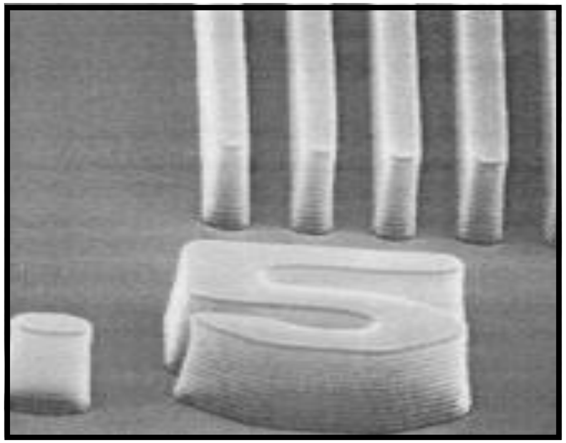
Long
Channel
Behavior

3.3 Volt Technology
VT's = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)

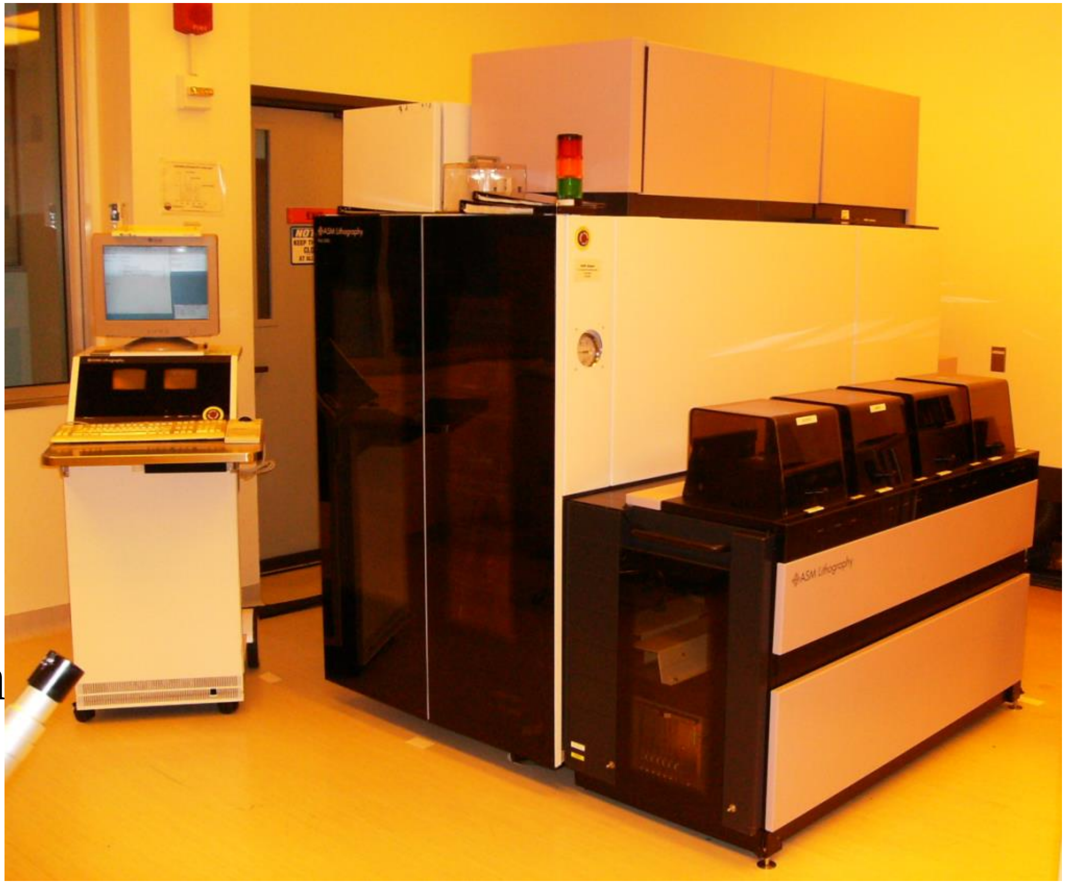
RIT SUBμ CMOS



ASML 5500/200 STEPPER

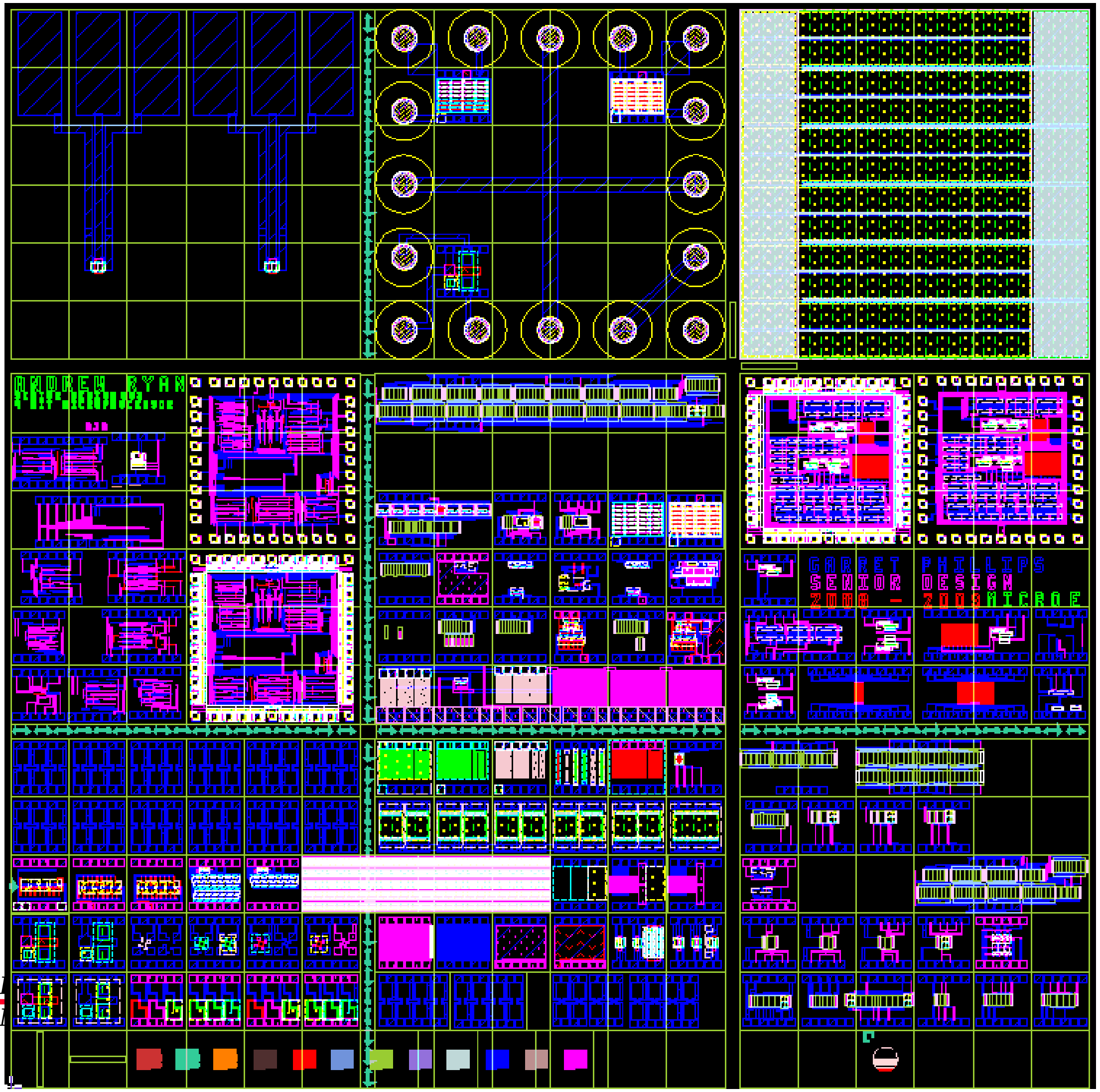


NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35µm
for NA=0.6, σ =0.85
Depth of Focus = $k_2 \lambda/(NA)^2$
= > 1.0 µm for NA = 0.6



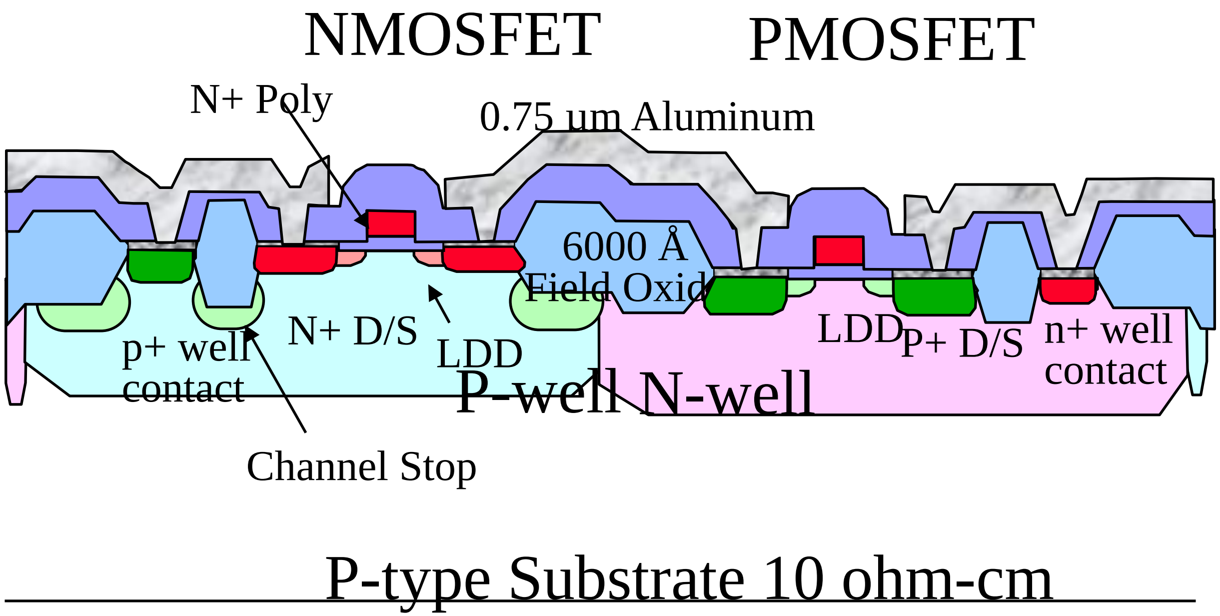
i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

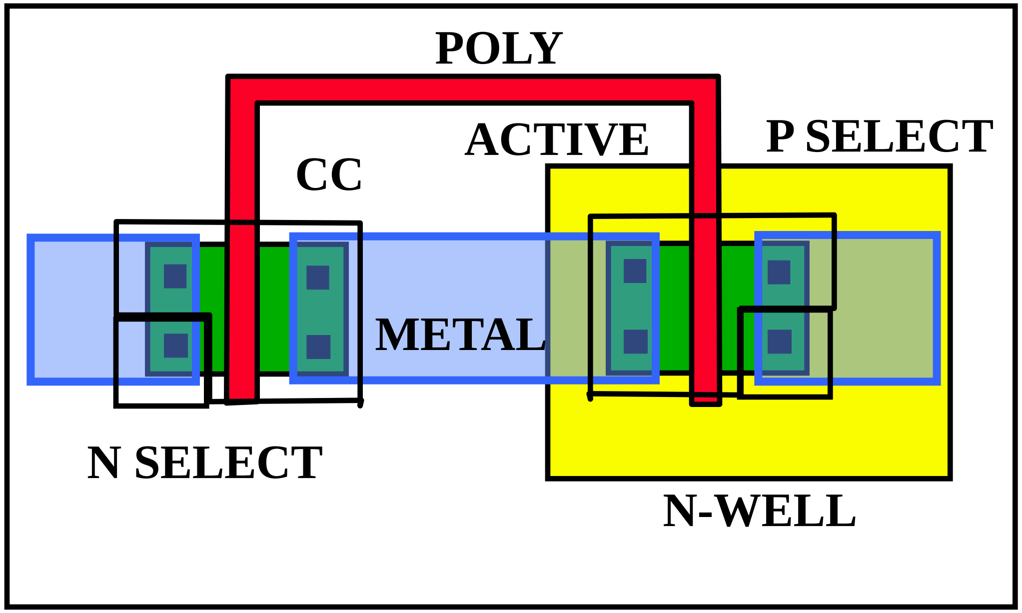
JOHN GALT CMOS TESTCHIP

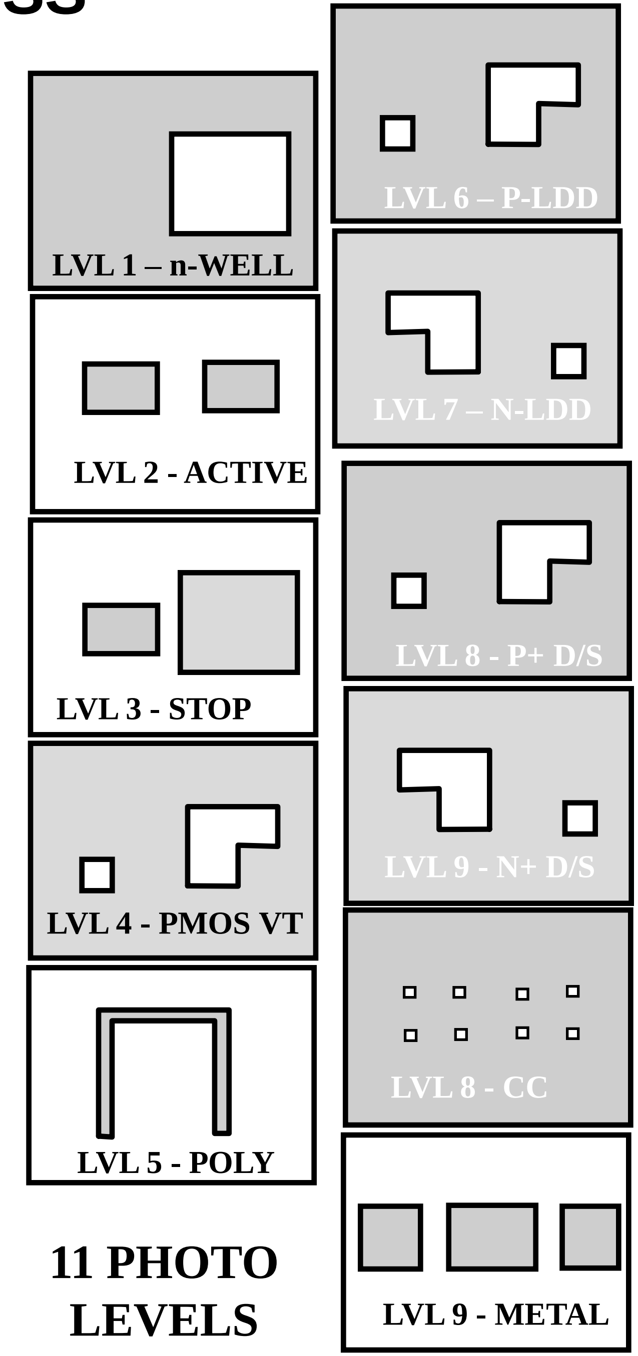


2010

RIT SUB-CMOS PROCESS

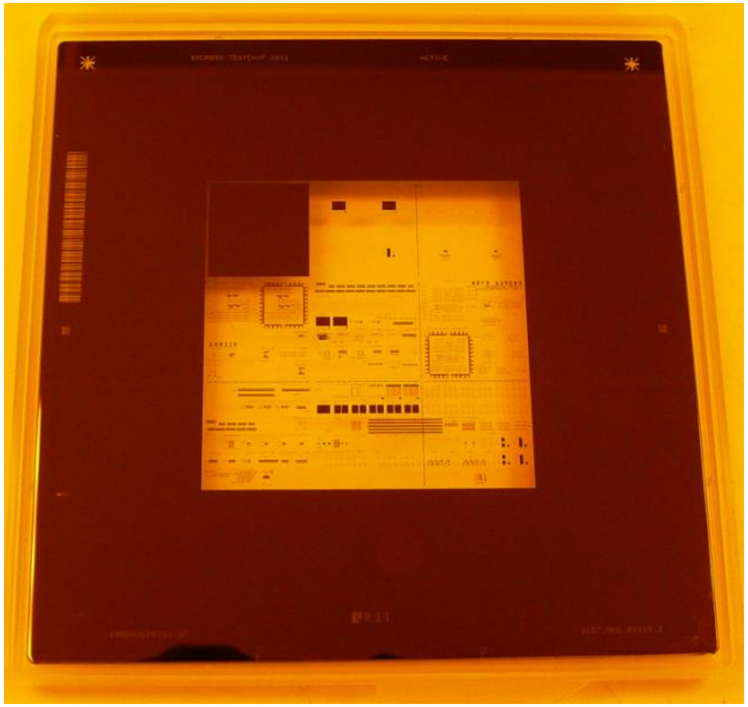




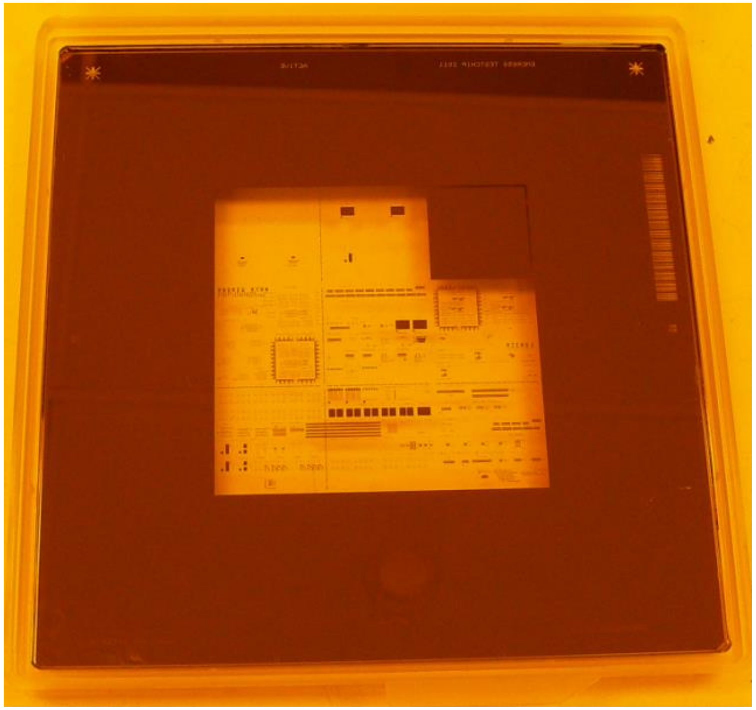


11 PHOTO LEVELS

ASML MASK



Chrome Side
Mirrored 90°
Chip Bottom at Bottom



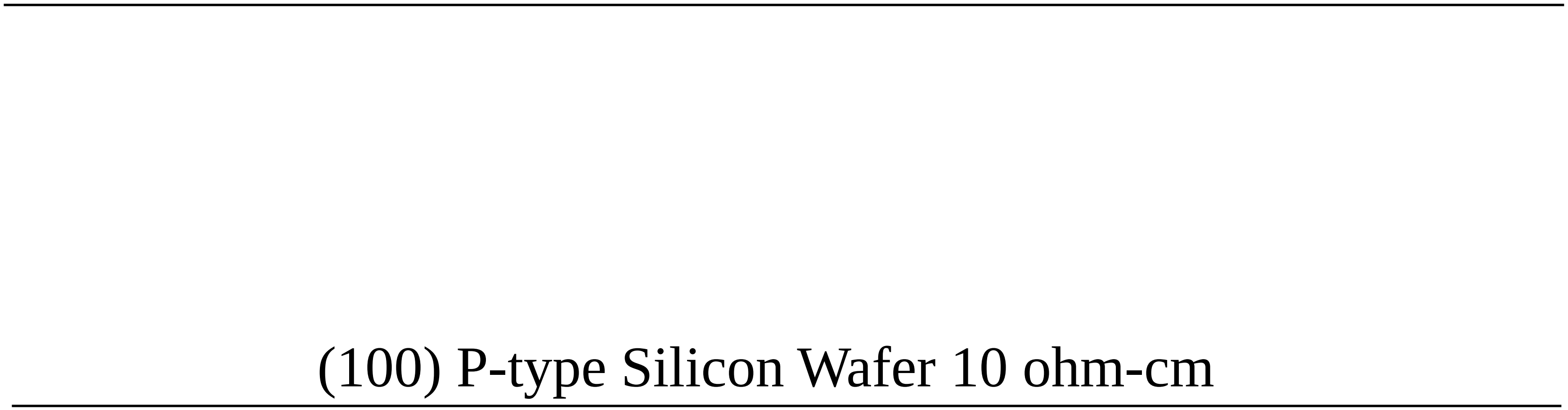
Non Chrome Side
As loaded into Reticle Pod, Chrome Down, Reticle Pre-Alignment Stars Sticking out of Pod

SUB-CMOS 150 PROCESS

SUB-CMOS Versions 150

1. CL01
2. OX05--- pad oxide, Tube 4
3. CV02- Si3N4-1500Å
4. PH03 –1- JG nwell
5. ET29 – Nitride Etch
6. IM01 – n-well
7. ET07 – Resist Strip
8. CL01
9. OX04 – well oxide, Tube 1
10. ET19 – Hot Phos Si3N4
11. IM01 – p-well
12. OX06 – well drive, Tube 1
13. ET06 - Oxide Etch
14. CL01
15. OX05 – pad oxide, Tube 4
16. CV02 – Si3N4 -1500 Å
17. PH03 – 2 – JG Active
18. ET29 – Nitride Etch
19. ET07 – Resist Strip
20. PH03 - -Pwell Stop
21. IM01- stop
22. ET07 Resist Strip
23. CL01
24. OX04 – field, Tube 1
25. ET19 – Hot Phos Si3N4
26. ET06 – Oxide Etch
27. OX04 – Kooi, Tube 1
28. IM01 – Blanket Vt
29. PH03 – 4-PMOS Vt Adjust
30. IM01 - Vt
31. ET07 – Resist Strip
32. ET06 – Oxide Etch
33. CL01
34. OX06 – gate, Tube 4
35. CV01 – Poly 5000A
36. IM01 - dope poly
37. OX08 – Anneal, Tube 3
38. DE01 – 4 pt Probe
39. PH03-5-JG poly
40. ET08 – Poly Etch
41. ET07 – Resist Strip
42. PH03 – 6 - n-LDD
43. IM01
44. ET07 – Resist Strip
45. PH03 – 7 - p-LDD
46. IM01
47. ET07 – Resist Strip
48. CL01
49. CV03 –TEOS, 5000A
50. ET10 - Spacer Etch
51. PH03 – 8 - N+D/S
52. IM01 – N+D/S
53. ET07 – Resist Strip
54. PH03 – 9 P+ D/S
55. IM01 – P+ D/S
56. ET07 – Resist Strip
57. CL01 Special - No HF Dip
58. OX08 – DS Anneal, Tube 2
59. CV03 – TEOS, 4000A
60. PH03 – 10 CC
61. ET26 - CC Etch
62. ET07 – Resist Strip
63. CL01 Special - Two HF Dips
64. ME01 – Metal 1 Dep
65. PH03 -11- metal
66. ET15 – plasma Etch Al
67. ET07 Resist Strip
68. SI01 - Sinter
69. CV03 – TEOS- 4000Å
70. PH03 – VIA
71. ET26 – Via Etch
72. ET07 – Resist Strop
73. ME01 – Metal 2 Dep
74. PH03- M2
75. ET15 – plasma Etch Al
76. ET07 - Resist Strip
77. SEM1
78. TE01
79. TE02
80. TE03
81. TE04

STARTING WAFER

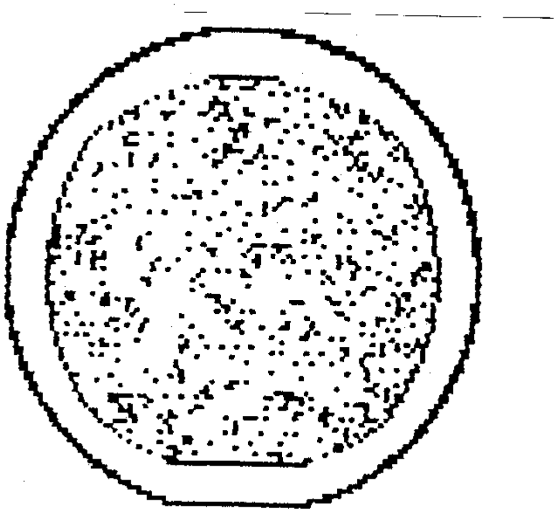


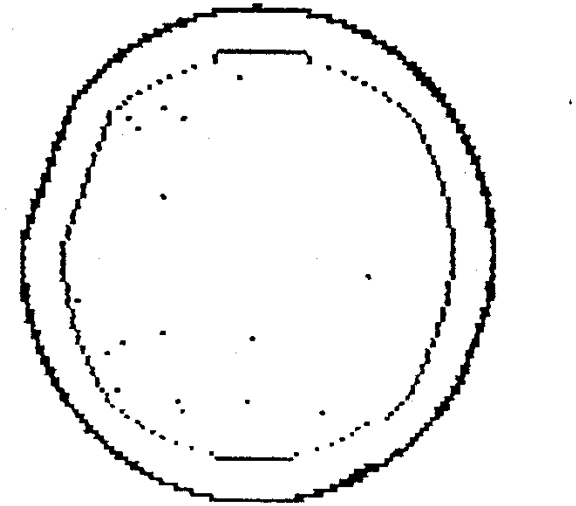
(100) P-type Silicon Wafer 10 ohm-cm

TENCORE SURF SCAN

Gives total surface particle count and count in 4 bins <0.5, 0.5 to 2.0, 2.0-10, >10. Bin boundary can be selected. Edge exclusion eliminated count from near the edge of the wafer.

EXAMPLE SURFACE PARTICLE COUNT DATA





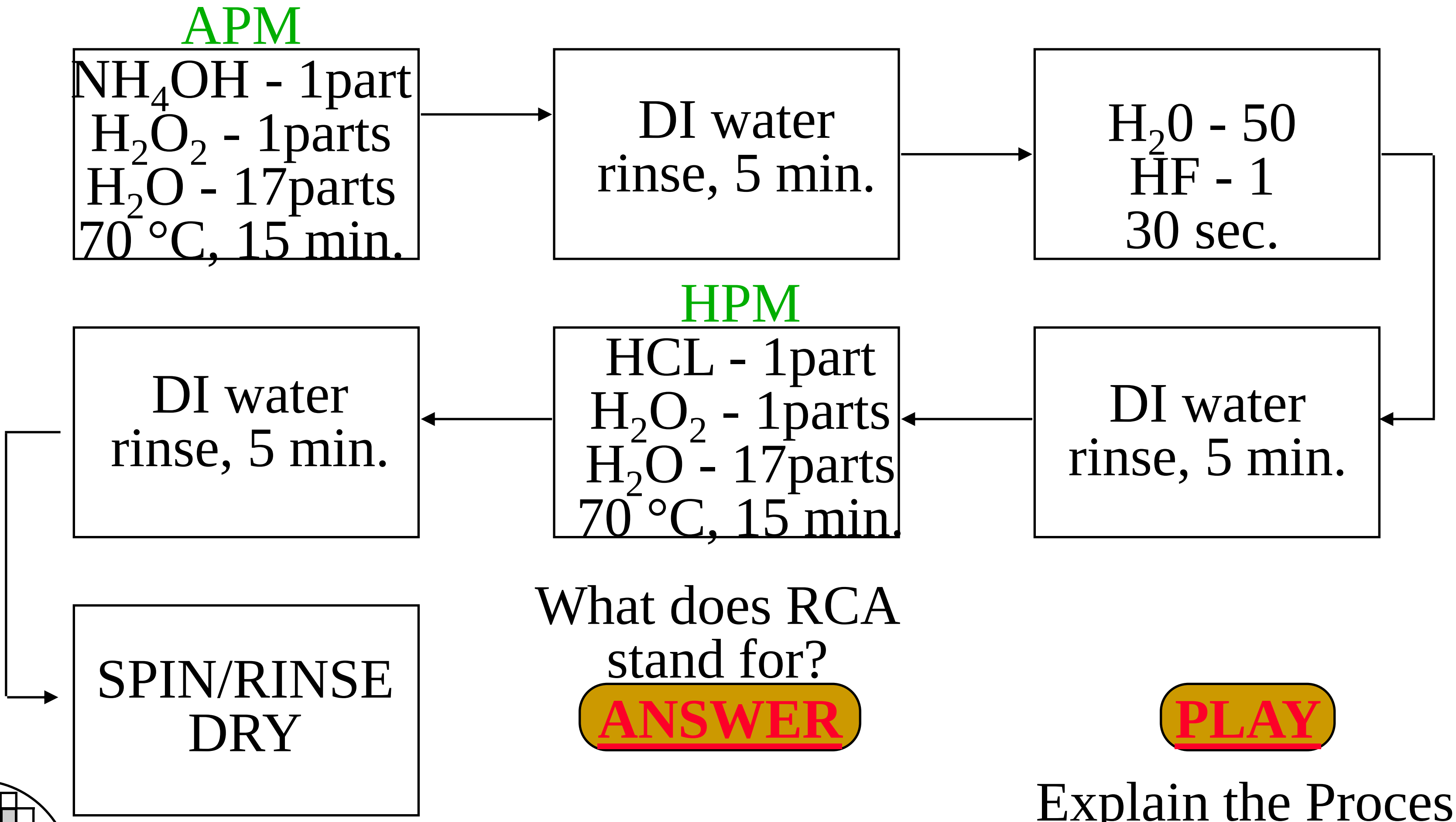
Before Cleaning (75 mm)

Size Range (µm)	Count
0.2 - 0.5	104
0.5 - 2.0	562
2.0 - 10	19
>10	2

After Cleaning (75 mm)

Size Range (µm)	Count
0.2 - 0.5	10
0.5 - 2.0	4
2.0 - 10	3
>10	0

RCA CLEAN



APM

NH_4OH - 1part
H_2O_2 - 1parts
H_2O - 17parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
30 sec.

DI water
rinse, 5 min.

HPM

HCL - 1part
H_2O_2 - 1parts
H_2O - 17parts
70 °C, 15 min.

DI water
rinse, 5 min.

SPIN/RINSE
DRY

What does RCA
stand for?

ANSWER

PLAY

Explain the Process

RCA CLEAN TOOLS

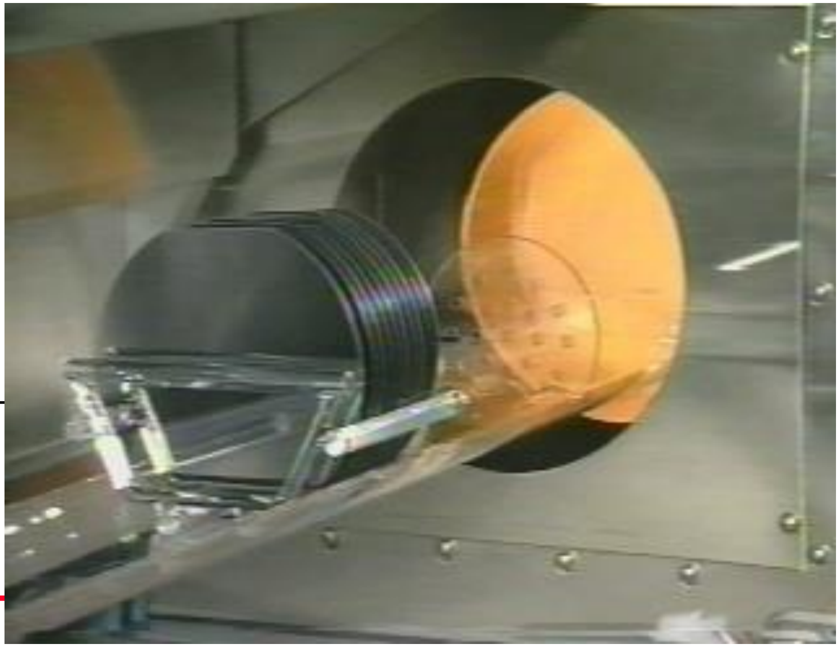
Megasonics Wet Bench
Spin/Rinse/Dry Tool (SRD)

PAD OXIDE GROWTH

Stress Relief for subsequent nitride layer
Etch stop for plasma etch of nitride
Screening oxide for n-well implant

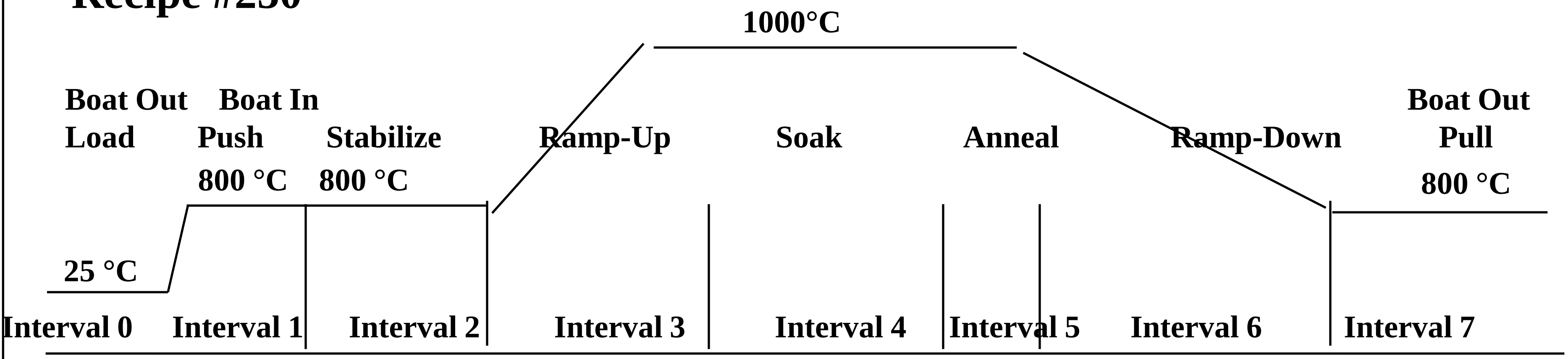
Pad Oxide, 500A
Bruce Furnace 04 Recipe 250

Substrate 10 ohm-cm



BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

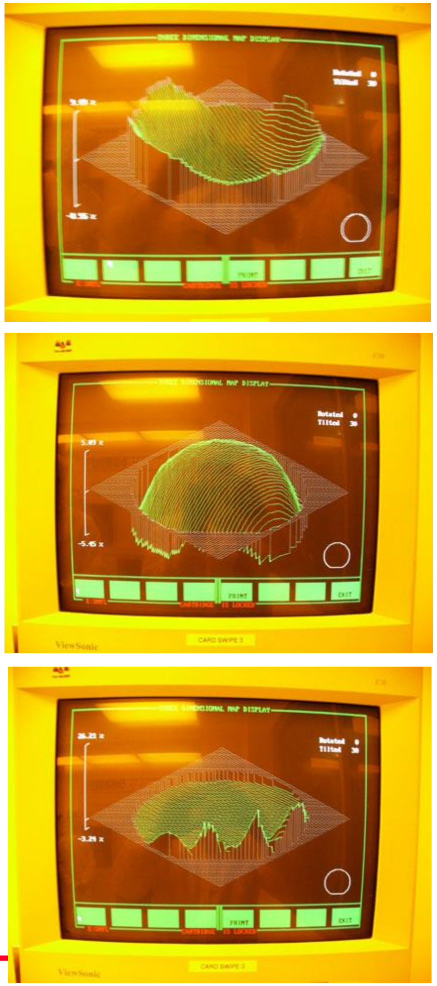
Recipe #250



Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Boat Out	Boat In						Boat Out
Load	Push	Stabilize	Ramp-Up	Soak	Anneal	Ramp-Down	Pull
25 °C	800 °C	800 °C		1000°C			800 °C
Any	12 min	15 min	20 min	40min	5min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

MEASURE OXIDE WITH TENCORE SPECROMAP



Record:

Mean
Std Deviation
Min
Max
No of Points

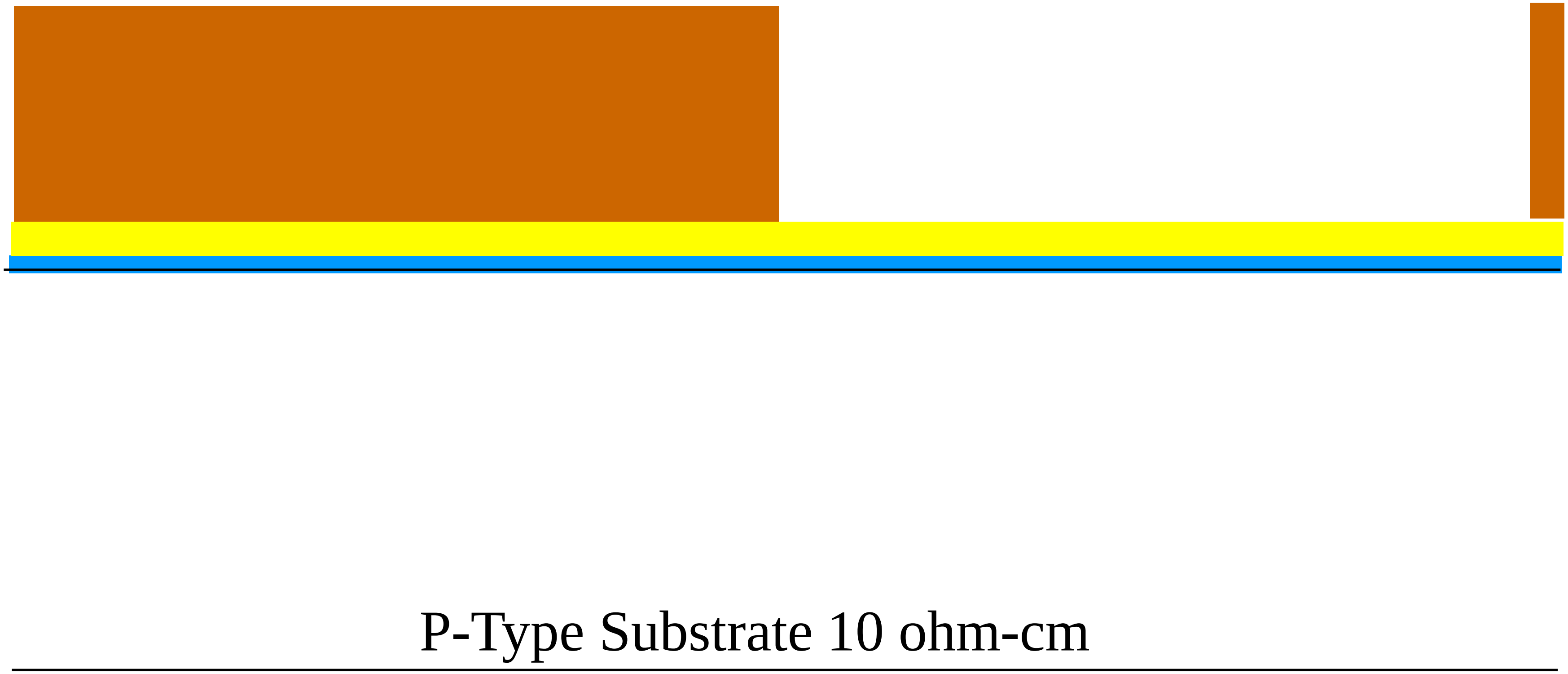
DEPOSIT SILICON NITRIDE

Nitride Target 1500A
LPCVD, 810C, Rate~60Å/min
Time~23 min

Recipe FACTORY NITRIDE 810
Temp = 810°C
Pressure = 400 mTorr
DCS Flow = 60 sccm
Ammonia Flow = 150 sccm

Substrate 10 ohm-cm

LEVEL 1 PHOTO - N-WELL



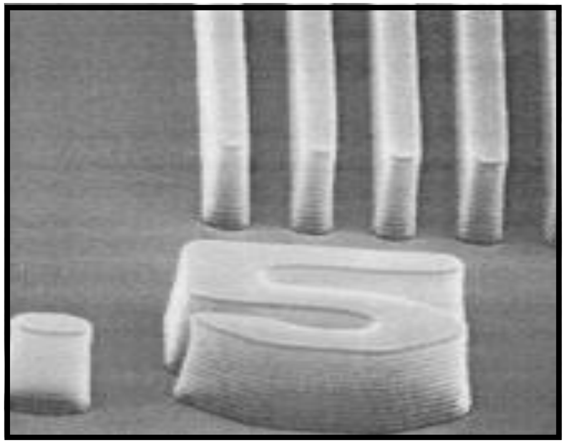
SSI COAT AND DEVELOP TRACK FOR 6” WAFERS

Use Recipe: Coat.rcp and Develop.rcp

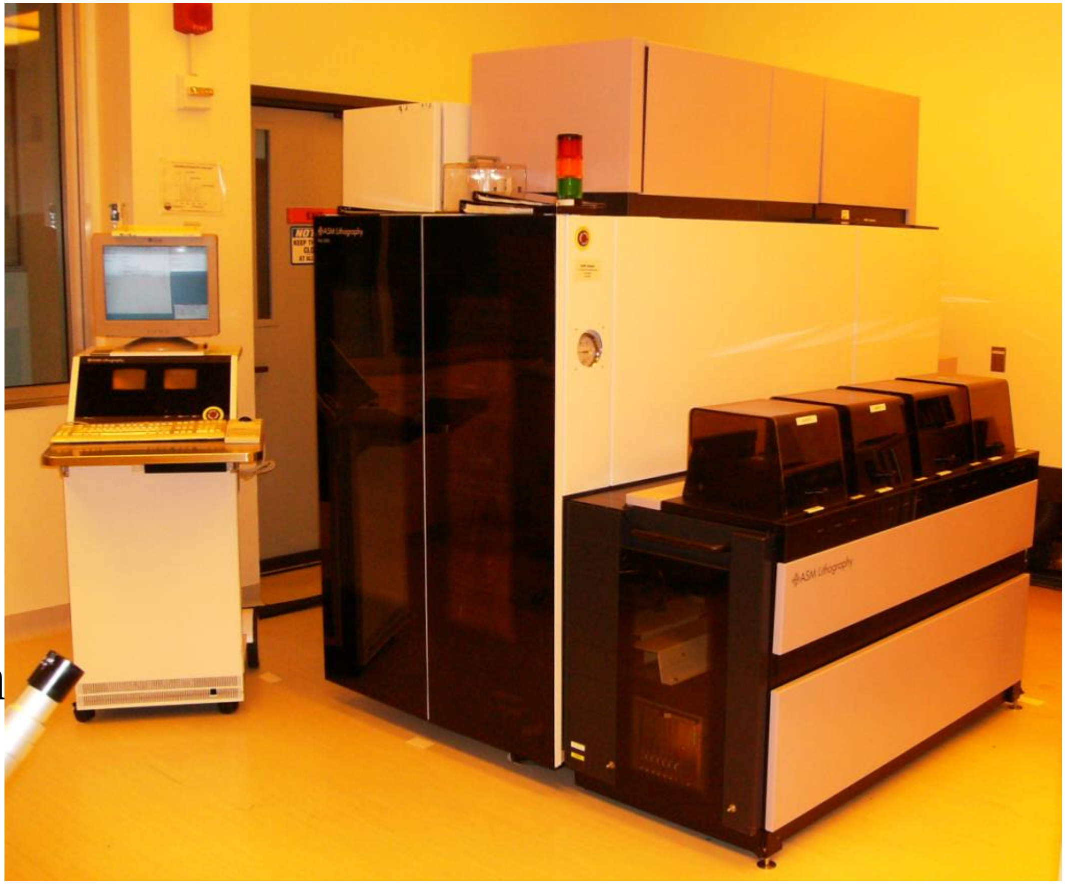
LITHOGRAPHY FOR SUB-CMOS 150 PROCESS

Lvl #	Level Name	Coat Recipe	Spin RPM	Xpr µm	Dose mj/cm^2	Dev Recipe	Dev Time	Hard Bake
1	Nwell	coat	3250	1.0	250	develop	50s	140C/1min
2	Active	coat	3250	1.0	250	devfac	60s	140C/1min
3	Stop	coat	3250	1.0	250	devfac	50s	140C/1min
4	pmosVt	coat	3250	1.0	250	devfac	60s	140C/1min
5	Poly	coat	3250	1.0	250	develop	50s	140C/1min
6	NLDD	coat	3250	1.0	250	develop	50s	140C/1min
7	PLDD	coat	3250	1.0	250	develop	50s	140C/1min
8	N+DS	coat	3250	1.0	250	develop	50s	140C/1min
9	P+DS	coat	3250	1.0	250	develop	50s	140C/1min
10	CC	coat	3250	1.0	250	devCC	120s	140C/1min
11	Metal 1	coatmtl	2000	1.3	250	devmtl	68s	140C/2min

ASML 5500/200

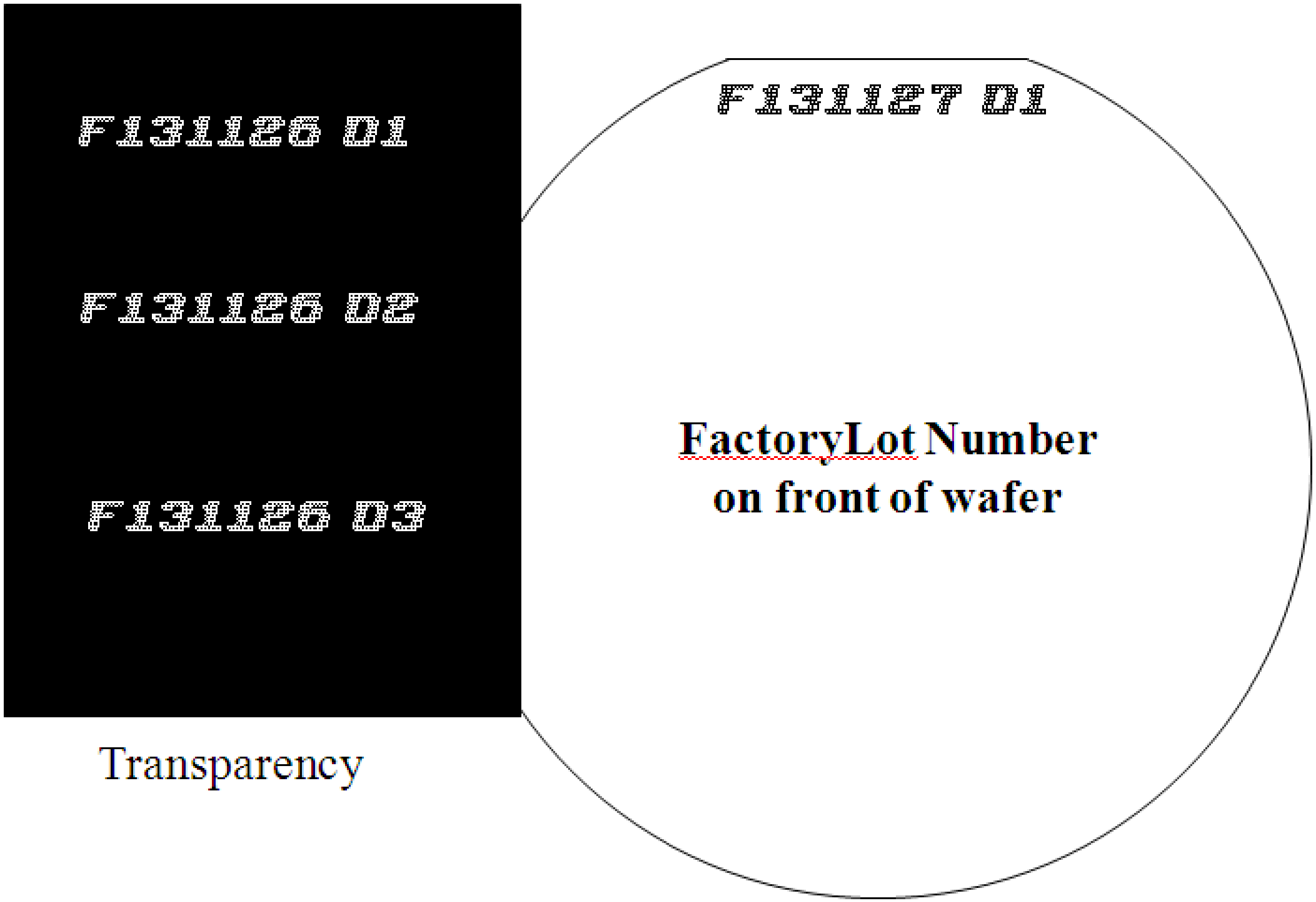


NA = 0.48 to 0.60 variable
σ= 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35µm
for NA=0.6, σ =0.85
Depth of Focus = k_2 $\lambda/(NA)^2$
= > 1.0 µm for NA = 0.6

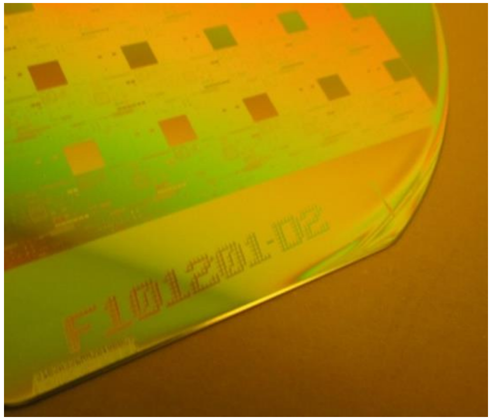


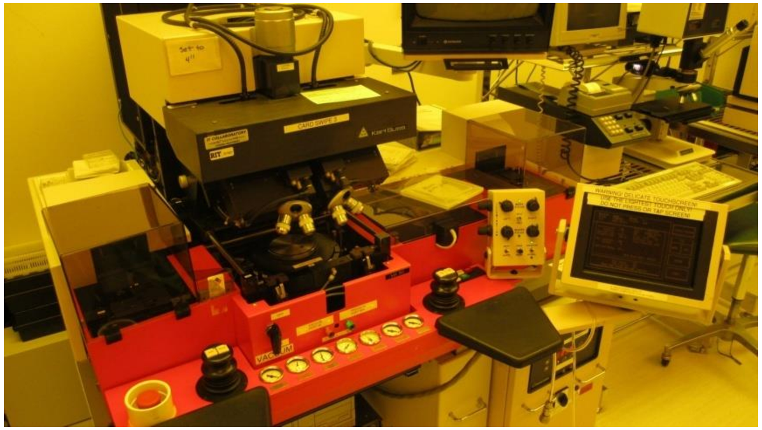
i-Line Stepper λ = 365 nm
22 x 27 mm Field Size

ADD WAFER IDNUMBER



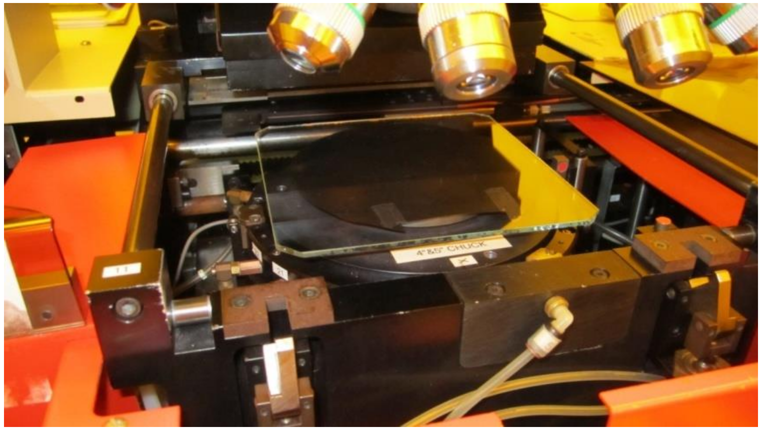
EXPOSE ID NUMBER ON FRONT OFWAFER





Karl Suss Aligner

After exposure in the ASML, place black plastic light shield with ID number (transparency) on the wafer. Use clear glass plate to hold flat and expose on Karl Suss Tool for 30s. Develop on SSI track.

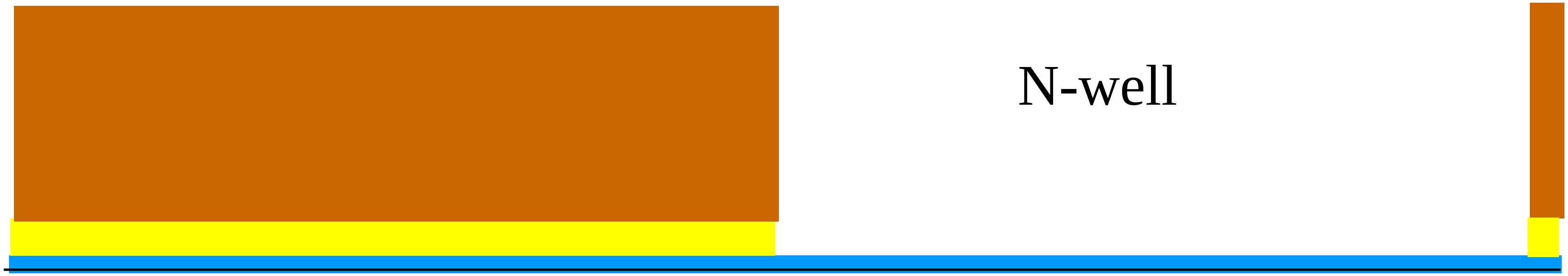


Wafer, Black Plastic Light Shield and Glass Plate on Karl Suss Chuck

MASK ID AND STEPPER JOB FOR JOHN GALT PRODUCT

Level #	Step#	Mask ID	Stepper Job	Level
1	4	JG NWELL	Factory Sub CMOS	Nwell
2	17	JG ACT	Factory Sub CMOS	Active
3	20	JG STOP	Factory Sub CMOS	Stop
4	29	JG VT	Factory Sub CMOS	pmosVt
5	39	JG POLY	Factory Sub CMOS	Poly
6	42	JG NLDD	Factory Sub CMOS	NLDD
7	45	JG PLDD	Factory Sub CMOS	PLDD
8	51	JG N+D/S	Factory Sub CMOS	N+DS
9	54	JG P+D/S	Factory Sub CMOS	P+DS
10	60	JG CC	Factory Sub CMOS	CC
11	65	JG M1	Factory Sub CMOS	Metal 1
12	70	JG VIA	Factory Sub CMOS	VIA
13	74	JG M2	Factory Sub CMOS	Metal 2

PLASMA ETCH NITRIDE



Nitride Etch: SF_6 plasma
LAM 490 Etcher, Etch Rate ~1000 Å/min

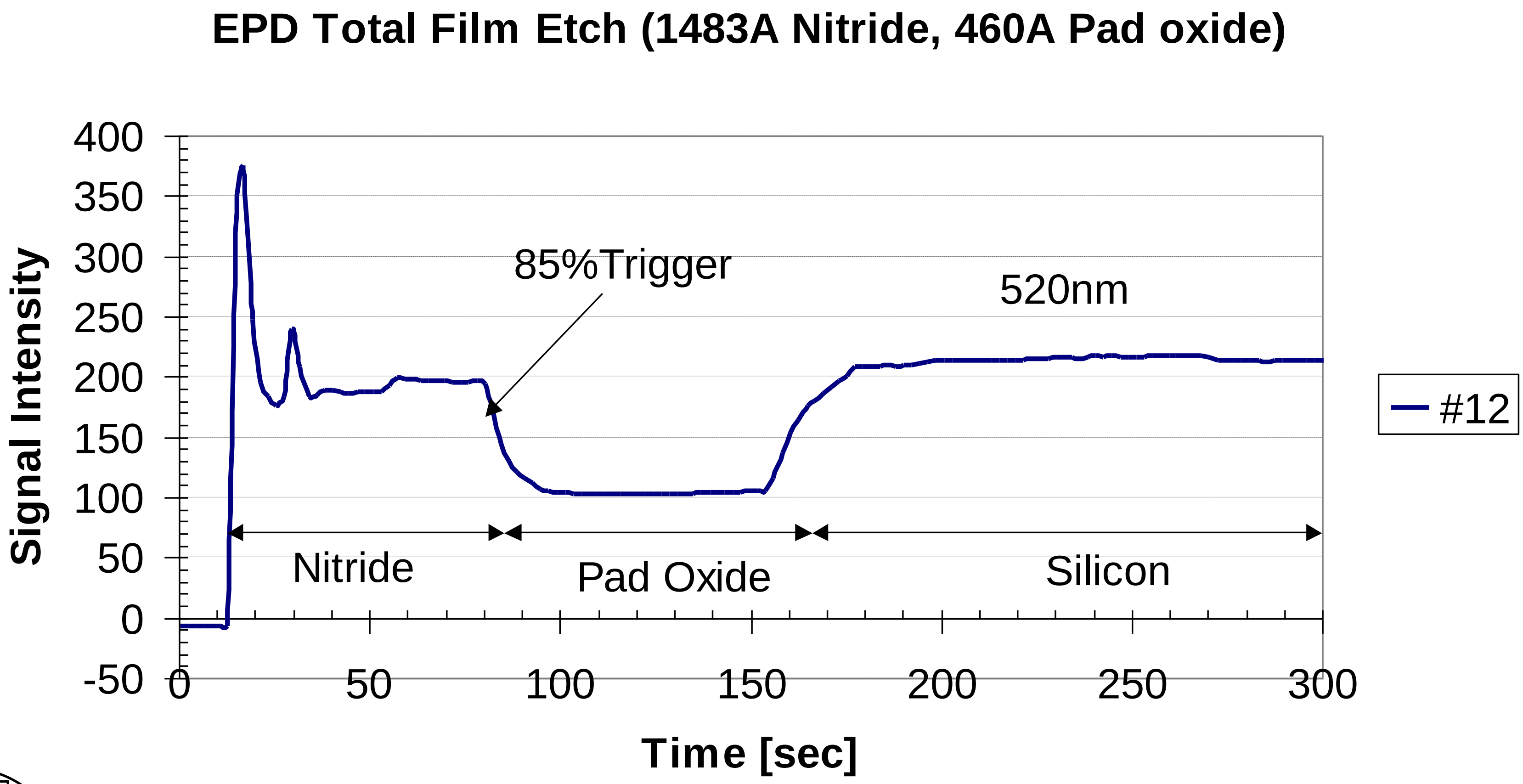
P-Type Substrate 10 ohm-cm

PLASMA ETCH TOOL

Lam 490 Etch Tool
Plasma Etch Nitride (~ 1500 Å/min)
SF_6 flow = 200 sccm
Pressure= 260 mTorr
Power = 125 watts
Time=thickness/rate

Use end point detection capability This system has filters at 520 nm and 470 nm. In any case the color of the plasma goes from pink/blue to white/blue once the nitride is removed.

LAM 490 END POINT

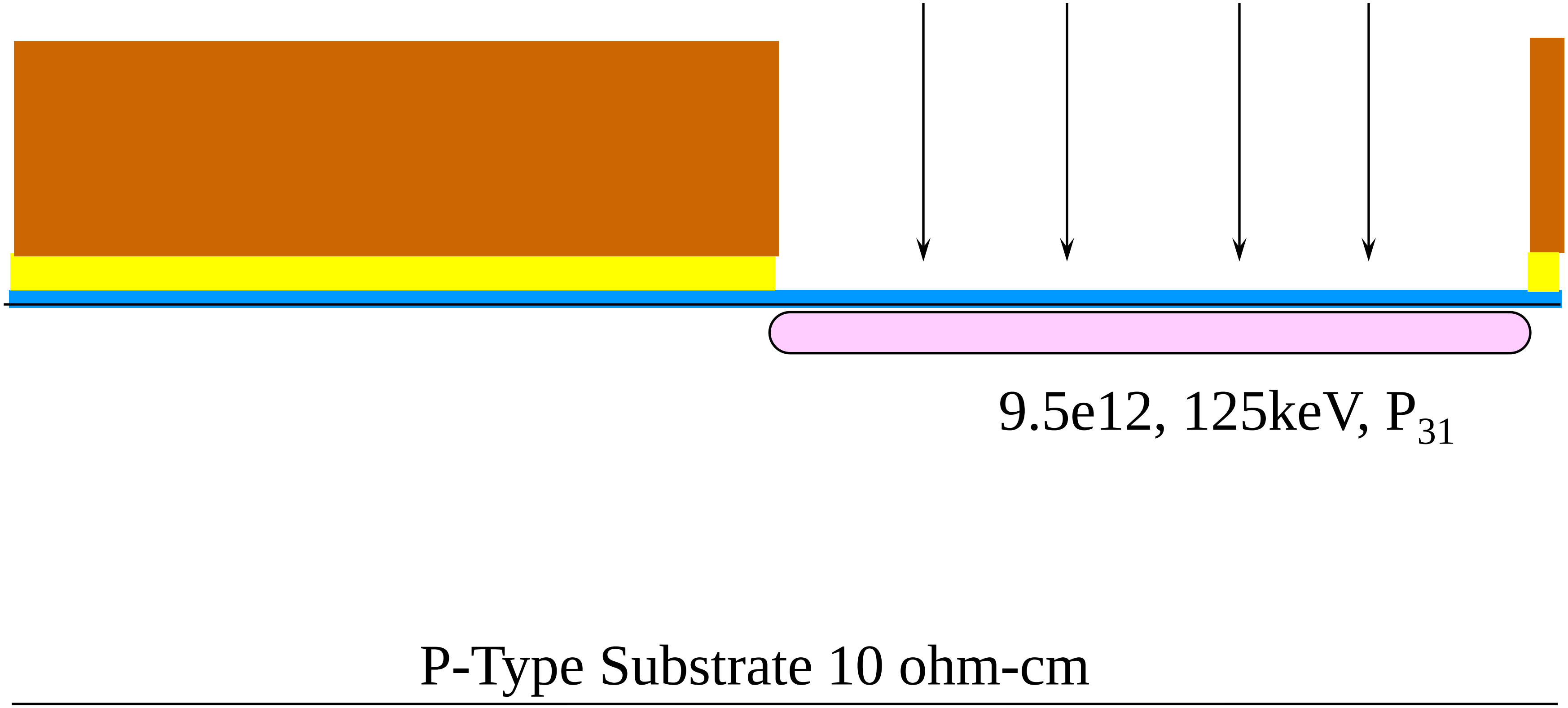


LAM 490 END POINT

Process: Step 1 – 260mTorr; 0W,
200sccm SF6,
Max Time = 1 min, Time Only
Process: Step 2 – 260mTorr; 125W,
200sccm SF6,
Max Time = 2min 30sec, Endpoint & Time
Process: Step 3 – 260mTorr; 125W,
200sccm SF6,
Over etch – 20%

Endpoint Parameters – Sampling A (ch12 @ 520nm)
Active during step 02
Delay 90sec before normalizing
Normalize for 10sec
Trigger at 90%

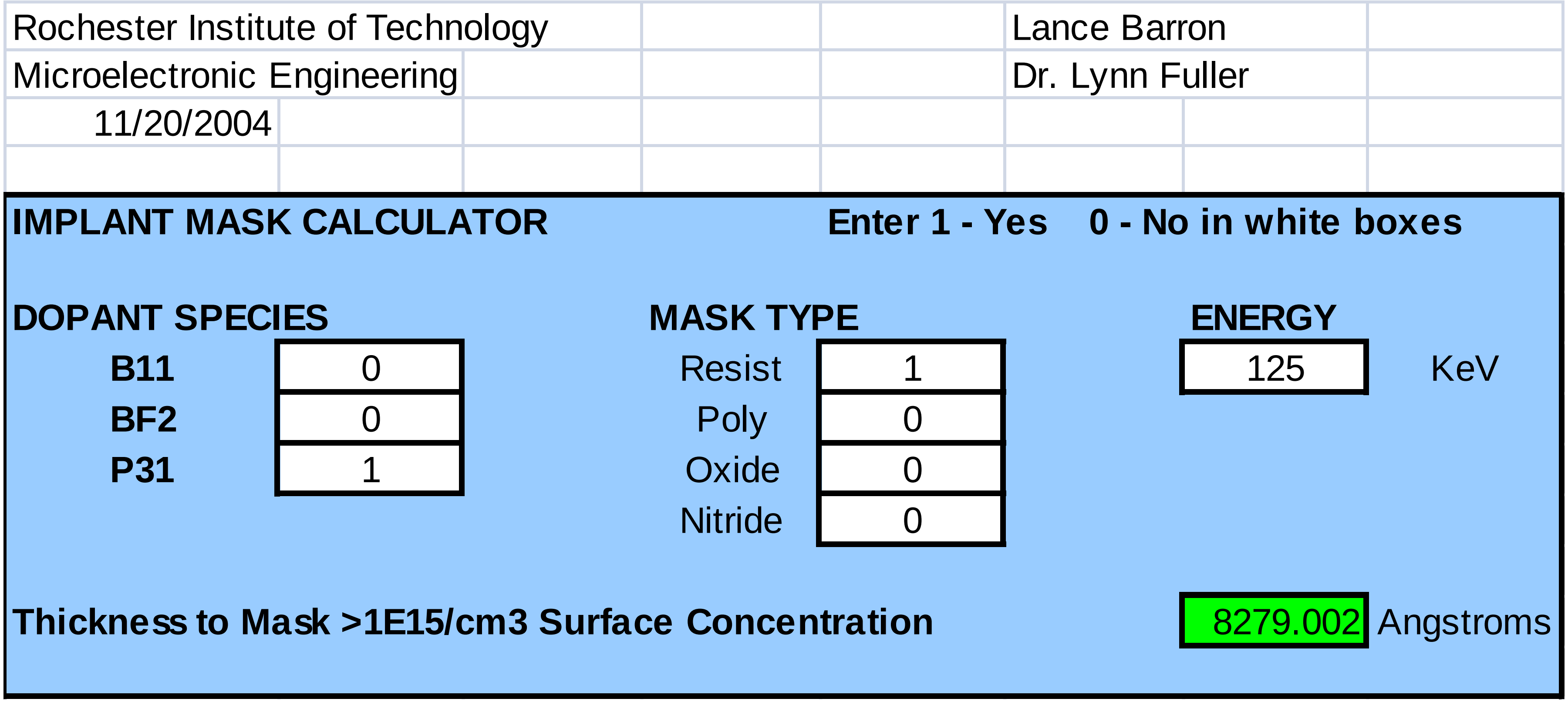
N-WELL IMPLANT



9.5e12, 125keV, P_{31}

P-Type Substrate 10 ohm-cm

IMPLANT MASKING THICKNESS CALCULATOR



Rochester Institute of Technology		Lance Barron
Microelectronic Engineering		Dr. Lynn Fuller
11/20/2004		

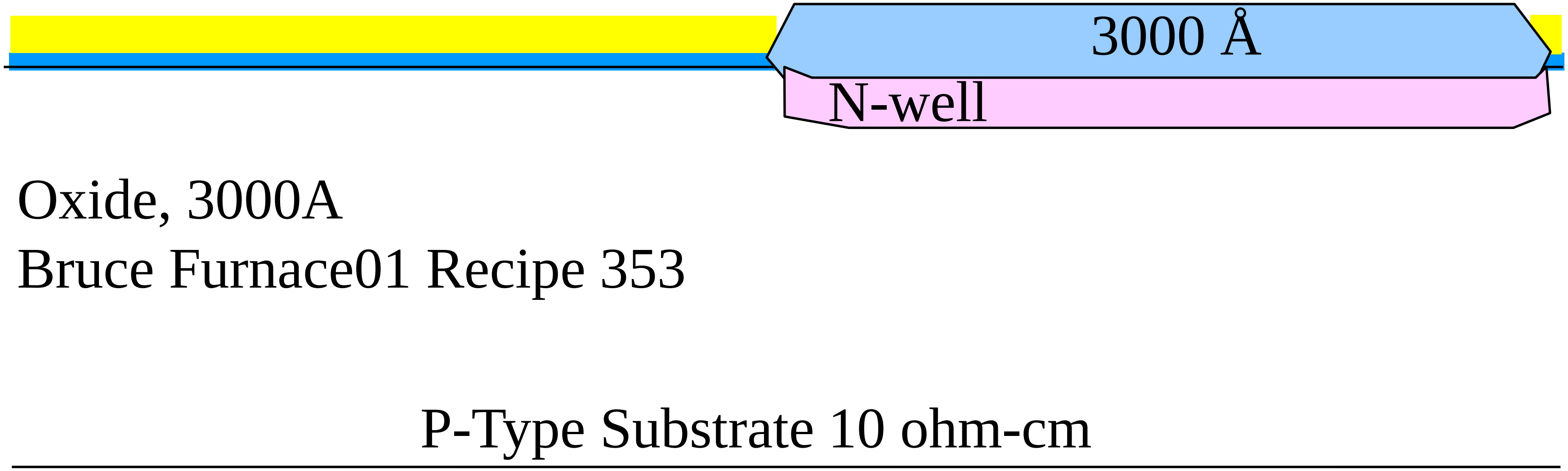
IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		**MASK TYPE**		**ENERGY**	
B11	0	Resist	1	125	KeV
BF2	0	Poly	0		
P31	1	Oxide	0		
		Nitride	0		

Thickness to Mask >1E15/cm3 Surface Concentration 8279.002 Angstroms

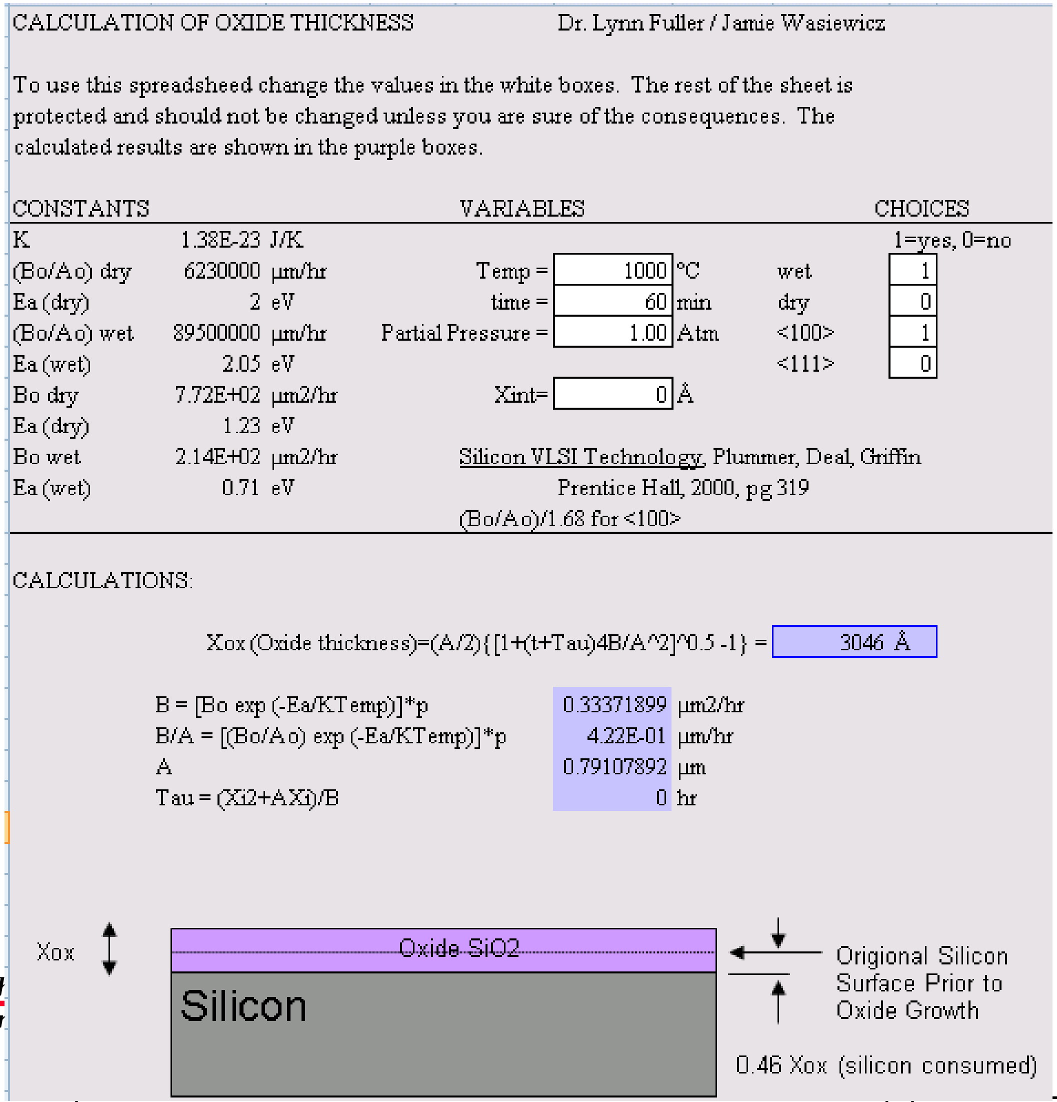
VARIAN 350 D ION IMPLANTER (4” AND 6” WAFERS)

PHOTORESIST ASH, RCA CLEAN AND, N-WELL MASKING OXIDE GROWTH



Oxide, 3000A
Bruce Furnace01 Recipe 353

OXIDE THICKNESS CALCULATOR



CALCULATION OF OXIDE THICKNESS Dr. Lynn Fuller / Jamie Wasiewicz

To use this spreadsheed change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

CONSTANTS			VARIABLES			CHOICES	
K	1.38E-23	J/K					1=yes, 0=no
(Bo/Ao) dry	6230000	µm/hr	Temp =	1000	°C	wet	1
Ea (dry)	2	eV	time =	60	min	dry	0
(Bo/Ao) wet	89500000	µm/hr	Partial Pressure =	1.00	Atm	<100>	1
Ea (wet)	2.05	eV				<111>	0
Bo dry	7.72E+02	µm2/hr	Xint=	0	Å		
Ea (dry)	1.23	eV					
Bo wet	2.14E+02	µm2/hr					
Ea (wet)	0.71	eV					

Silicon VLSI Technology, Plummer, Deal, Griffin
Prentice Hall, 2000, pg 319
(Bo/Ao)/1.68 for <100>

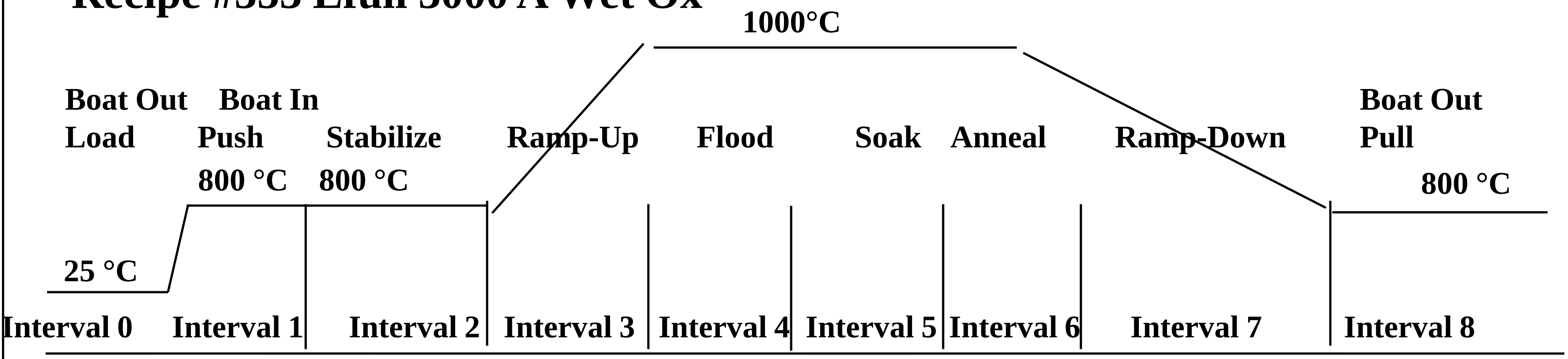
CALCULATIONS:

Xox (Oxide thickness)=(A/2){[1+(t+Tau)4B/A^2]^0.5 -1} = 3046 Å

B = [Bo exp (-Ea/KTemp)]*p	0.33371899	µm2/hr
B/A = [(Bo/Ao) exp (-Ea/KTemp)]*p	4.22E-01	µm/hr
A	0.79107892	µm
Tau = (Xi2+AXi)/B	0	hr

BRUCE FURNACE RECIPE 330

Recipe #353 Lfull 3000 A Wet Ox



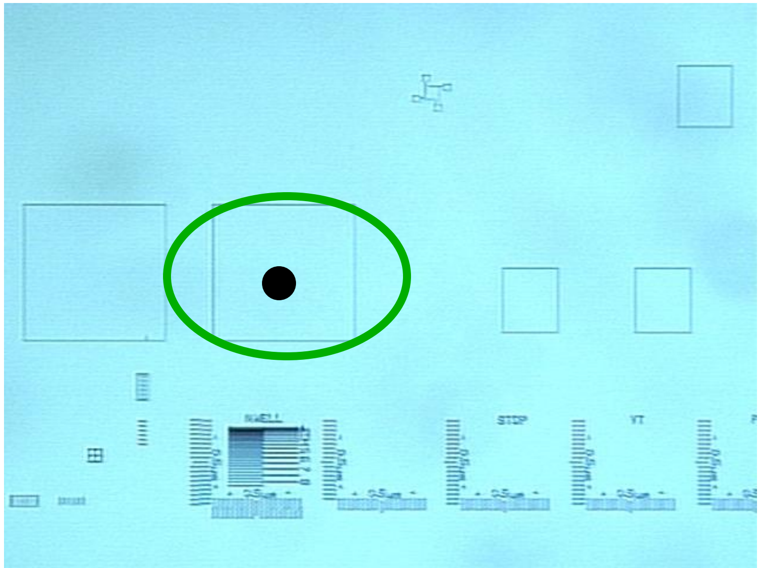
Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7	Interval 8
Any	12 min	15 min	20 min	5 min	50 min	5 min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	5 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	N2	O2	O2/H2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

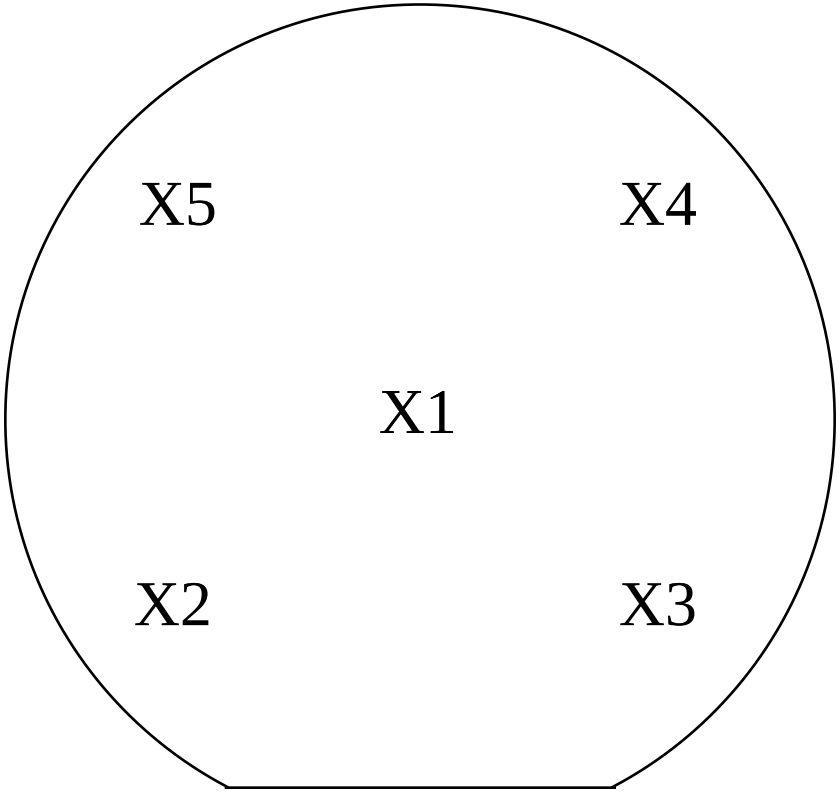
Wet Oxide Growth, Target 3000 Å

MEASURE OXIDE THICKNESS

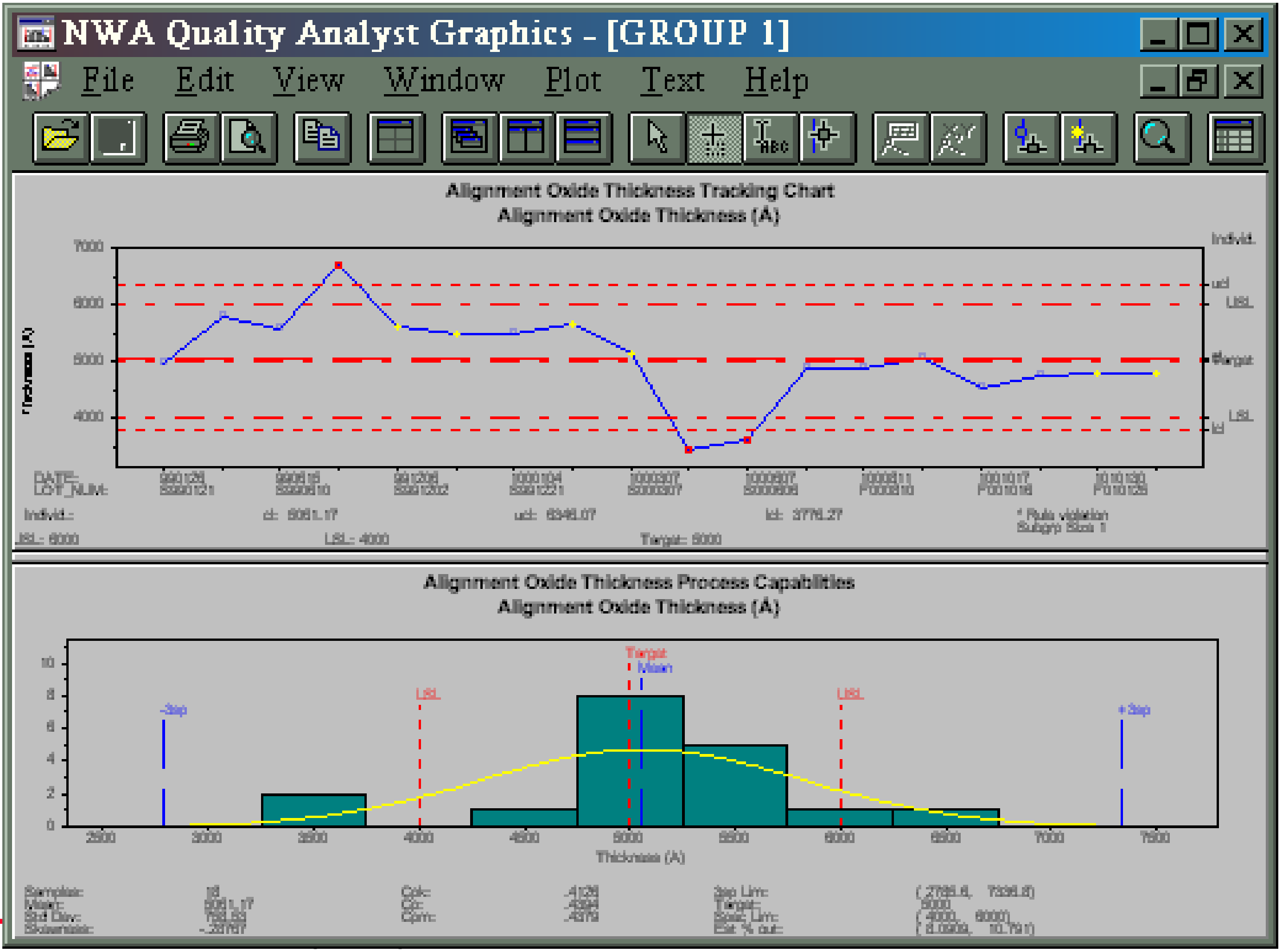
Record:
Color =
Color Chart Thickness = Å
Nanospec Thickness = Å



FACTORY THICKNESS MEASUREMENT LOCATIONS



SPC CHARTS



Individ.: cl: 5061.17 ucl: 6346.07 lcl: 3776.27

USL: 6000 LSL: 4000 Target: 5000

* Rule violation
Subgrp Size 1

Samples: 18
Mean: 5061.17
Std Dev: 758.53
Skewness: -.23787

Cpk: .4126
Cp: .4394
Cpm: .4379

3sp Lim: (2785.6, 7336.8)
Target: 5000
Spec Lim: (4000, 6000)
Est % out: (8.0909, 10.7911)

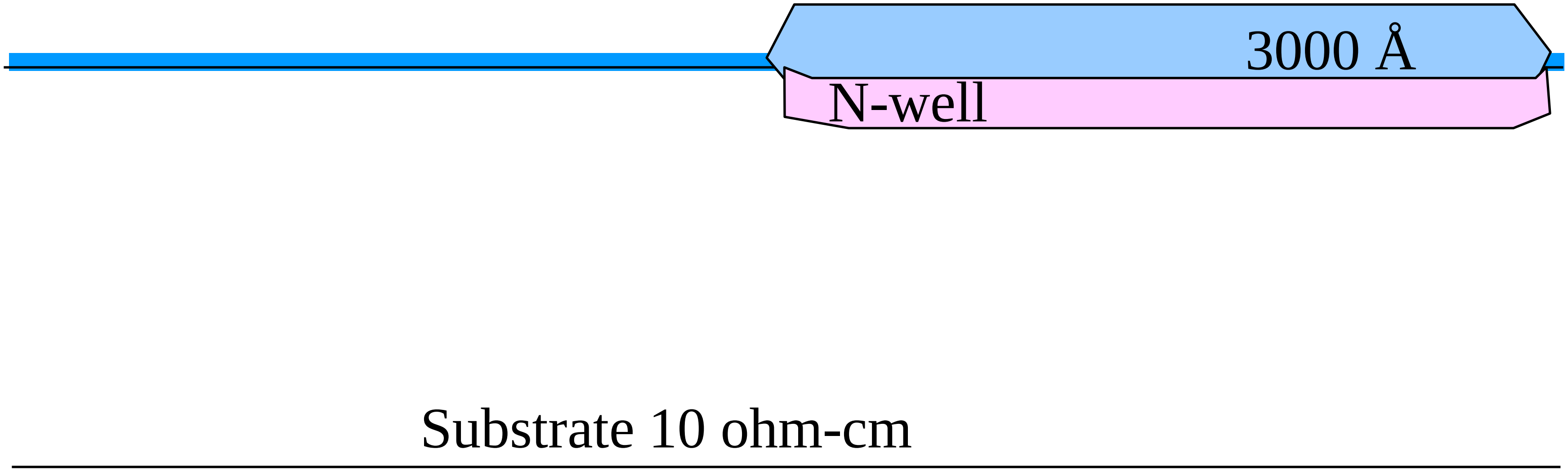
MEGASONIC RCA CLEAN, SRD & ASHER

RCA Clean Bench

Branson Asher

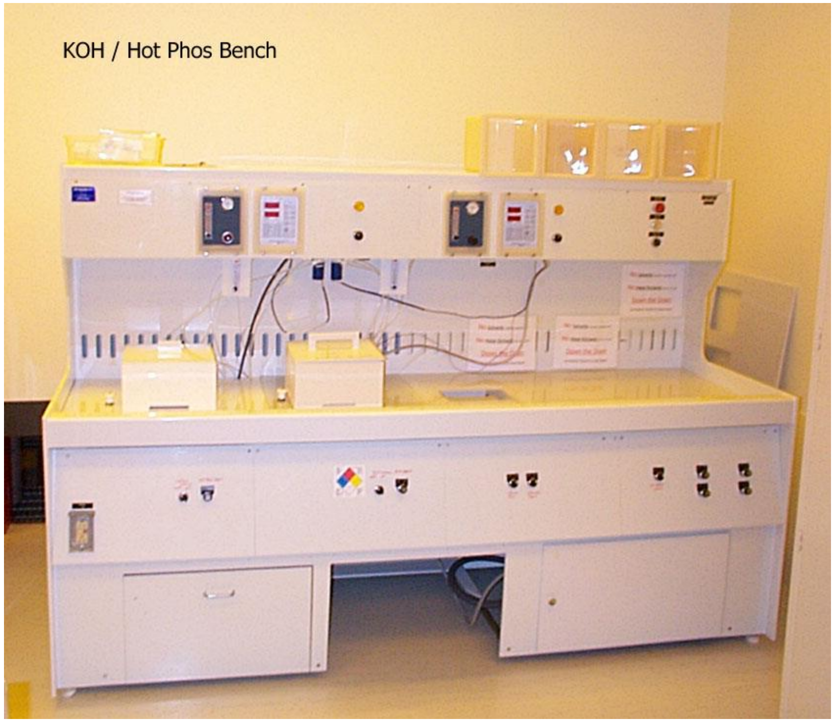
WET ETCH NITRIDE

Hot Phosphoric Acid
Wet Nitride Etch.
Etch Rate ~50 Å/min
Etch 45 min.



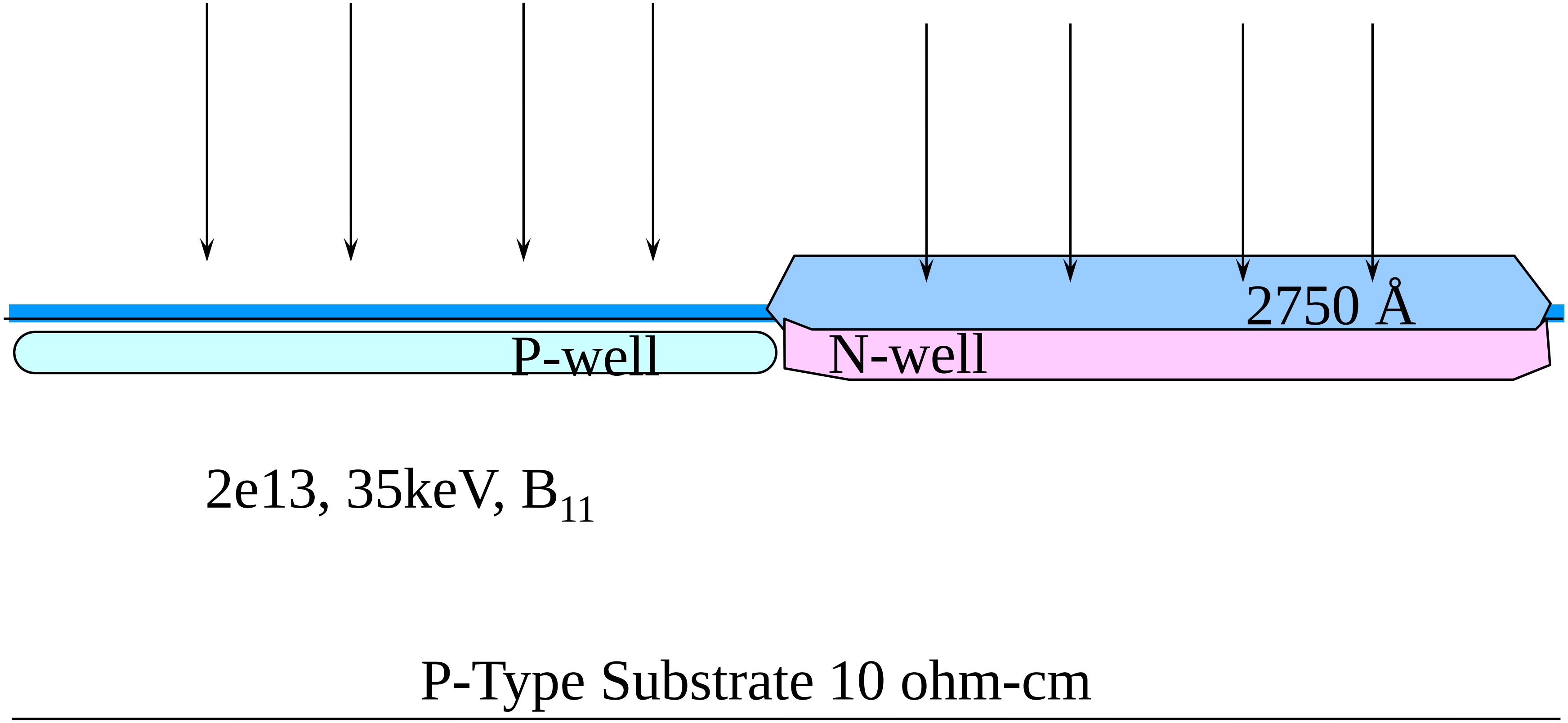
HOT PHOSPHORIC ACID ETCH BENCH

Include all Device Wafers
Warm up Hot Phosphoric Acid pot to ~165º C
Etch Oxynitride in BOE if appropriate
    10:1 BOE for ~30sec. Rinse in DI, 5 min
Rinse, SRD
Use Teflon boat to place wafers in acid bath
"U" shape handle allows cover to close tightly
    3500Å +/-500 → 90 minutes
    1500Å +/- 500 → 45minutes
    Etch rate of ~80 Å/min
Rinse for 5 minutes in Cascade Rinse
Spin/Rins/Dry (SRD) wafers



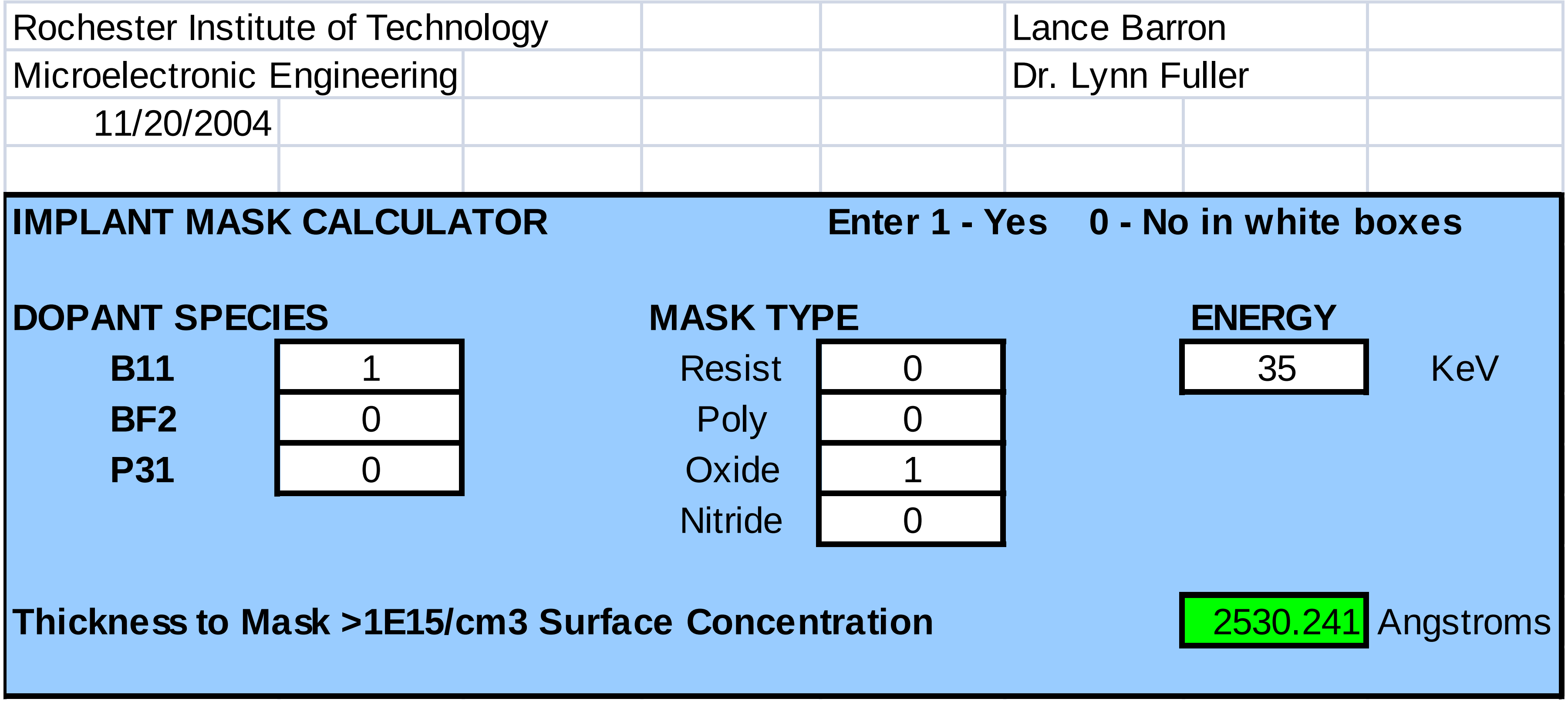
Sub-CMOS Process

IMPLANT P-WELL



2e13, 35keV, B_{11}

IMPLANT MASKING THICKNESS CALCULATOR



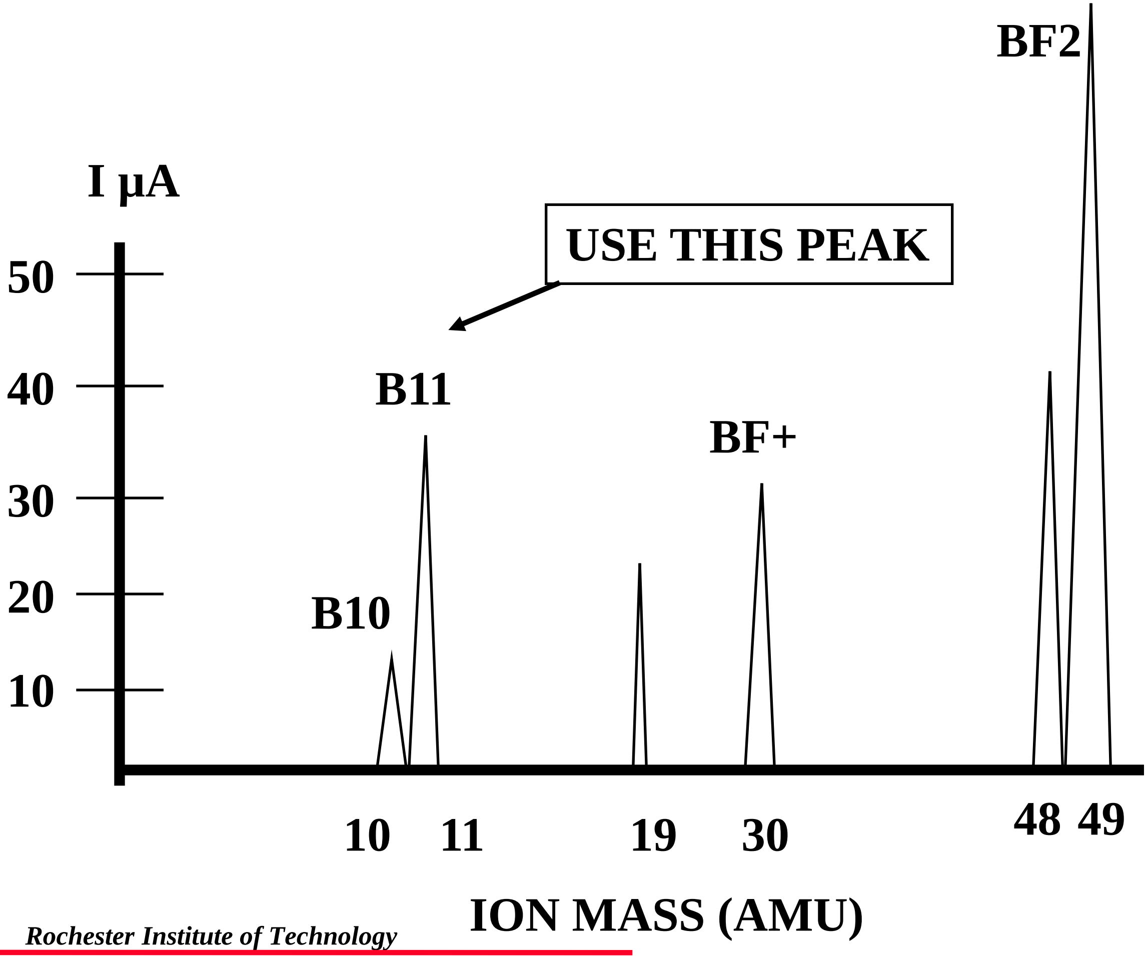
Rochester Institute of Technology	Lance Barron
Microelectronic Engineering	Dr. Lynn Fuller
11/20/2004	

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

DOPANT SPECIES		MASK TYPE		ENERGY	
B11	1	Resist	0	35	KeV
BF2	0	Poly	0		
P31	0	Oxide	1		
		Nitride	0		

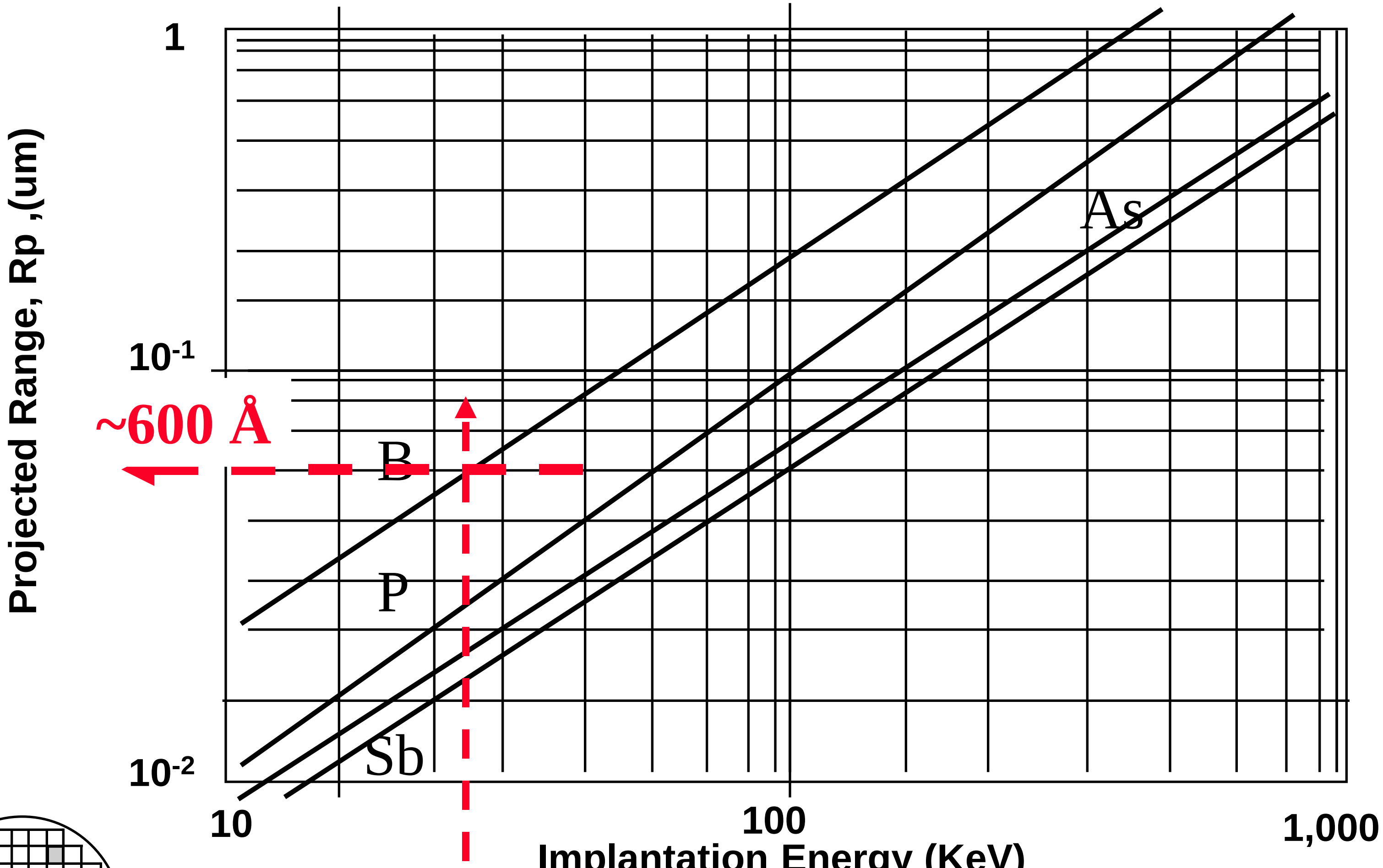
Thickness to Mask >1E15/cm3 Surface Concentration 2530.241 Angstroms

B_{11} IMPLANT FOR BORON THRESHOLD ADJUSTS, STOP, P-WELL



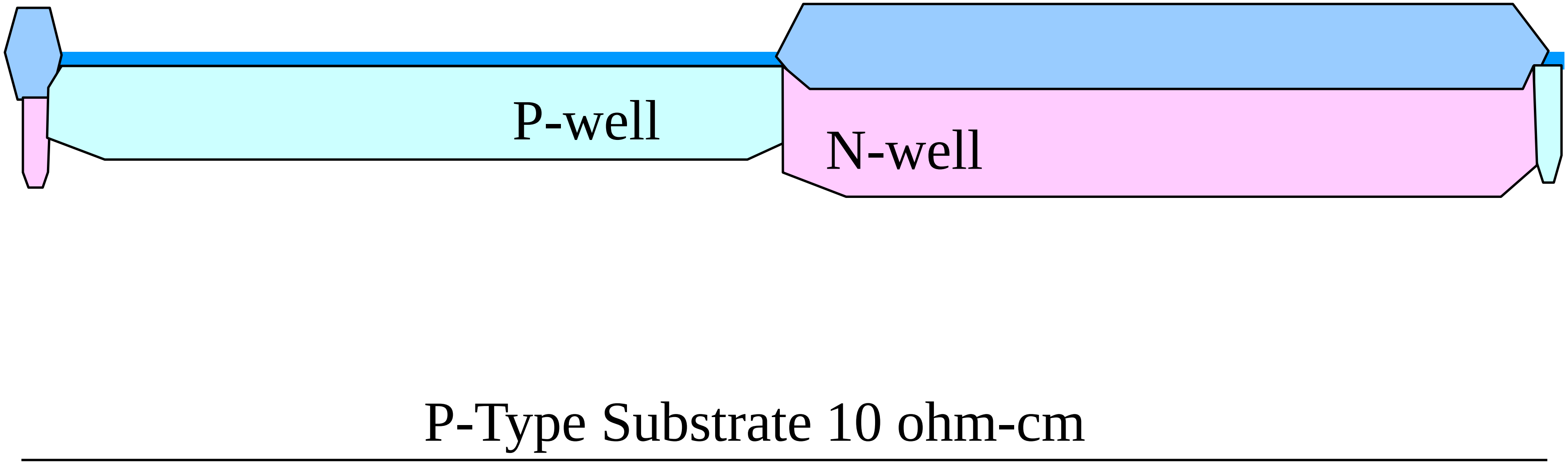
PLAY

ION IMPLANT RANGE CHART



WELL DRIVE

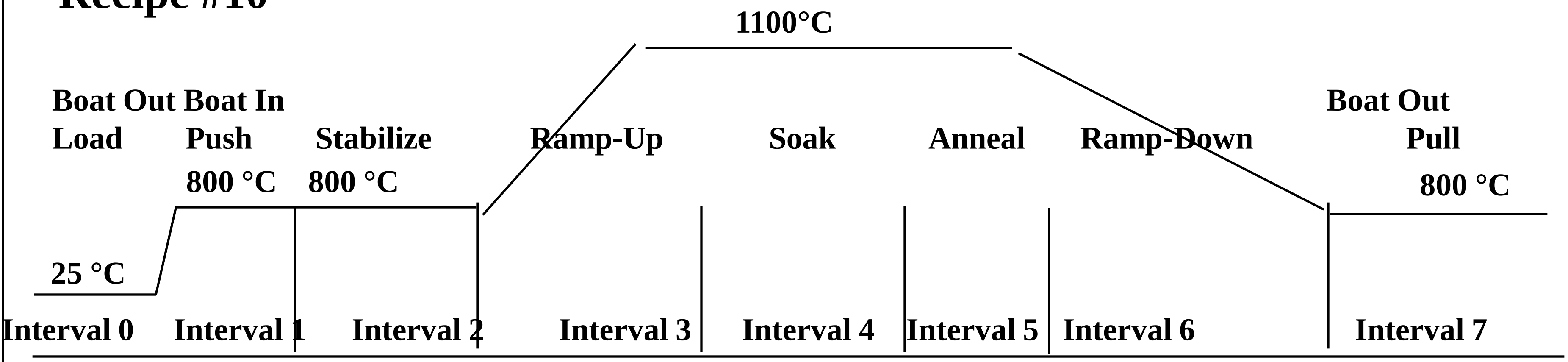
1100 C, 10 Hours, N2



BRUCE FURNACE RECIPE 10 SUB-CMOS WELL DRIVE

Verified:12-8-04

Recipe #10

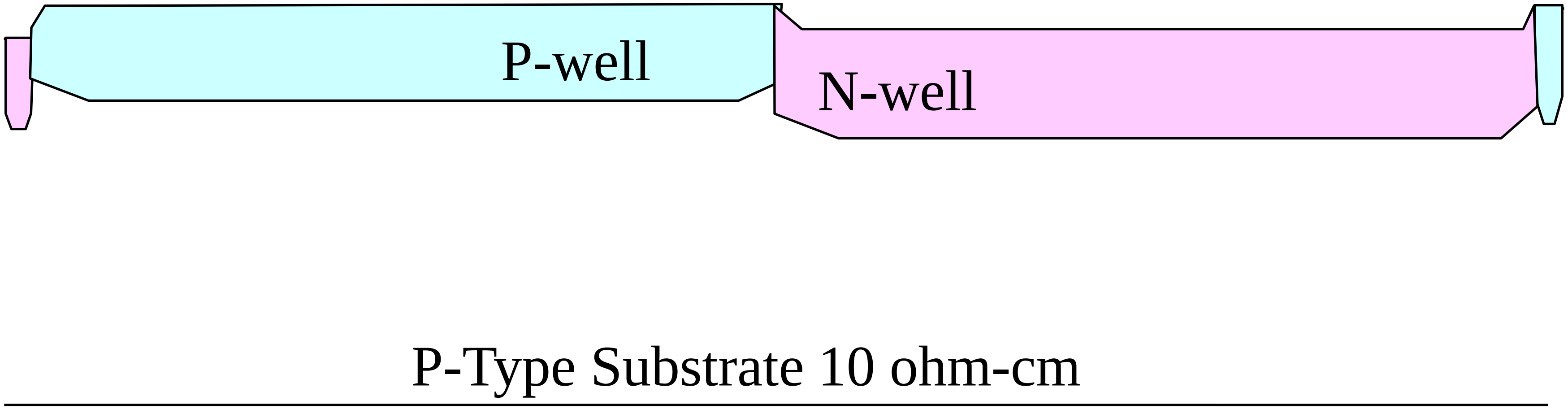


Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Boat Out Load	Boat In Push	Stabilize	Ramp-Up	Soak	Anneal	Ramp-Down	Boat Out Pull
25 °C	800 °C	800 °C		1100°C			800 °C
Any	12 min	15 min	30 min	600 min	5 min	60 min	12 min
0 lpm	10 lmp	10 lpm	10 lpm	10 lpm	10 lpm	10 lpm	5 lpm
none	N2	N2	N2	N2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

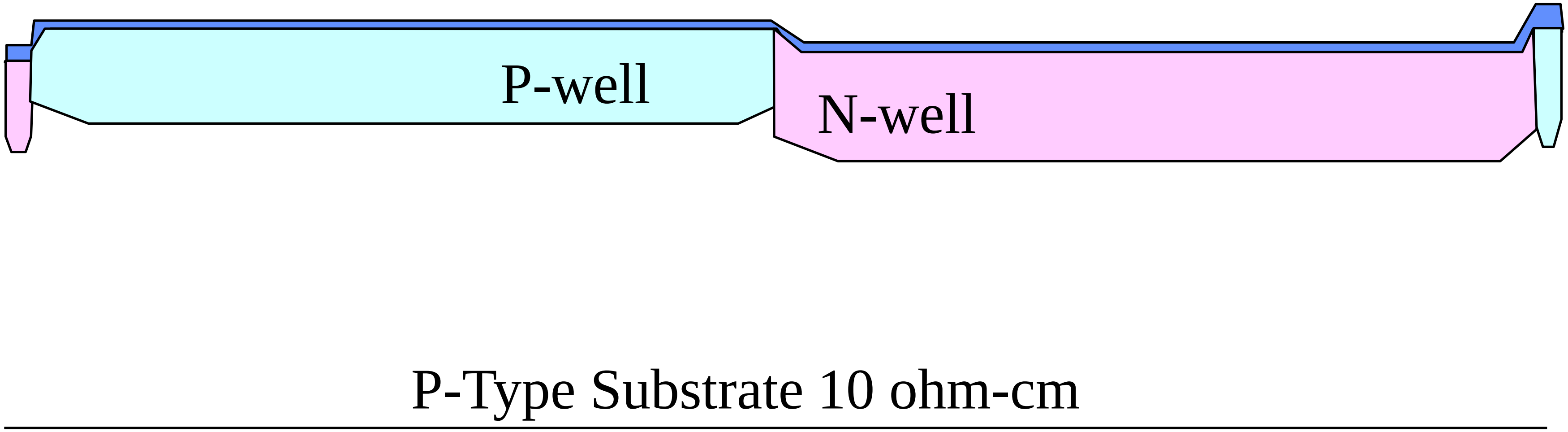
Sub-CMOS Well Drive, No Oxide Growth, Tube 1

ETCH ALL OXIDE



GROW PAD OXIDE

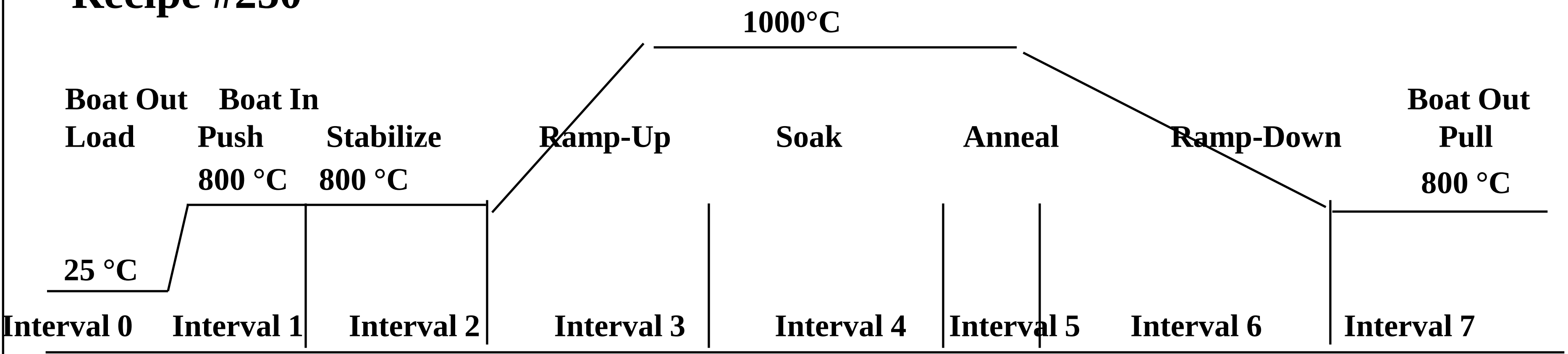
Pad Oxide, 500A
Bruce Furnace 01 Recipe 250



P-Type Substrate 10 ohm-cm

BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

Recipe #250



Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Any	12 min	15 min	20 min	40min	5min	40 min	12 min
0 lpm	10 lpm	10 lpm	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

DEPOSIT NITRIDE

Nitride, 1500A
LPCVD, 810C, 25min

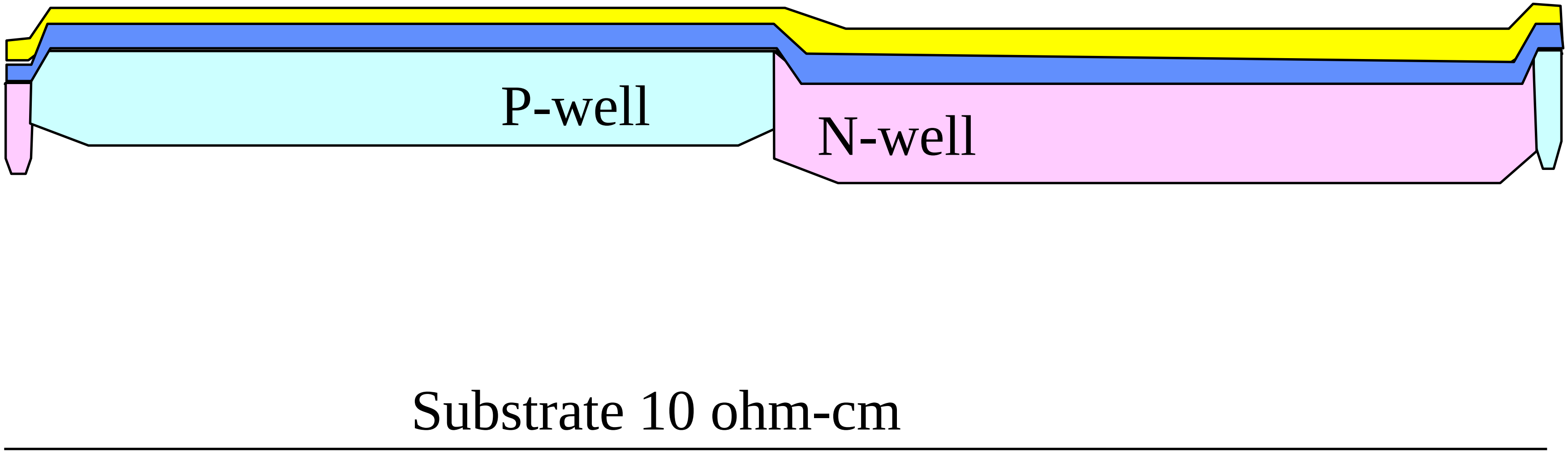
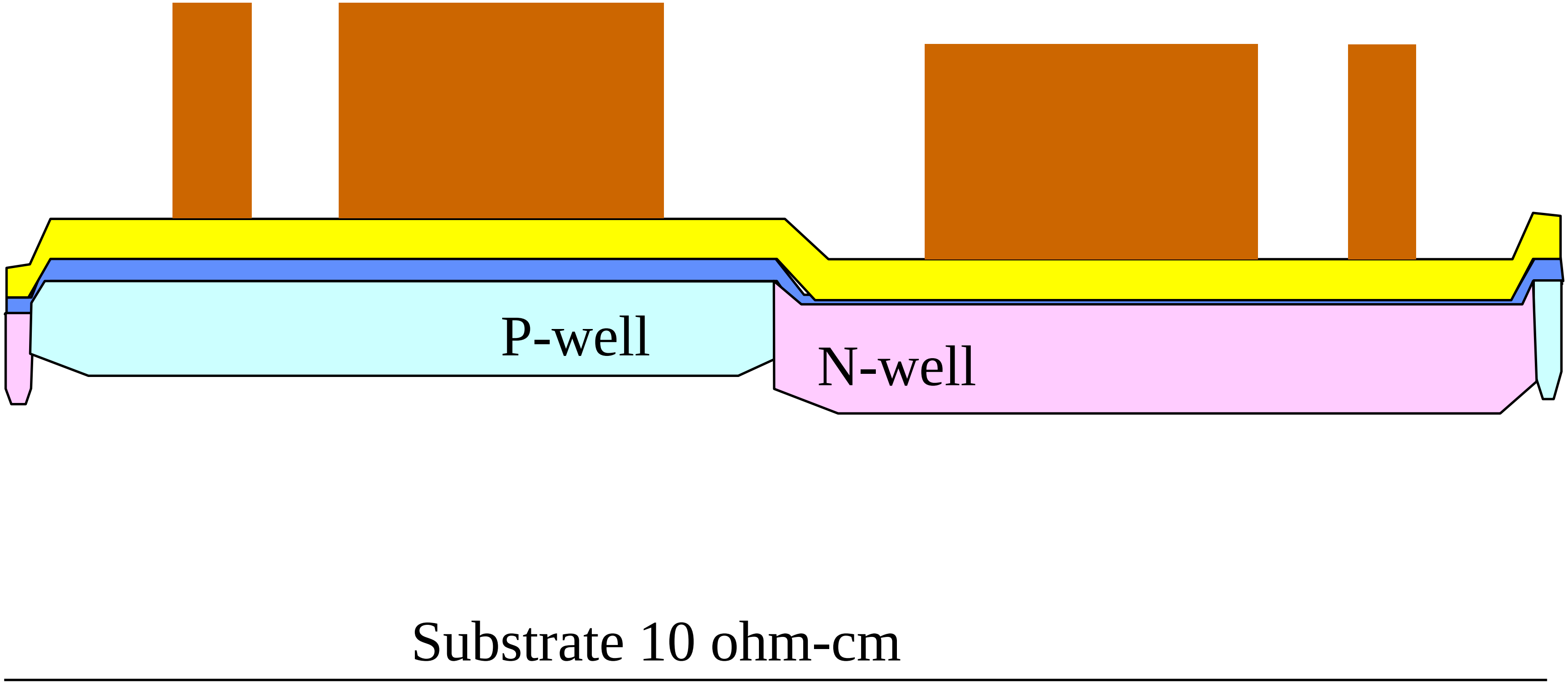
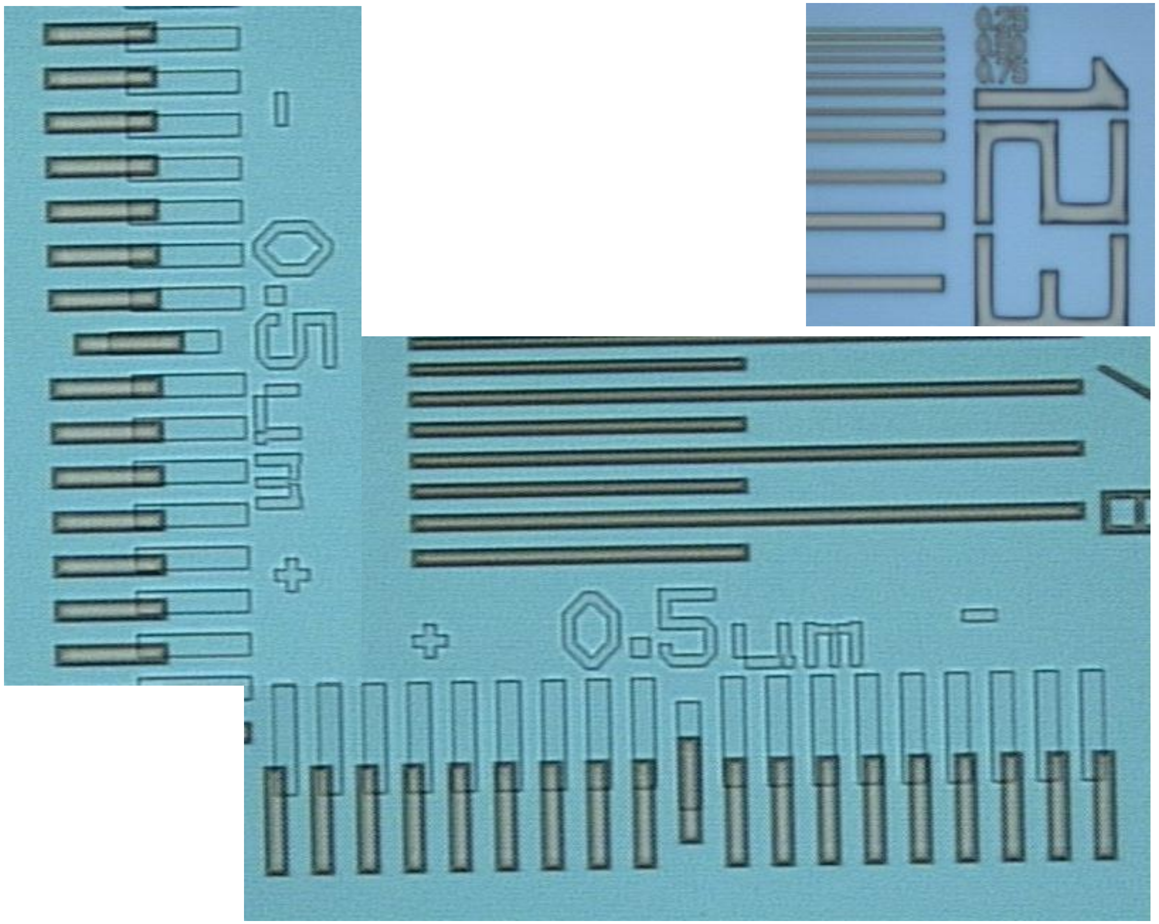


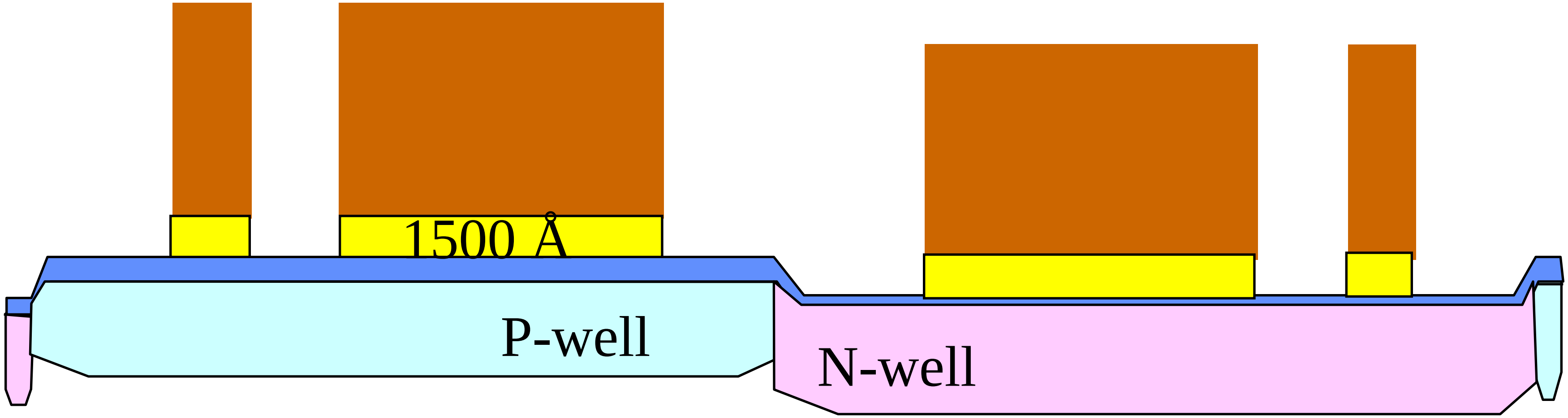
PHOTO 2 ACTIVE



RIT 0.5 µm OVERLAY VERNIERS



ETCH NITRIDE



Nitride Etch: SF_6 plasma

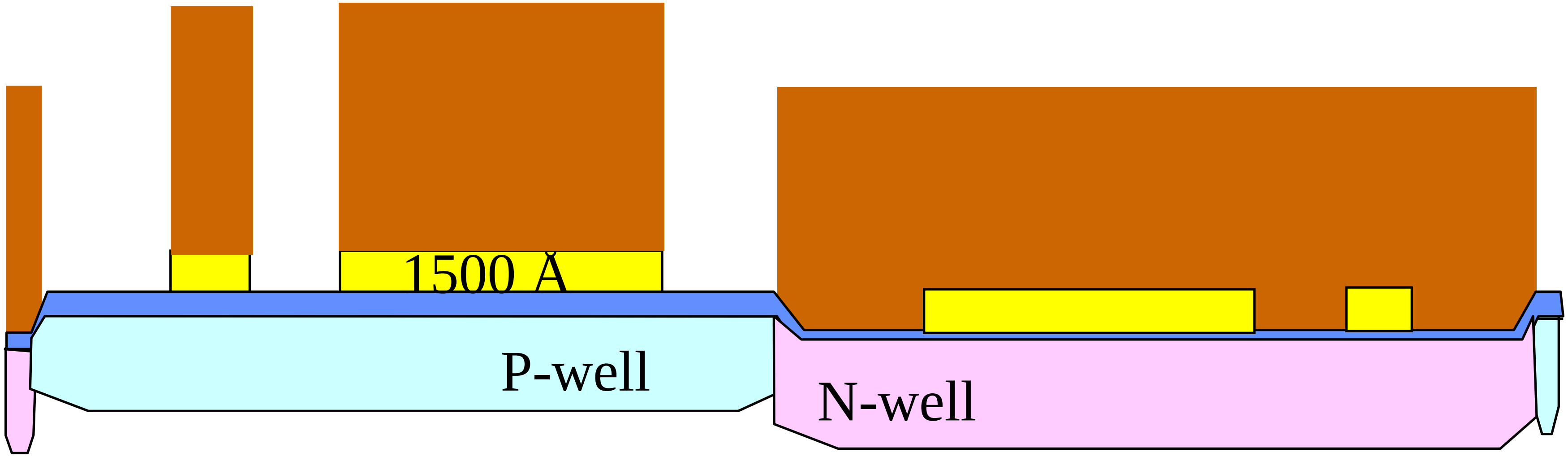
LAM 490 Etcher, Etch Rate ~1000 Å/min

LAM 490 END POINT

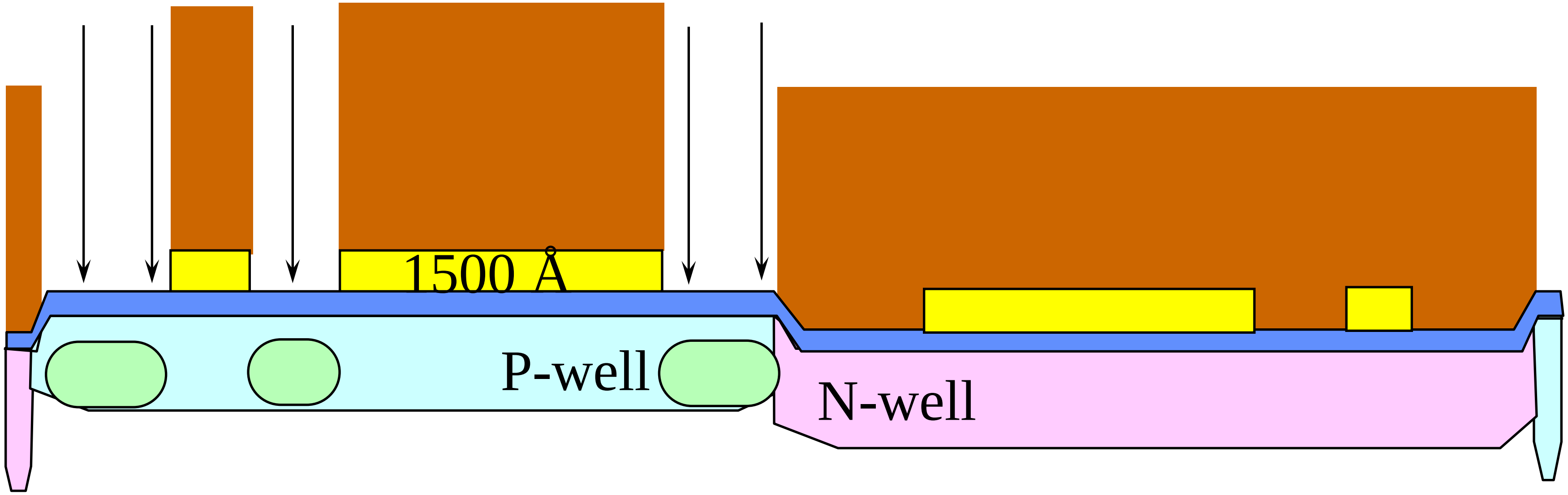
Process: Step 1 – 260mTorr; 0W,
200sccm SF6,
Max Time = 2 min, Time Only
Process: Step 2 – 260mTorr; 125W,
200sccm SF6,
Max Time = 2min 30sec, Endpoint & Time
Process: Step 3 – 260mTorr; 125W,
200sccm SF6,
Over etch – 40%

Endpoint Parameters – Sampling A (ch12 @ 520nm)
Active during step 02
Delay 50sec before normalizing
Normalize for 10sec
Trigger at 85%

PHOTO 3 CHANNEL STOP



CHANNEL STOP IMPLANT

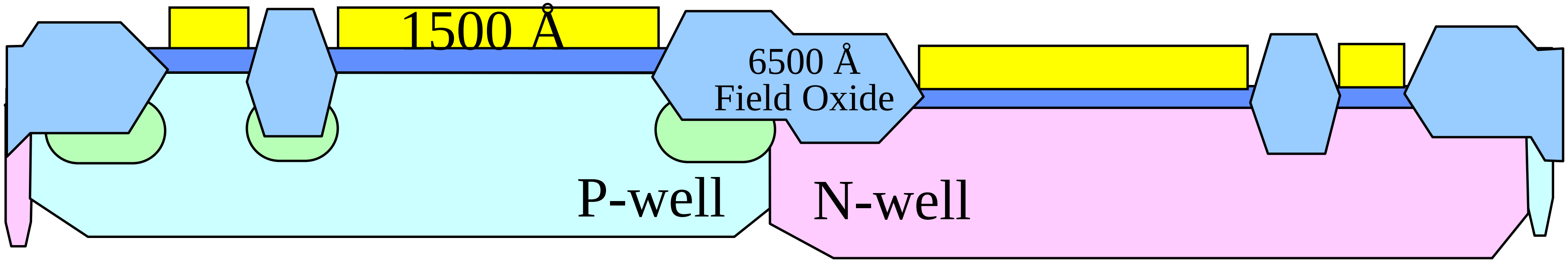


B11

Dose = 8E13

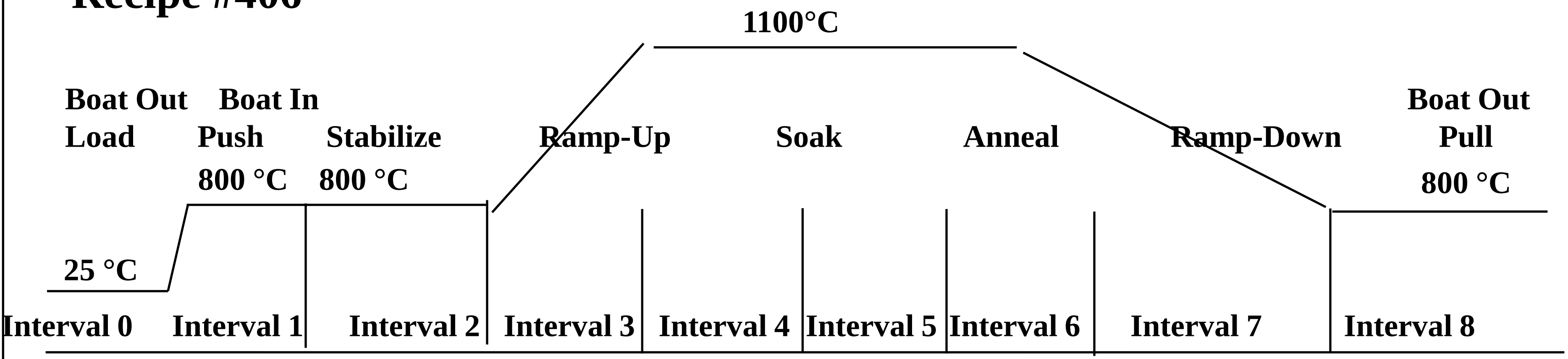
100 KeV

RESIST STRIP, CLEAN, GROW FIELD OXIDE



BRUCE FURNACE RECIPE 406 – WET OXIDE 6,500Å

Recipe #406

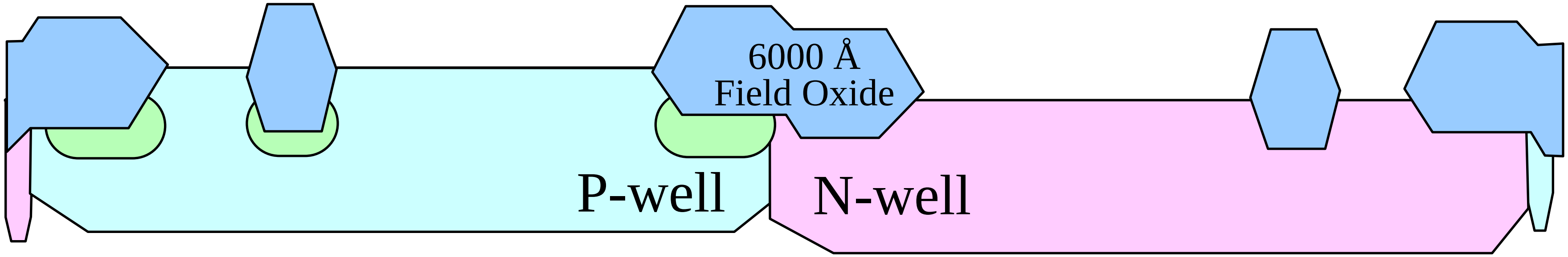


Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7	Interval 8
Any	12 min	15 min	30 min	5 min	65 min	5 min	55 min	15 min
0 lpm	10 lpm	10 lpm	5 lpm	5 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	N2	O2	O2/H2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

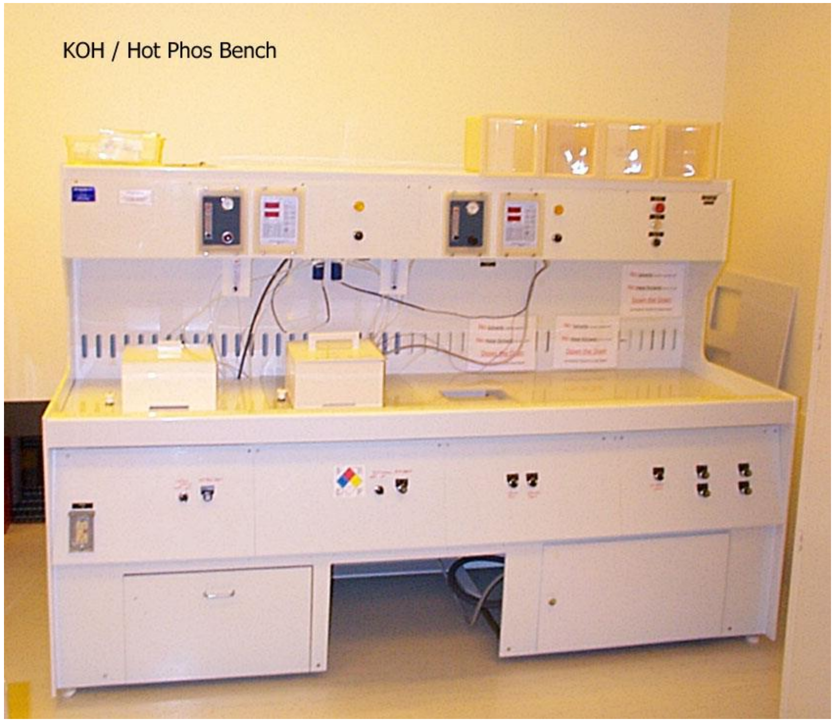
Wet Oxide Growth, Target 6,500 Å

ETCH NITRIDE AND PAD OXIDE



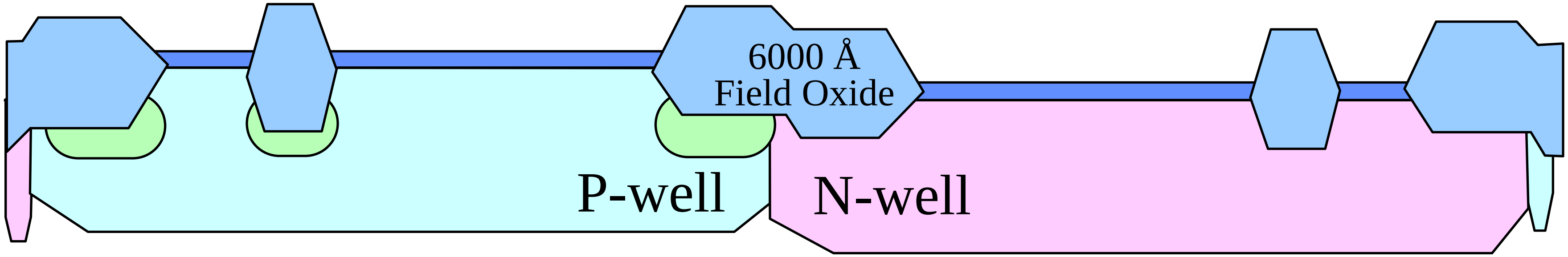
HOT PHOSPHORIC ACID ETCH BENCH

Include all Device Wafers
Warm up Hot Phosphoric Acid pot to ~165° C
Etch Oxynitride in BOE if appropriate
    10:1 BOE for ~1 min. Rinse in DI, 5 min
Rinse, SRD
Use Teflon boat to place wafers in acid bath
“U” shape handle allows cover to close tightly
    3500Å +/-500 → 90 minutes
    1500Å +/- 500 → 45minutes
    Etch rate of ~80 Å/min
Rinse for 5 minutes in Cascade Rinse
Spin/Rins/Dry (SRD) wafers

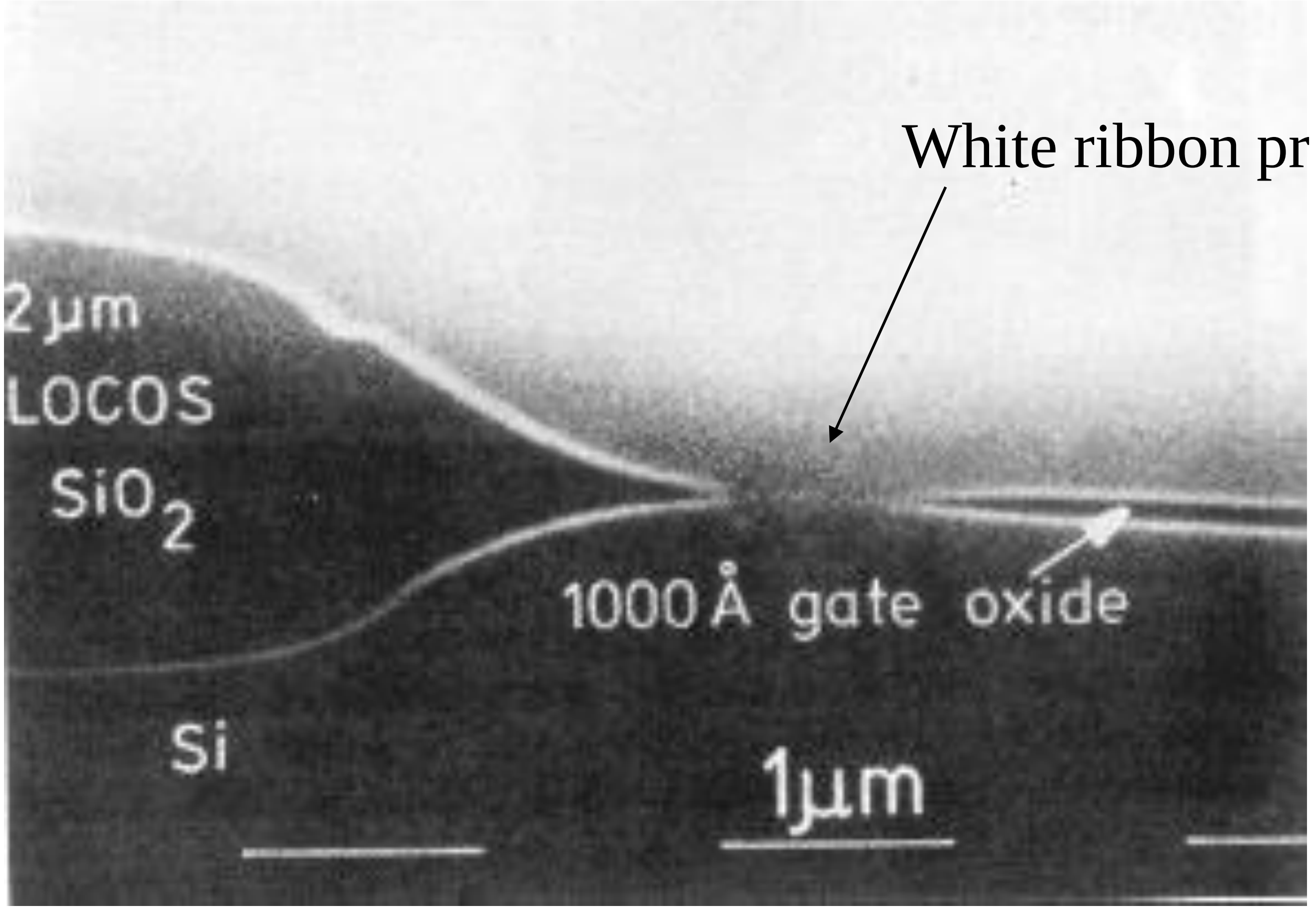


GROW SACRIFICIAL OXIDE (KOOI OXIDE)

1000 Å Oxide, 900°C, Wet O_2
Bruce Furnace01 Recipe 311:



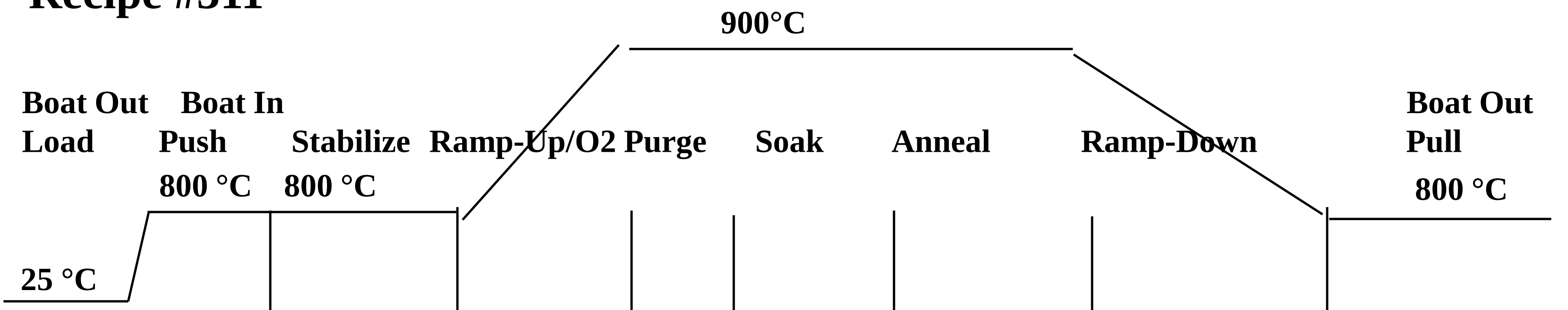
KOOI (SACRIFICIAL) OXIDE



White ribbon problem

BRUCE FURNACE RECIPE 311 – WET OXIDE 1,000Å

Recipe #311

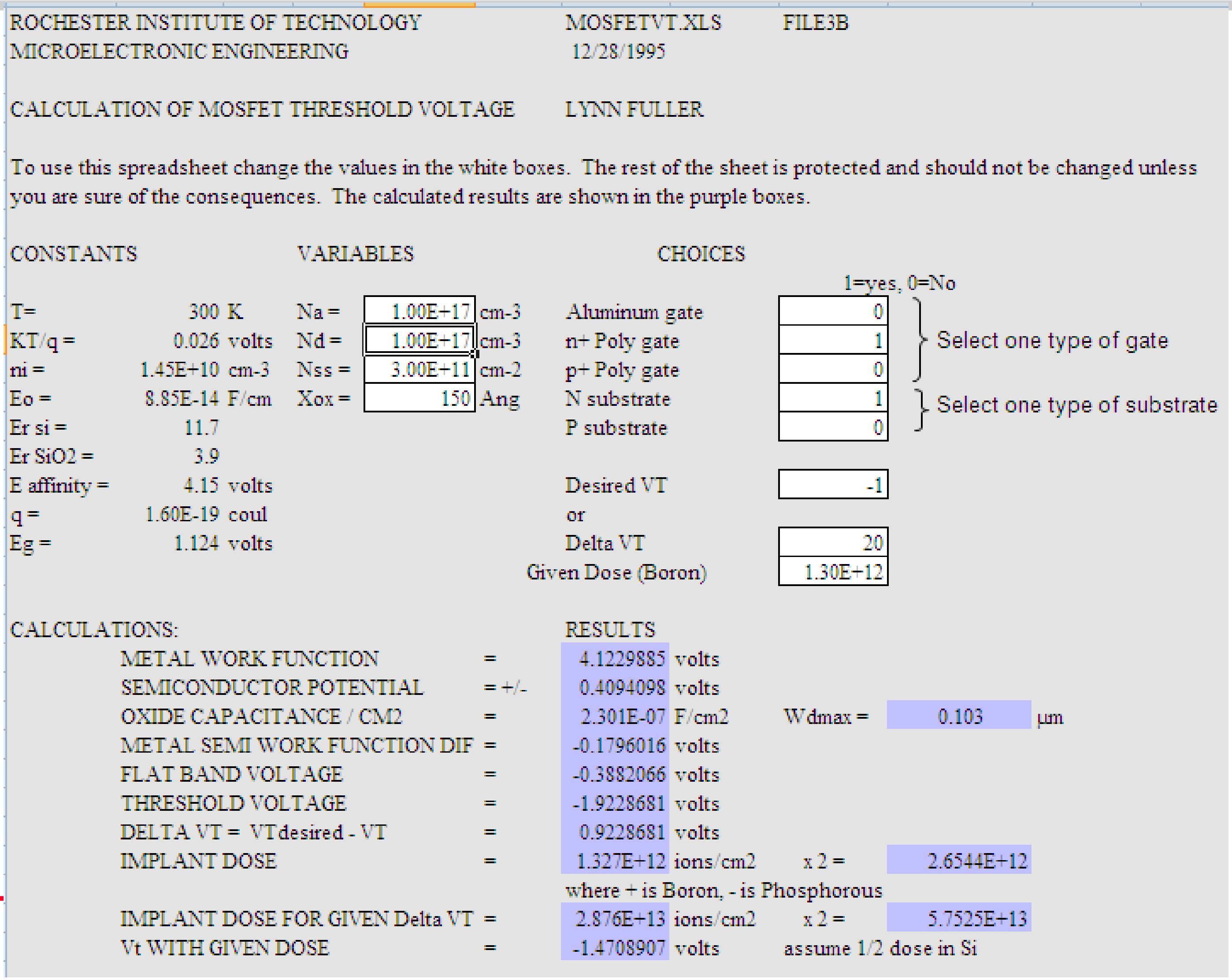


Interval 0	Interval 1	Interval 2	Interval 3	4	Interval 5	Interval 6	Interval 7	Interval 8
Any	12 min	15 min	10 min	5 min	40 min	5 min	15 min	15 min
0 lpm	15 lpm	15 lmp	10 lpm	10 lpm	10 lpm	15 lpm	10 lpm	15 lpm
none	N2	N2	O2	O2	O2/H2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Wet Oxide Growth, Target 1000 Å, Kooi

THRESHOLD VOLTAGE ADJUST IMPLANT DOSE



ROCHESTER INSTITUTE OF TECHNOLOGY MOSFETVT.XLS FILE3B
MICROELECTRONIC ENGINEERING 12/28/1995

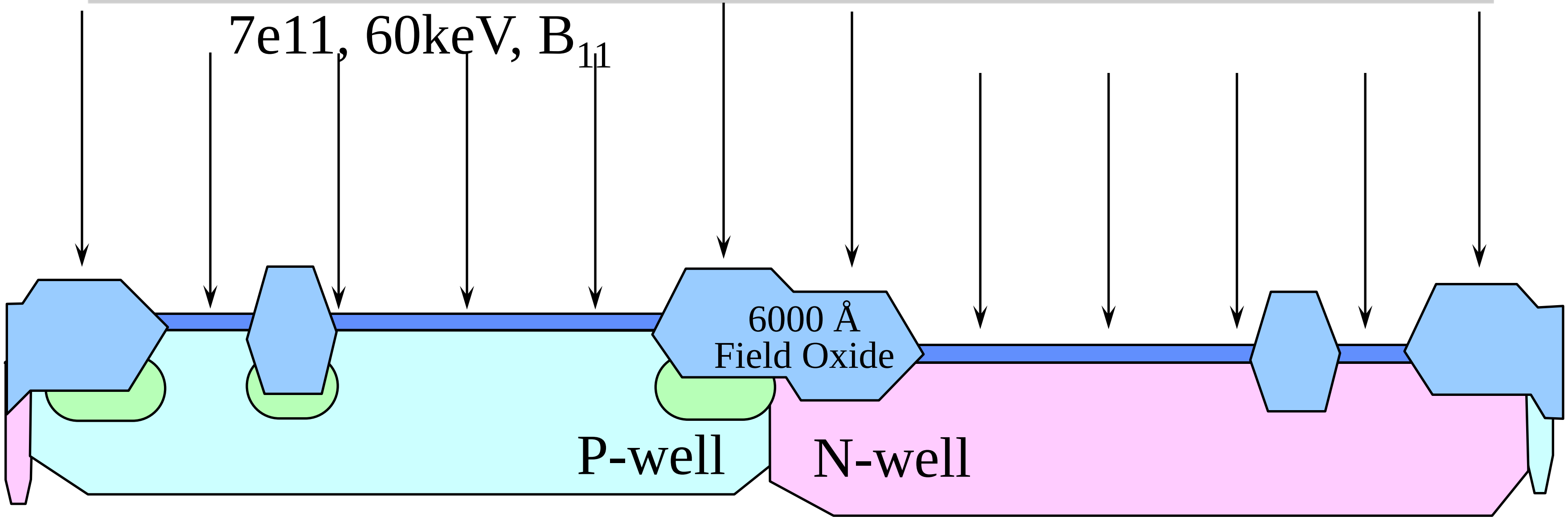
CALCULATION OF MOSFET THRESHOLD VOLTAGE LYNN FULLER

To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

CONSTANTS			VARIABLES			CHOICES		
							1=yes, 0=No	
T=	300	K	Na =	1.00E+17	cm-3	Aluminum gate	0	Select one type of gate
KT/q =	0.026	volts	Nd =	1.00E+17	cm-3	n+ Poly gate	1	
ni =	1.45E+10	cm-3	Nss =	3.00E+11	cm-2	p+ Poly gate	0	
Eo =	8.85E-14	F/cm	Xox =	150	Ang	N substrate	1	Select one type of substrate
Er si =	11.7					P substrate	0	
Er SiO2 =	3.9							
E affinity =	4.15	volts				Desired VT	-1	
q =	1.60E-19	coul				or		
Eg =	1.124	volts				Delta VT	20	
						Given Dose (Boron)	1.30E+12	

CALCULATIONS:		RESULTS				
METAL WORK FUNCTION	=	4.1229885	volts			
SEMICONDUCTOR POTENTIAL	=+/-	0.4094098	volts			
OXIDE CAPACITANCE / CM2	=	2.301E-07	F/cm2	Wdmax =	0.103	µm
METAL SEMI WORK FUNCTION DIF	=	-0.1796016	volts			
FLAT BAND VOLTAGE	=	-0.3882066	volts			
THRESHOLD VOLTAGE	=	-1.9228681	volts			
DELTA VT = VTdesired - VT	=	0.9228681	volts			
IMPLANT DOSE	=	1.327E+12	ions/cm2	x 2 =	2.6544E+12	
		where + is Boron, - is Phosphorous				
IMPLANT DOSE FOR GIVEN Delta VT	=	2.876E+13	ions/cm2	x 2 =	5.7525E+13	
Vt WITH GIVEN DOSE	=	-1.4708907	volts	assume 1/2 dose in Si		

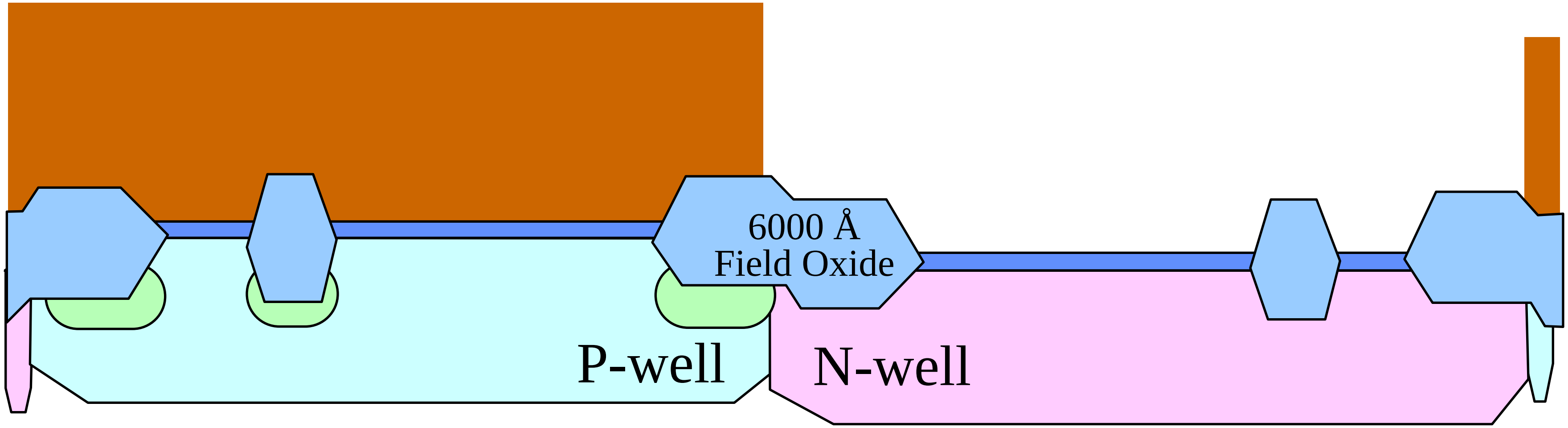
BLANKET PMOS & NMOS VT ADJUST IMPLANT



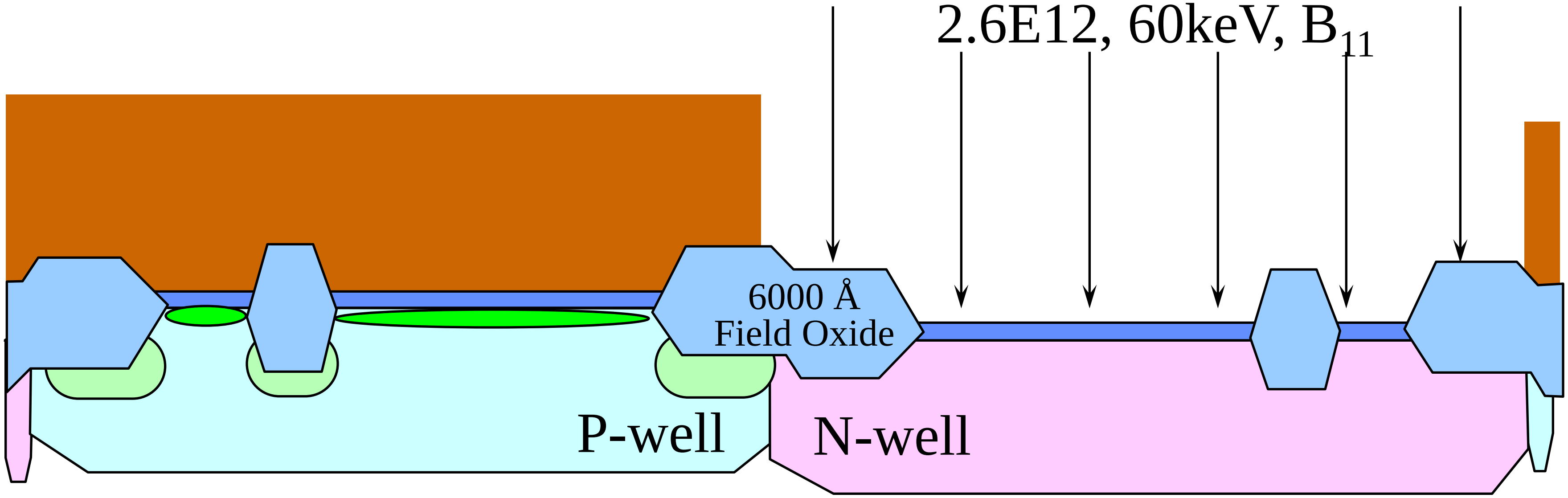
7e11, 60keV, B_{11}

Rochester Institute of Technology
Microelectronic Engineering

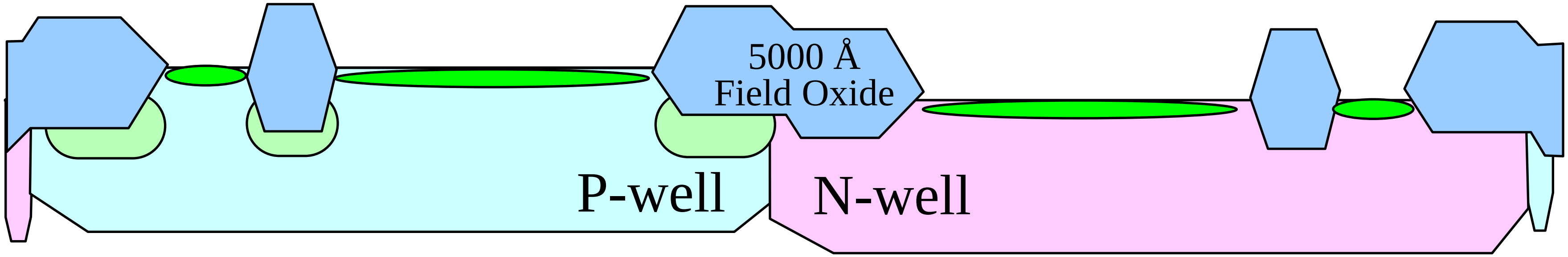
PHOTO 4 PMOS VT



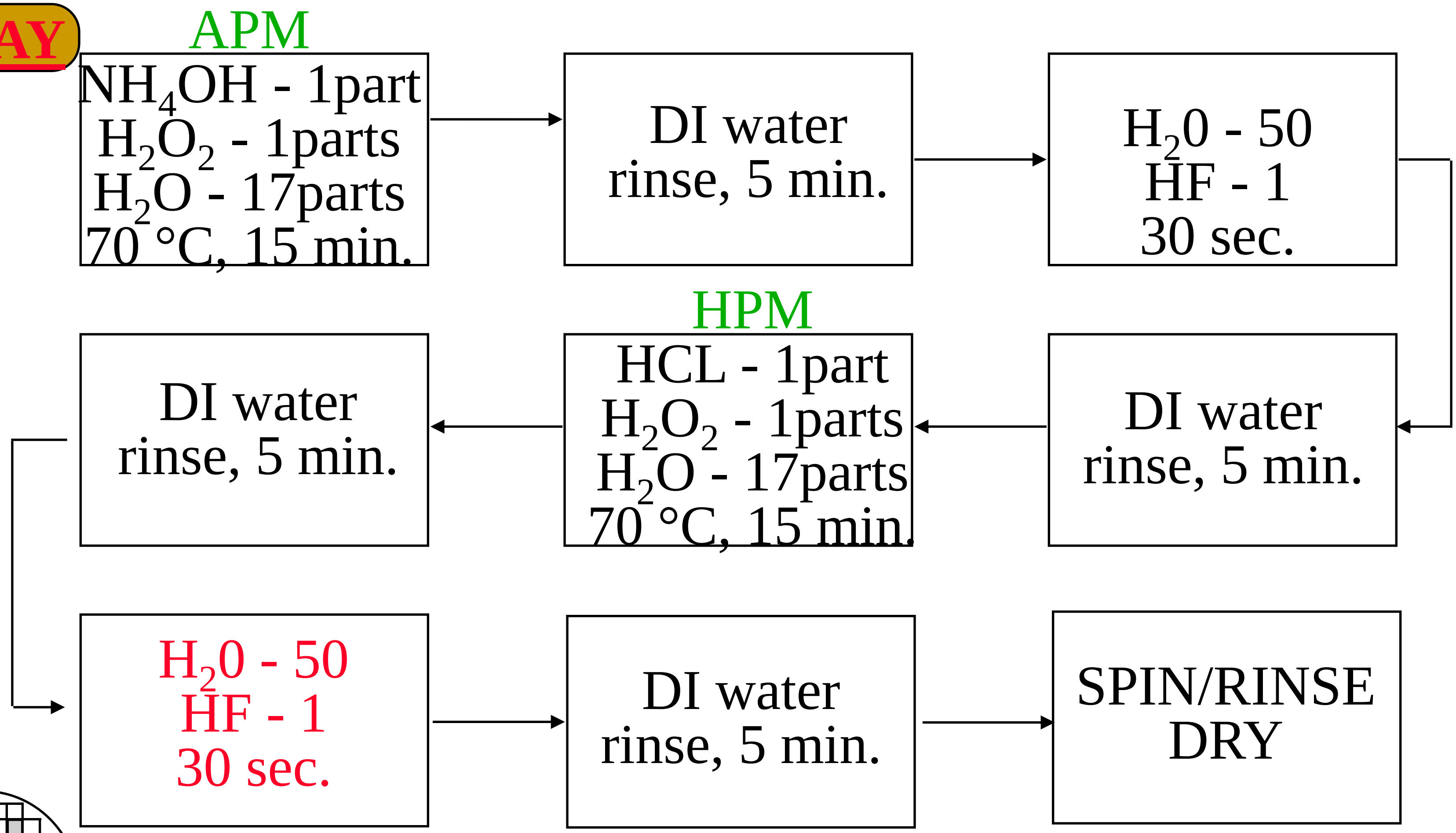
PMOS VT IMPLANT



ASH RESIST, ETCH KOOI OXIDE, RCA CLEAN



SPECIAL RCA CLEAN (TWO 50:1 HF STEPS)



PLAY

APM

NH_4OH - 1part
H_2O_2 - 1parts
H_2O - 17parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
30 sec.

DI water
rinse, 5 min.

HPM

HCL - 1part
H_2O_2 - 1parts
H_2O - 17parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
30 sec.

DI water
rinse, 5 min.

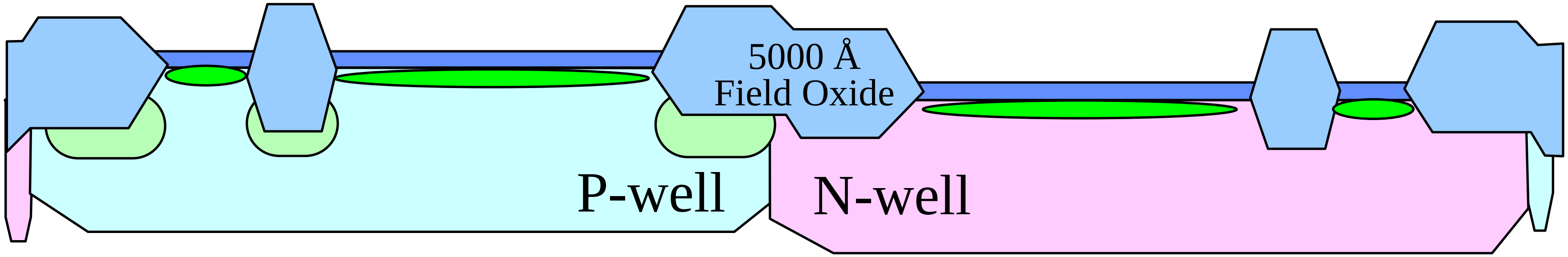
SPIN/RINSE
DRY

Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide

GROW GATE OXIDE

Oxide, 150A, Dry O_2

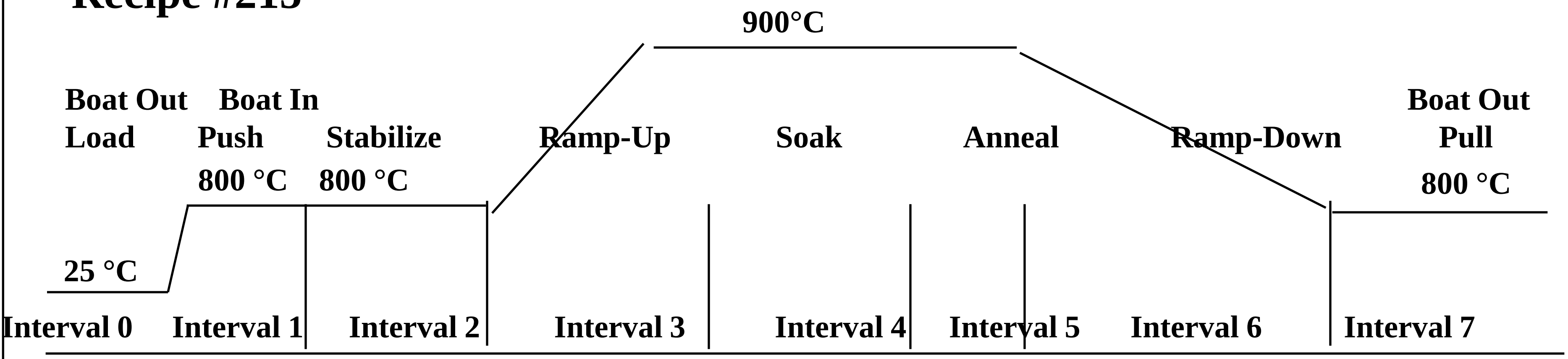
Bruce Furnace04 Recipe 215



BRUCE FURNACE RECIPE 215 – 150Å DRY OXIDE

Verified:2-24-04

Recipe #215



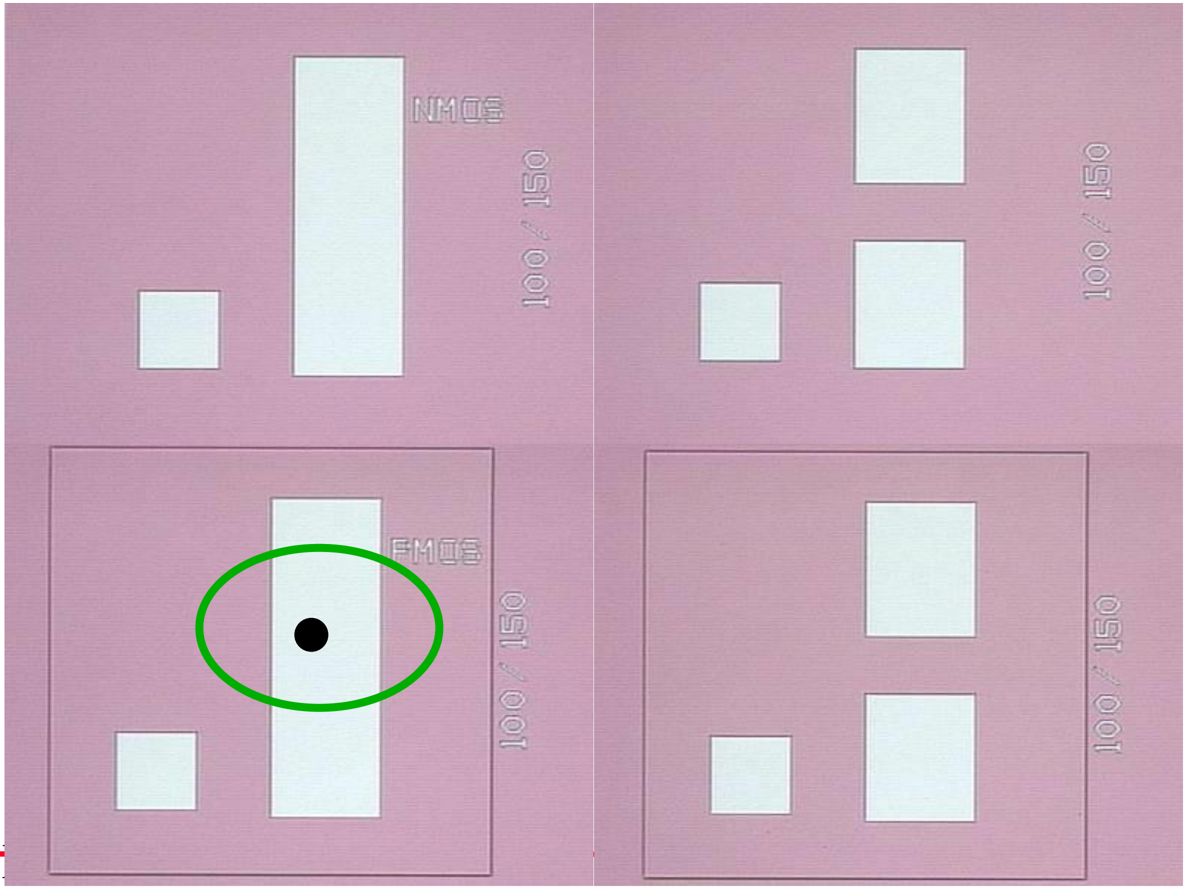
Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Boat Out Load	Boat In Push	Stabilize	Ramp-Up	Soak	Anneal	Ramp-Down	Boat Out Pull
25 °C	800 °C	800 °C		900°C			800 °C
Any	12 min	15 min	10 min	45 min	5 min	20 min	15 min
0 lpm	10 lpm	10 lmp	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Dry Oxide Growth, Target 150 Å

LOCATION FOR MEASUREMENT OF GATE OXIDE

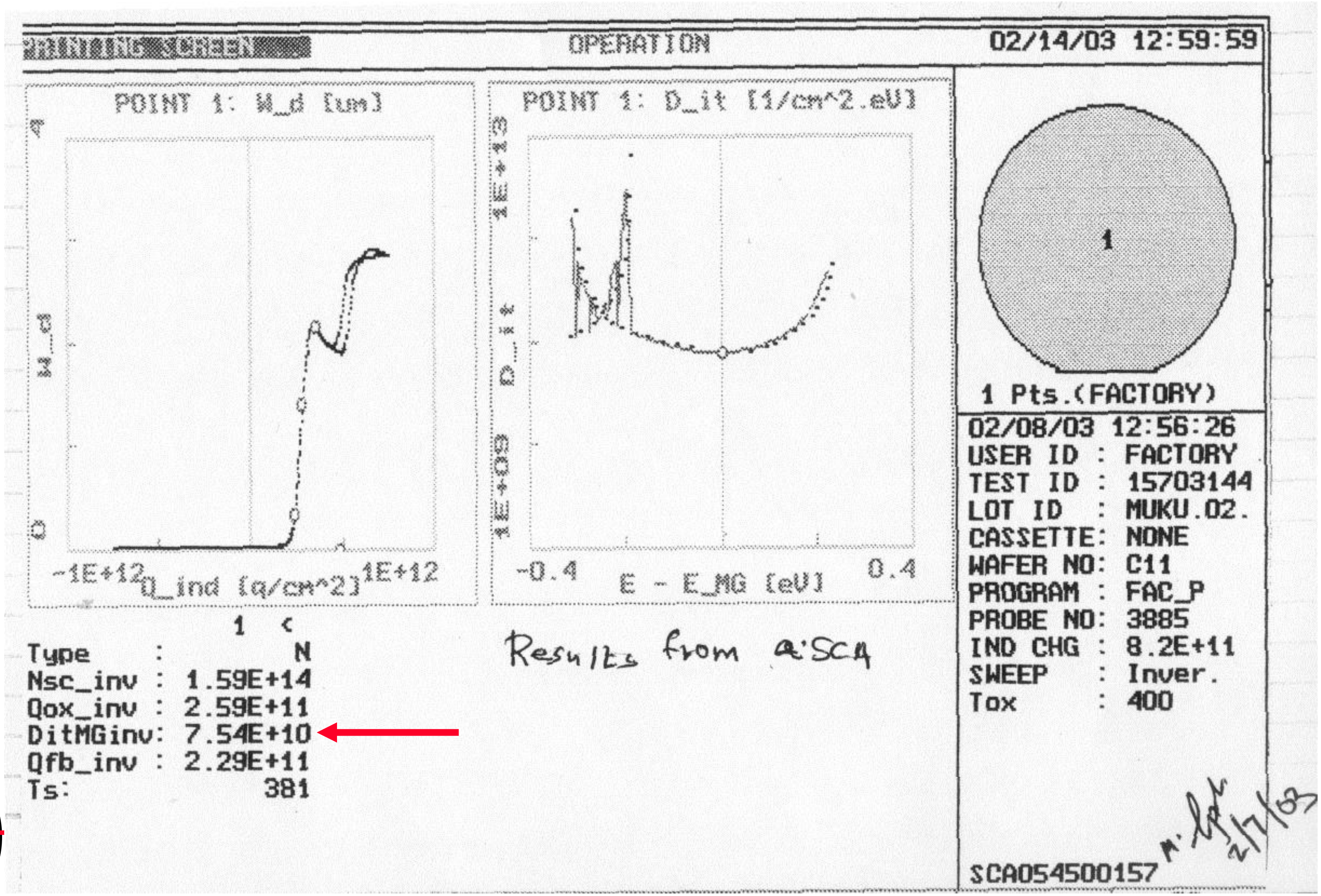
Measure gate oxide thickness (~150A) in white active area



MEASURE OXIDE QUALITY ON SCA-2500

Login: FACTORY
Password: OPER
<F1> Operate
<F1> Test Center the wafer on the stage
Select (use arrow keys on the numeric pad (far right on the keyboard)
space bar, page up, etc)
PROGRAM = FAC-P or FAC-N
LOT ID = HAWAII
WAFER NO. = C1
TOX = 250 (from nanospec)
<F12> start test and wait for measurement
<Print Screen> print results
<F8> exit and log off
<ESC> can be used anytime, but wait for
current test to be completed

SCA MEASUREMENT OF GATE OXIDE



```
OPERATION                                02/14/03 12:59:59
```

```
            1  <
Type      :     N
Nsc_inv  : 1.59E+14
Qox_inv  : 2.59E+11
DitMGinv: 7.54E+10
Qfb_inv  : 2.29E+11
Ts:          381
```

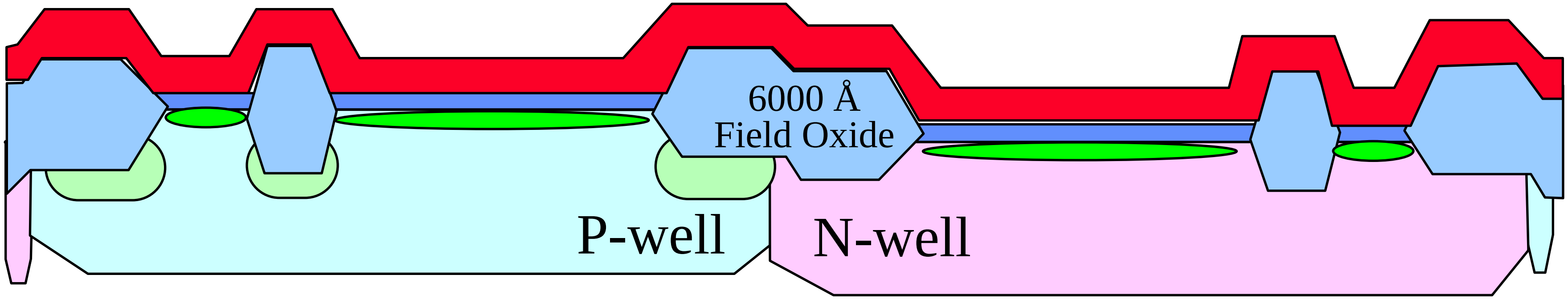
Results from a'SCA

```
02/08/03 12:56:26
USER ID  : FACTORY
TEST ID  : 15703144
LOT ID   : MUKU.02.
CASSETTE: NONE
WAFER NO: C11
PROGRAM  : FAC_P
PROBE NO: 3885
IND CHG  : 8.2E+11
SWEEP    : Inver.
Tox      : 400

SCA054500157
```

2/17/03

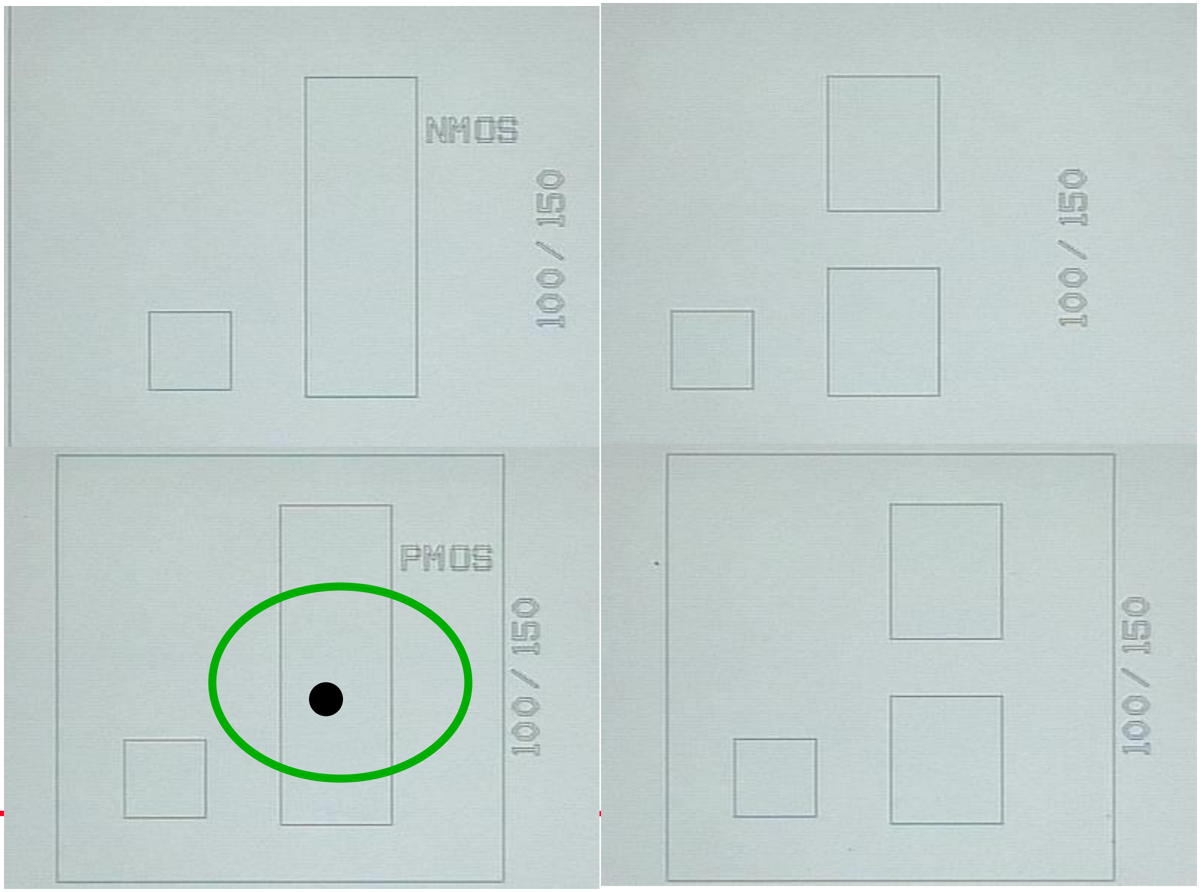
LPCVD POLY

Polysilicon, 5000A
LPCVD, 610C, 55 min

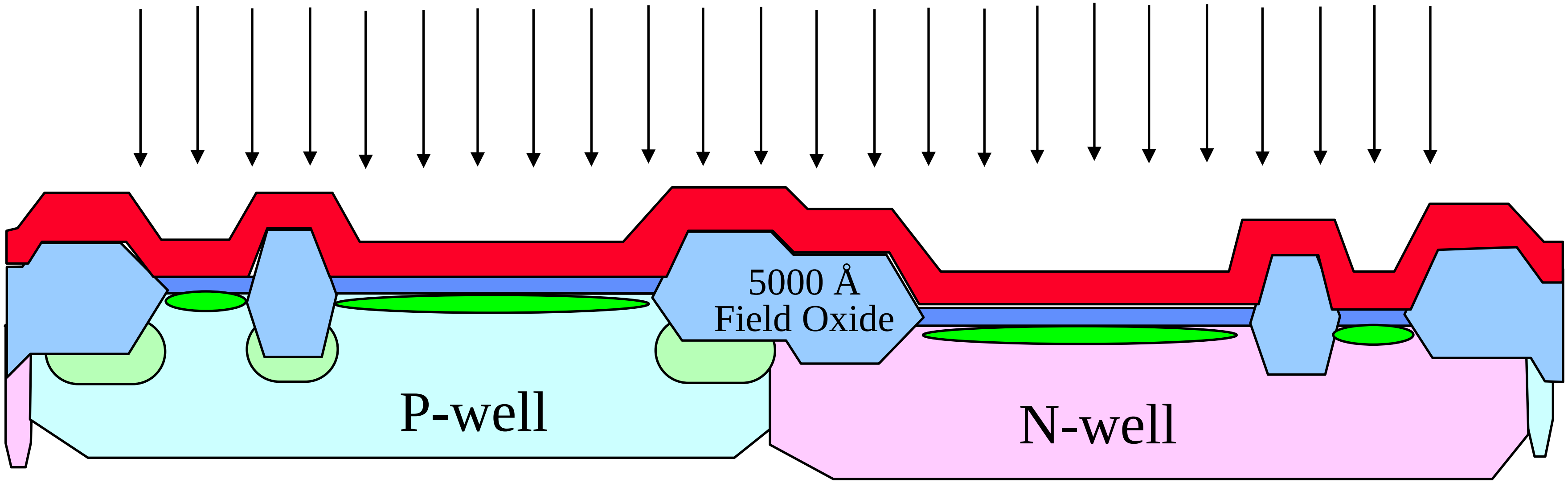


LOCATION FOR POLY THICKNESS MEASUREMENT

Measure poly thickness within active area using thin film stack #4 (poly on oxide) on nanospec



POLYSILICON DOPING

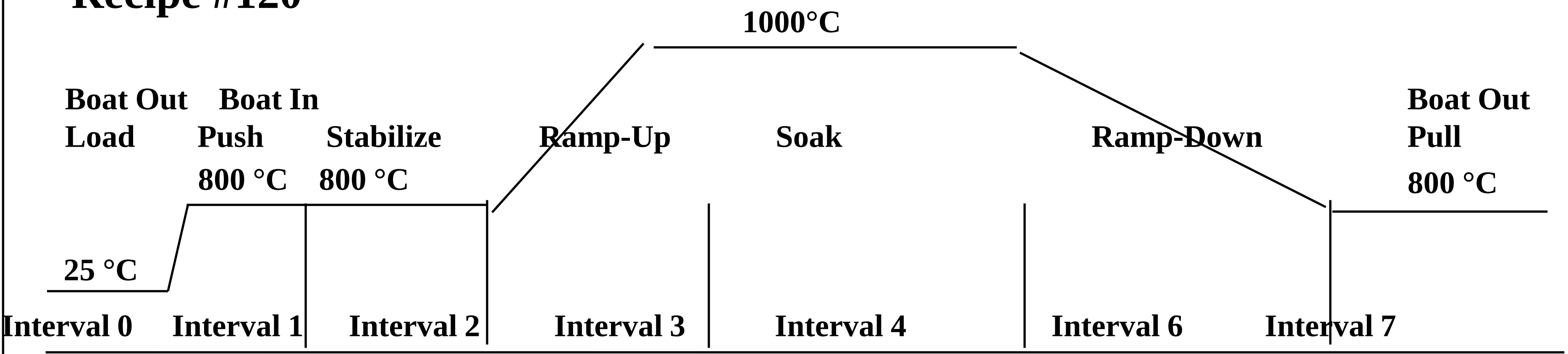


Ion Implant P31
Dose = 2E16
Energy = 50KeV
Time ~20 min at 400 µA
Anneal Tube 3 Recipe 120

BRUCE FURNACE RECIPE 120- N+ POLY DOPE

Recipe #120

Verified:2-24-04



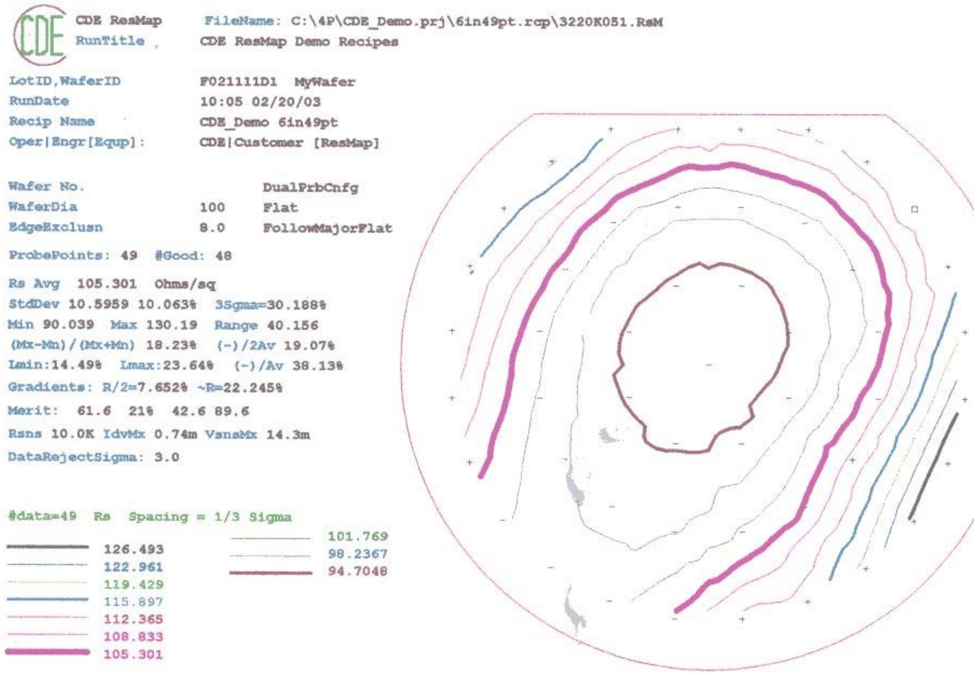
Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 6	Interval 7
Any	12 min	15 min	20 min	15 min	40 min	15 min
0 lpm	10 lpm	10 lmp	5 lpm	10 lpm	10 lpm	5 lpm
none	N2	N2	N2	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

N+ Poly Doping, Thin Poly, < 1 µm, No Oxide Growth

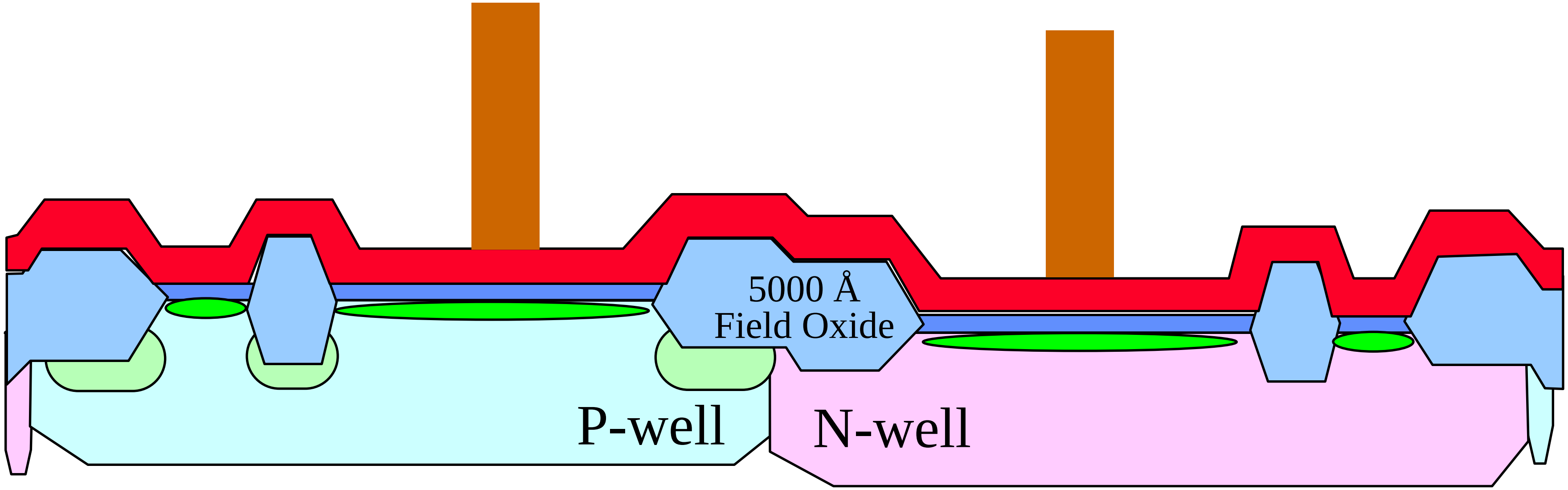
MEASURE POLY SHEET RESISTANCE

CDE Resistivity Mapper

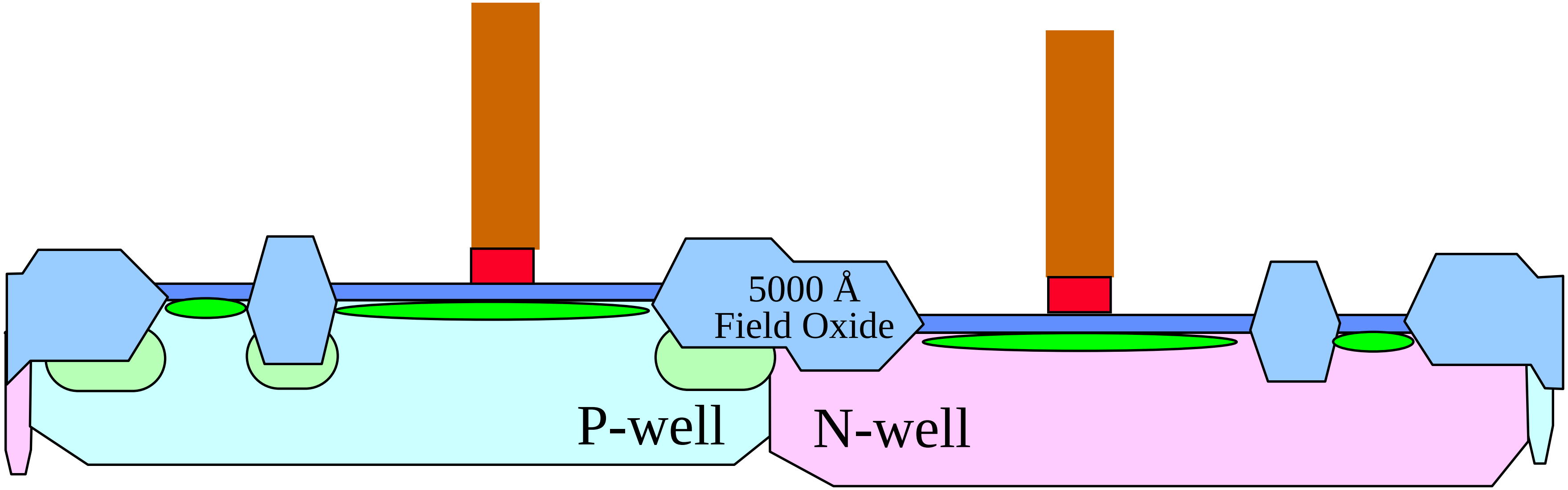


```
CDE ResMap        FileName: C:\4P\CDE_Demo.prj\6in49pt.rcp\3220K051.RsM
RunTitle          CDE ResMap Demo Recipes

LotID,WaferID          F021111D1  MyWafer
RunDate                10:05 02/20/03
Recip Name             CDE_Demo 6in49pt
Oper|Engr[Equp]:       CDE|Customer [ResMap]

Wafer No.                        DualPrbCnfg
WaferDia               100       Flat
EdgeExclusn            8.0       FollowMajorFlat

ProbePoints: 49  #Good: 48

Rs Avg  105.301  Ohms/sq
StdDev 10.5959 10.063%  3Sgma=30.188%
Min 90.039  Max 130.19  Range 40.156
(Mx-Mn)/(Mx+Mn) 18.23%  (-)/2Av 19.07%
Imin:14.49%  Imax:23.64%  (-)/Av 38.13%
Gradients: R/2=7.652% ~R=22.245%
Merit:  61.6  21%  42.6 89.6
Rsns 10.0K IdvMx 0.74m VsnsMx 14.3m
DataRejectSigma: 3.0

#data=49  Rs  Spacing = 1/3 Sigma

           126.493                101.769
           122.961                98.2367
           119.429                94.7048
           115.897
           112.365
           108.833
           105.301
```

PHOTO 5 POLY GATE

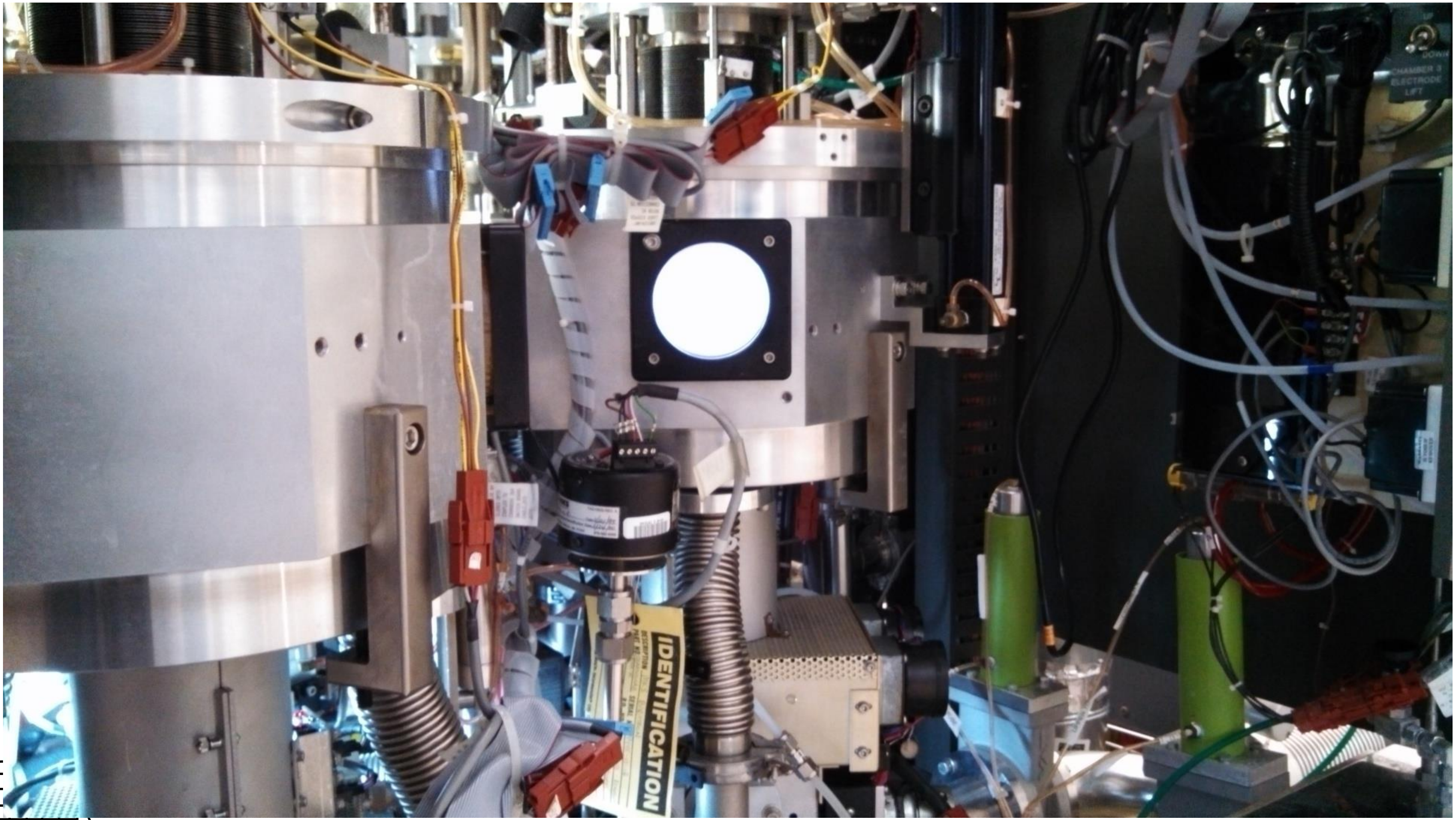


POLY ETCH

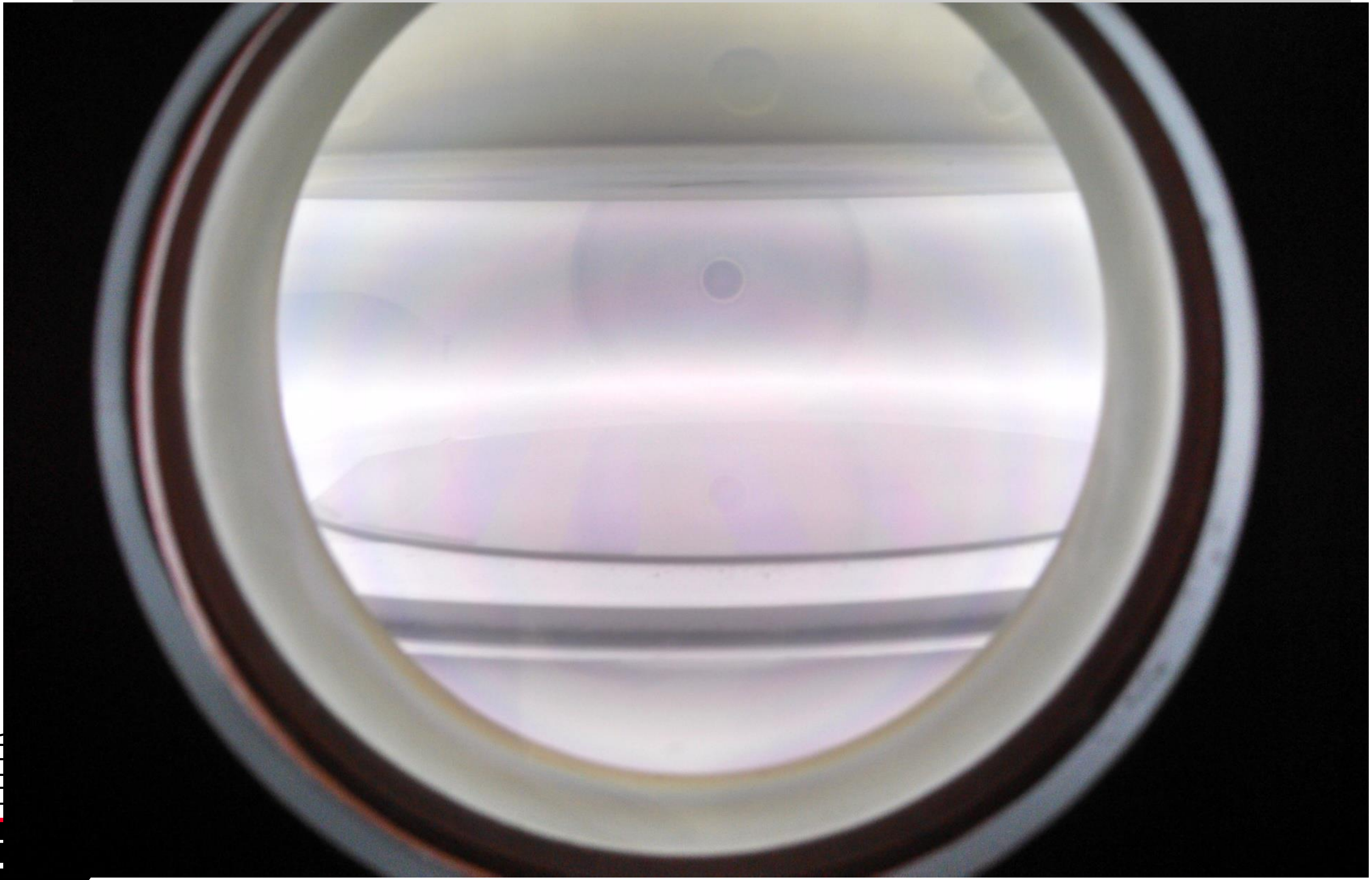


DRYTEK QUAD RIE TOOL

2 OF 4 CHAMBERS IN THE DRYTEK QUAD RIE TOOL



PLASMA ETCHING IN THE DRYTEK QUAD



ANISOTROPIC POLY GATE ETCH RECIPE

Anisotropic Poly Gate Etch Recipe

SF6 30 sccm, CHF3 30 sccm, O2 5 sccm, RF Power 160 w, Pressure 40 mTorr, 1900 A/min (Anisotropic), Resist Etch Rate 300 A/min, Oxide Etch Rate 200 A/min

Recipe Name:	FACPOLY Step 2
Chamber	2
Power	160 watts
Pressure	40 mTorr
Gas	SF6
Flow	30 sccm
Gas	CHF3
Flow	30 sccm
Gas	O2
Flow	5 sccm
Poly Etch Rate	1150 Å/min
Photoresist Etch Rate:	300 Å/min
Oxide Etch Rate:	200 Å/min

Endpoint See Video
http://people.rit.edu/lffeee/videos.htm

POLY ETCH WITH END POINT


LAM 490 Plasma Etcher

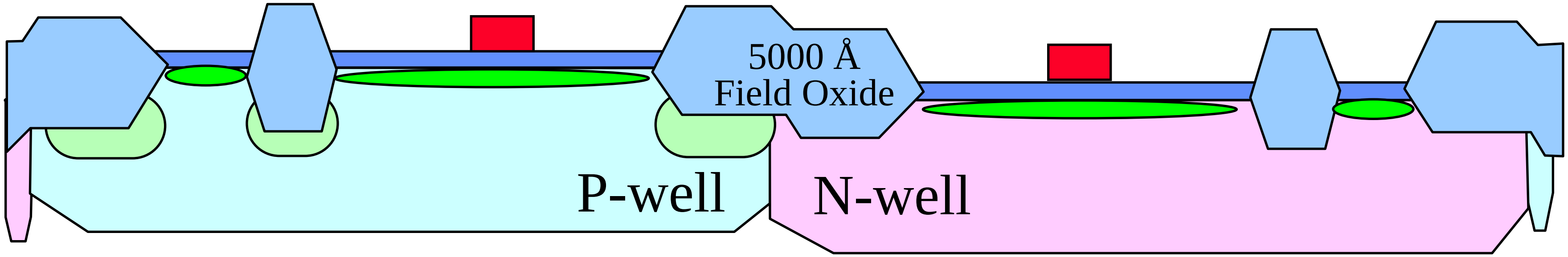
Process: Step 1 – 325mTorr; 0 watts
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Max Time = 2 min.
Time Only

Process: Step 2 – 325mTorr; 100 watts,
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Max Time = 1 min. 15 sec
Time or Endpoint
Endpoint and Time
Sampling A (ch12 @ 520nm)
Active during step 02
Delay 15sec before normalizing
Normalize for 10sec
Trigger at 90%

Process: Step 3 – 325mTorr; 140W,
Gap = 1.5 cm
140sccm SF6, 15 sccm O2
Overetch – 10%

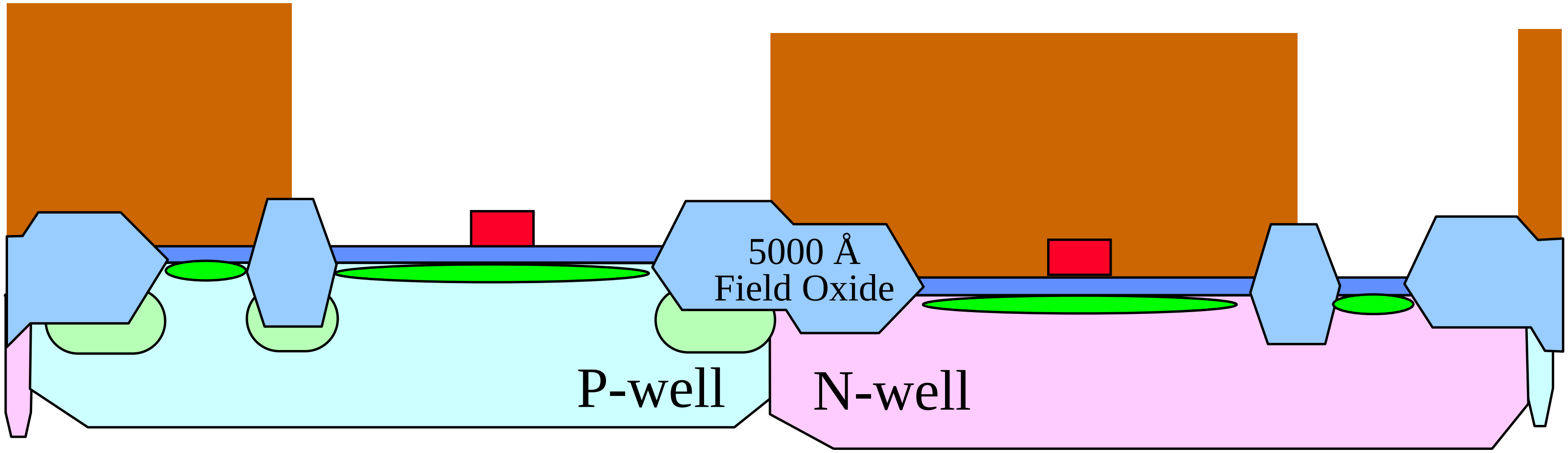
FPOLY6K.RCP

STRIP RESIST



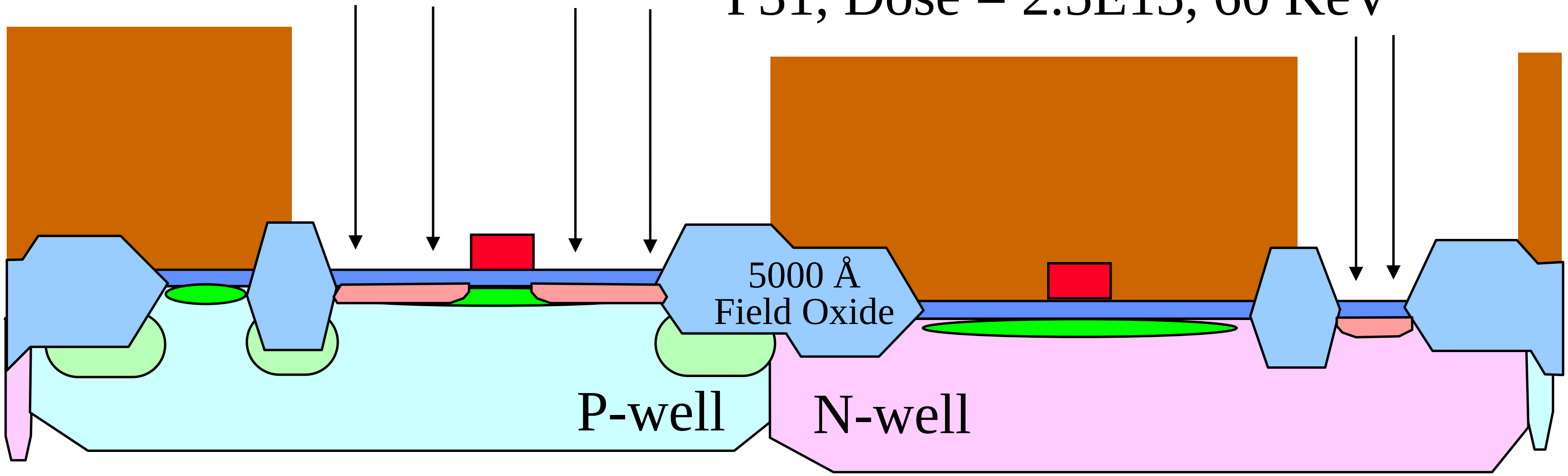
Strip Photresist in Branson Asher
Using Recipe 6"FACTORY

PHOTO 6 LDD N-TYPE IMPLANT

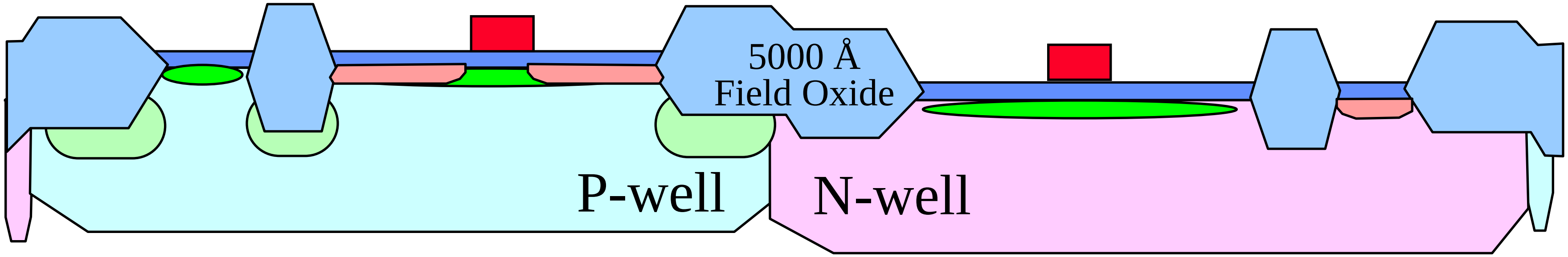


IMPLANT LDD

P31, Dose = 2.5E13, 60 KeV

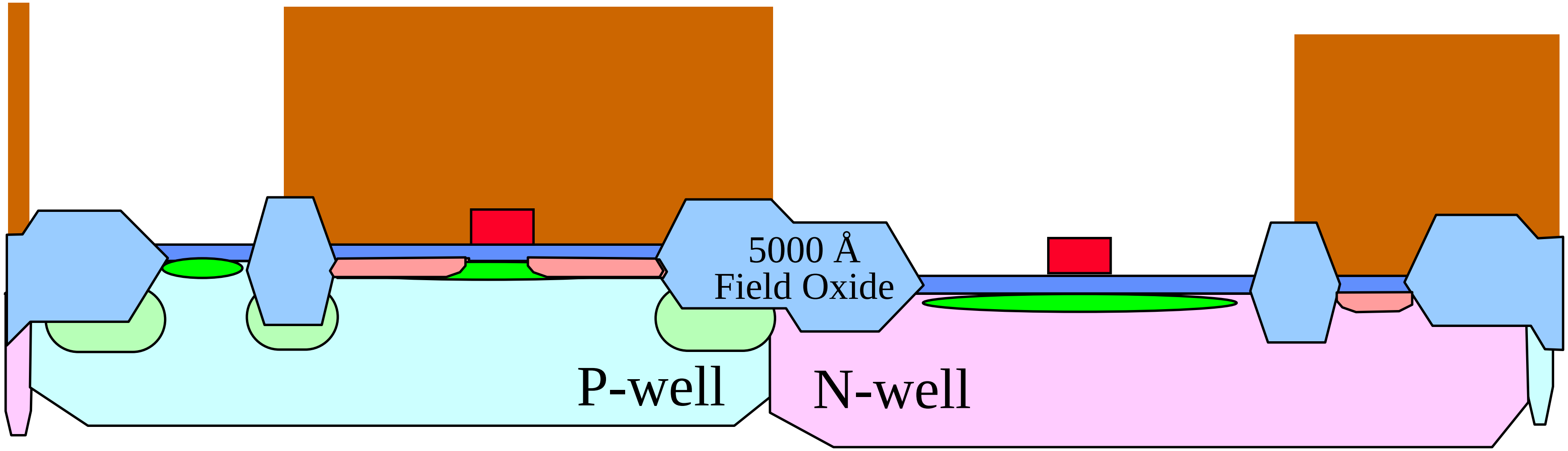


STRIP RESIST



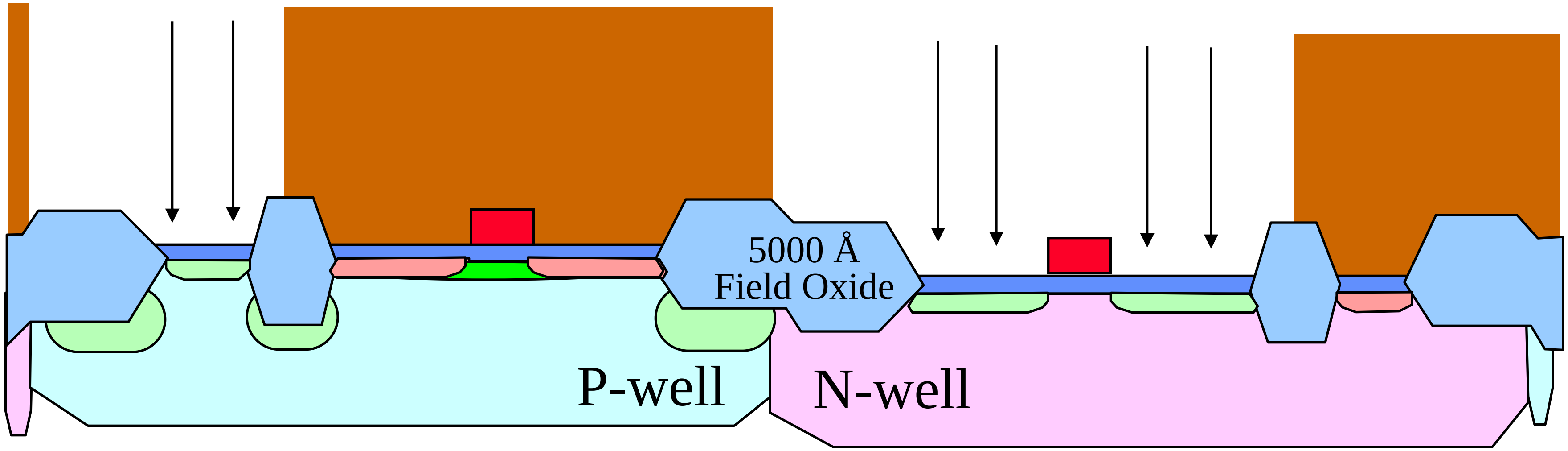
Strip Photresist in Gasonics Asher
Using Recipe FF

PHOTO 7 LDD P-TYPE IMPLANT

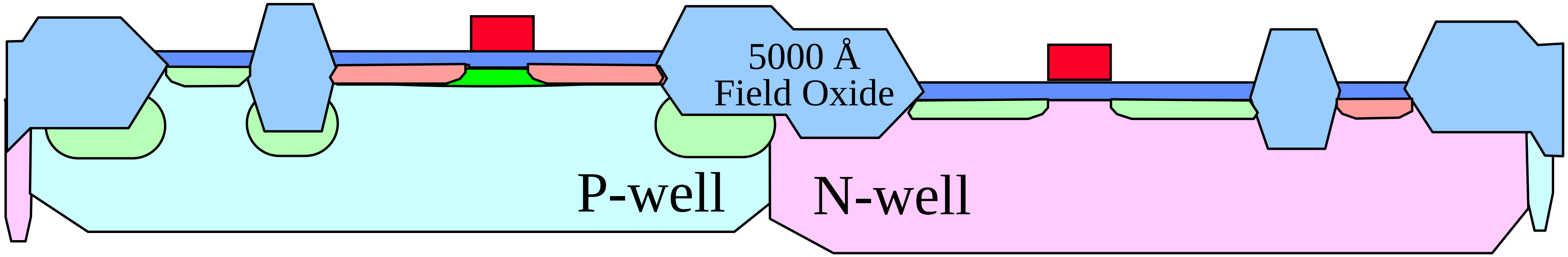


IMPLANT LDD

B11, Dose = 4E13, E = 50 KeV



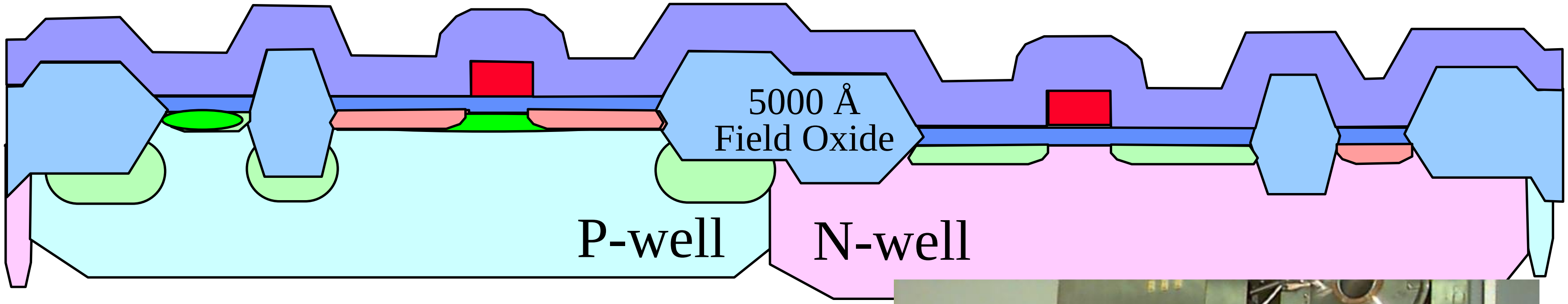
STRIP RESIT

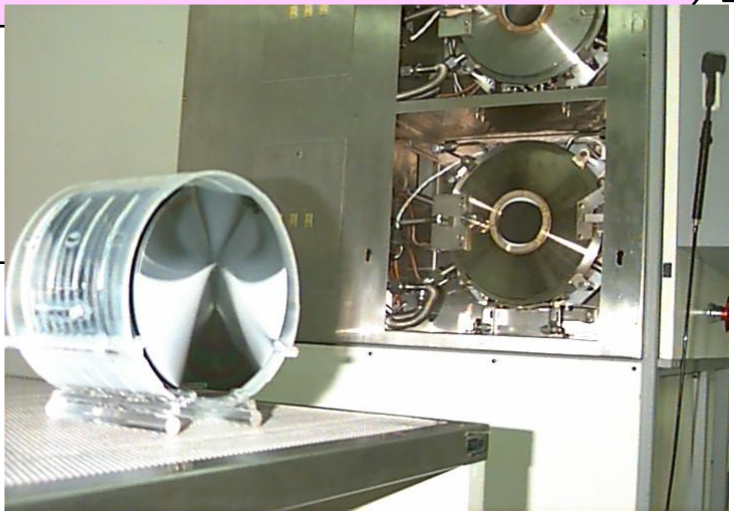


Strip Photresist in Gasonics Asher
Using Recipe FF

LPCVD OXIDE

Target 5000 Å





ASM 6” LPCVD Tool

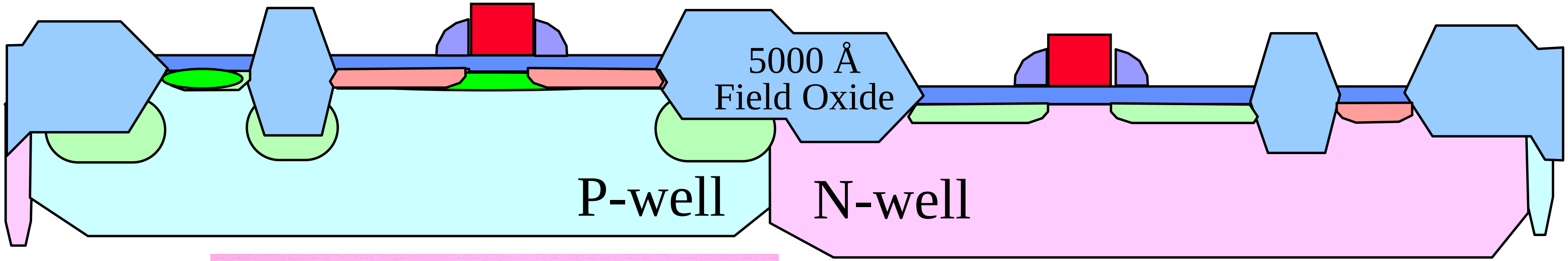
PECVD OXIDE FROM TEOS

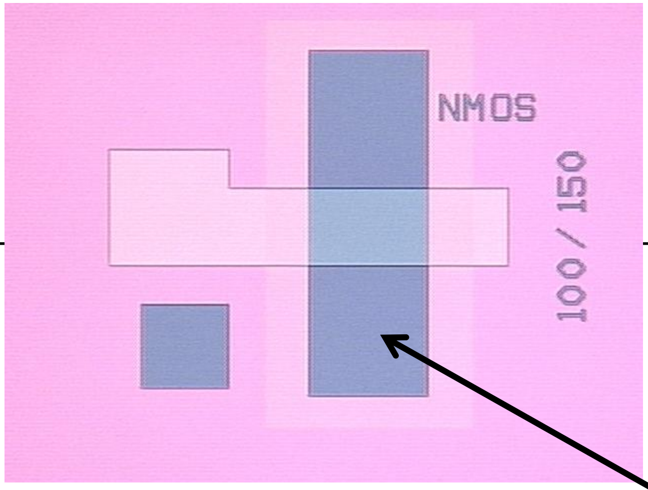
TEOS Program: (Chamber A)
Step 1
- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 2 – Deposition
- Dep Time = 55 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

Step 3 – Clean
- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

ETCH OXIDE TO FORM SIDE WALL SPACERS





Drytek Quad
Recipe FACSPCR
65 sccm Ar
65 sccm CHF3
5 sccm O2
Power = 200 watts
Pressure = 70 mTorr

Measure remaining oxide here

SIDE WALL SPACER ETCH IN DRYTEK QUAD

Drytek Quad
Recipe FACSPCR
65 sccm Ar
65 sccm CHF_3
5 sccm O_2
Power = 200 watts
Pressure = 70 mTorr
Thermal Oxide Etch Rate = 330 Å/min
LTO/TEOS Etch Rate = 1000 Å/min
Annealed TEOS Etch Rate 400 Å/min
Photoresist Etch Rate = 200 Å/min

Etch 5 min, Measure remaining Oxide
Should be less than 1000Å

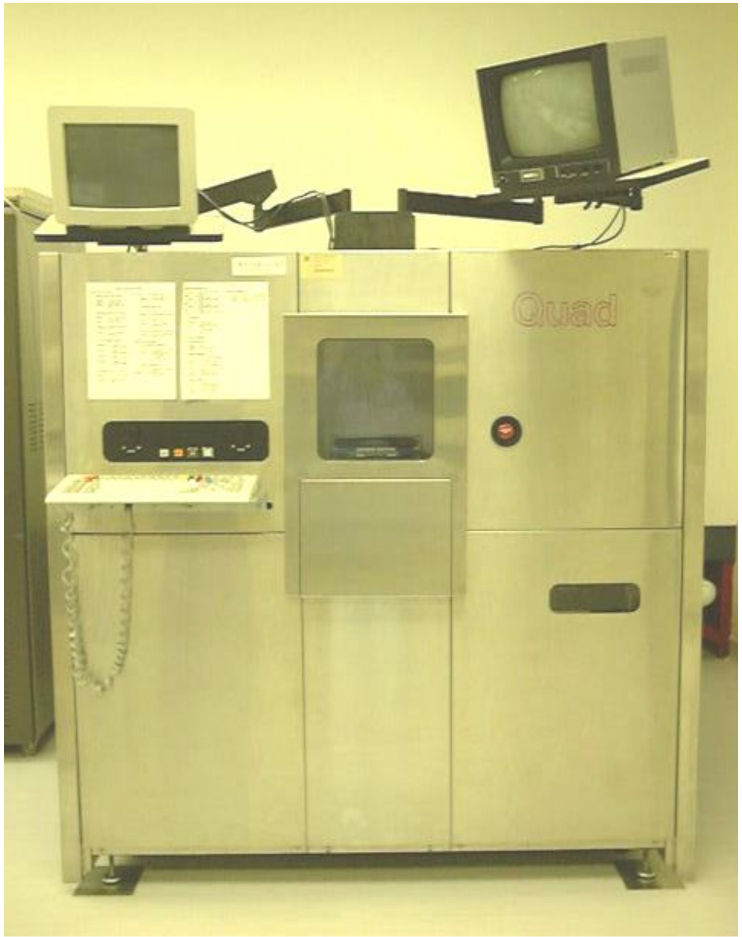
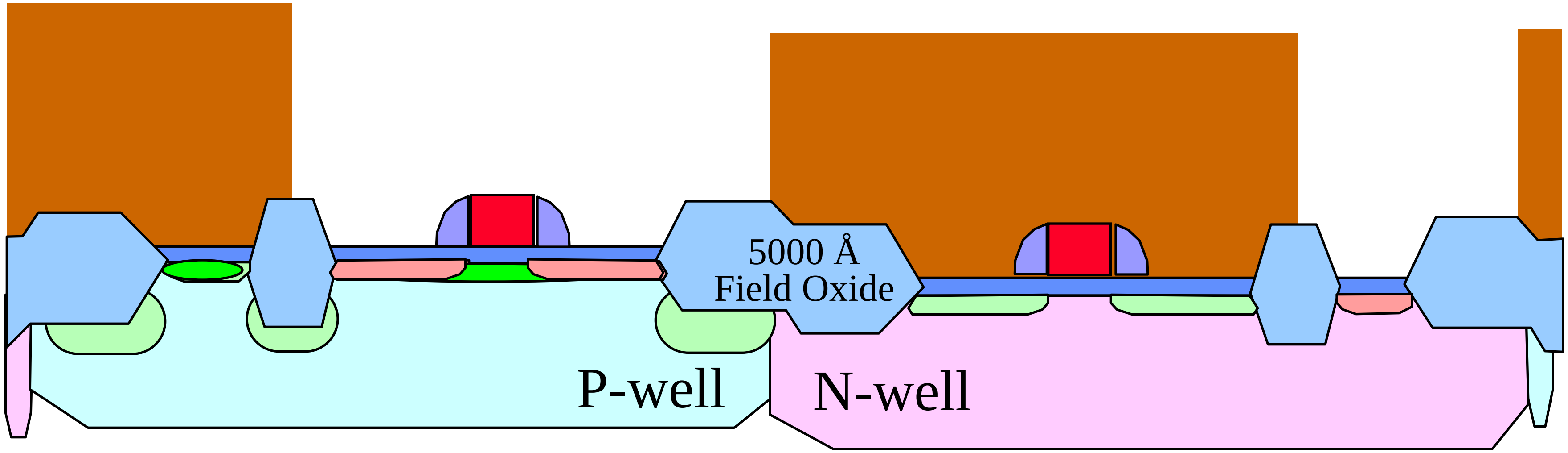
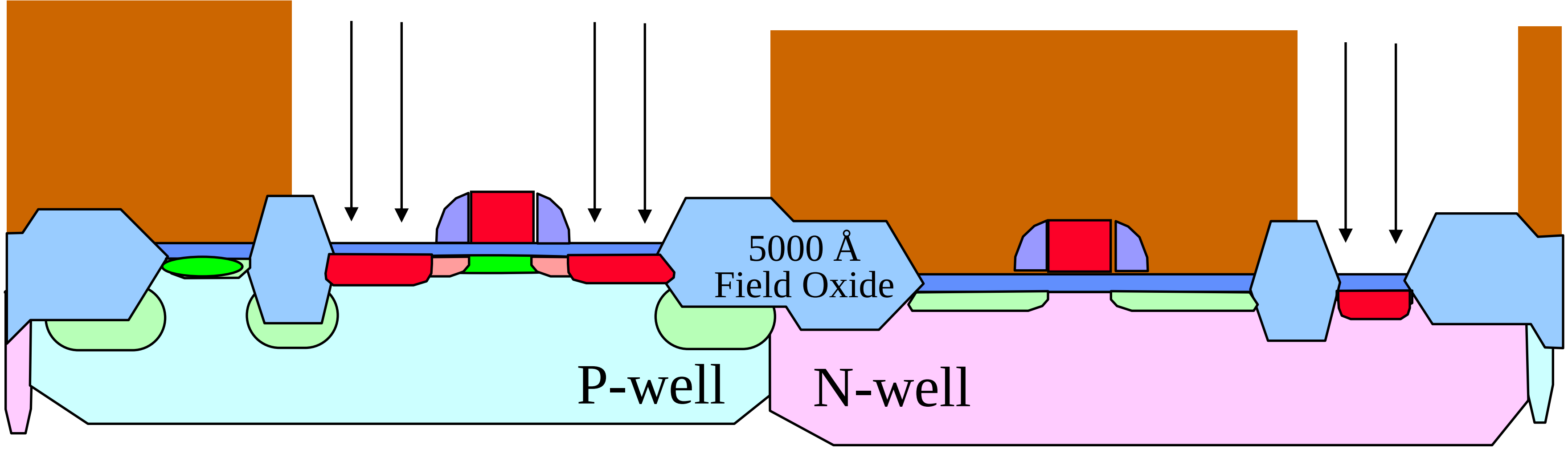


PHOTO 8 N+ D/S

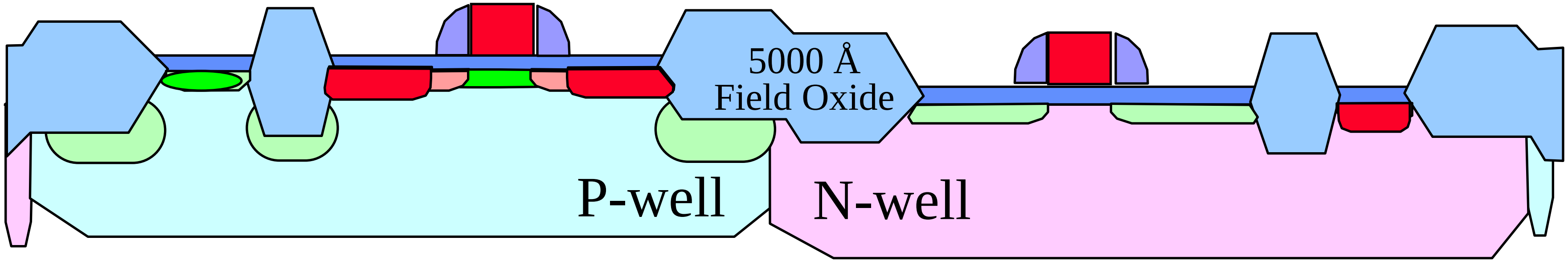


IMPLANT N+ D/S

P31, Dose = 2 E15, E = 60 KeV

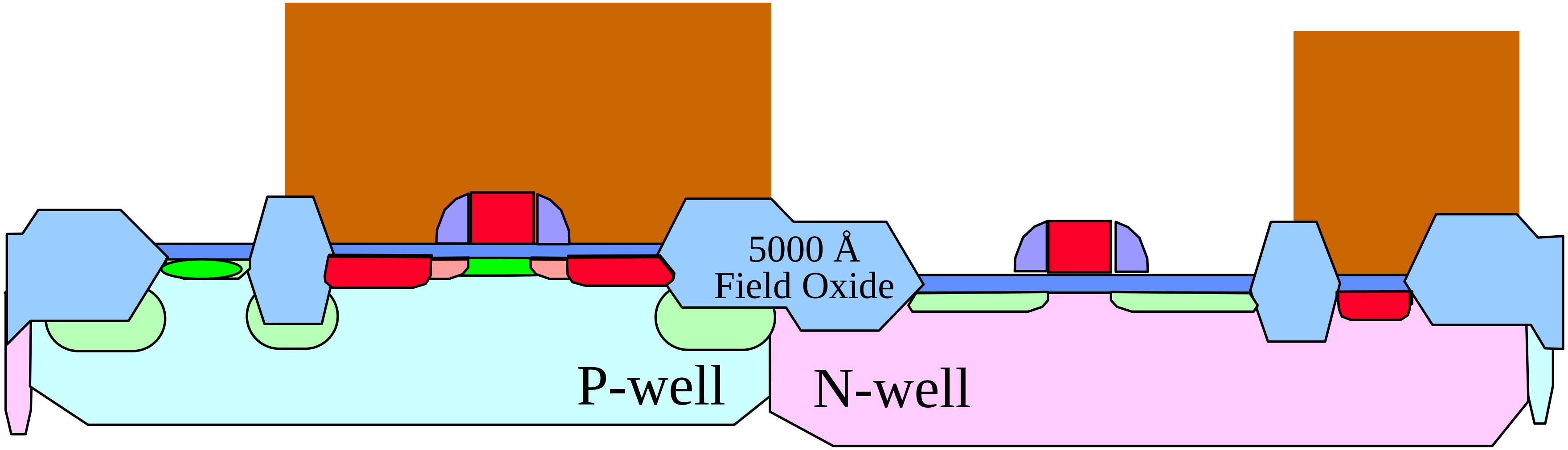


STRIP RESIST



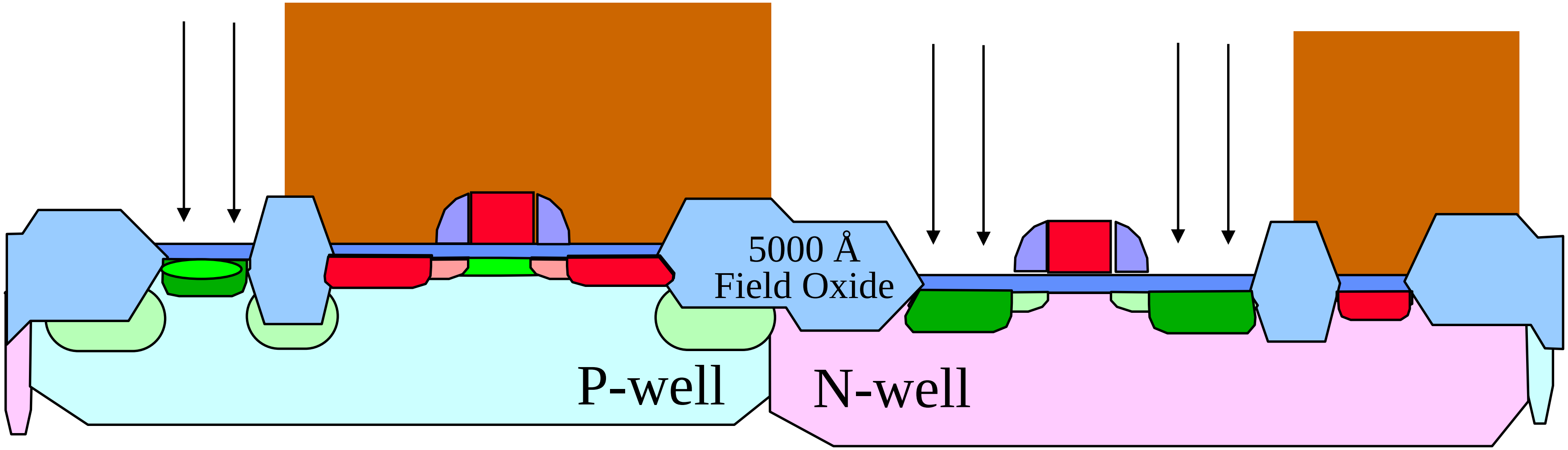
Strip Photresist in Branson Asher
Using Recipe 6”FACTORY

PHOTO 9 P+ D/S

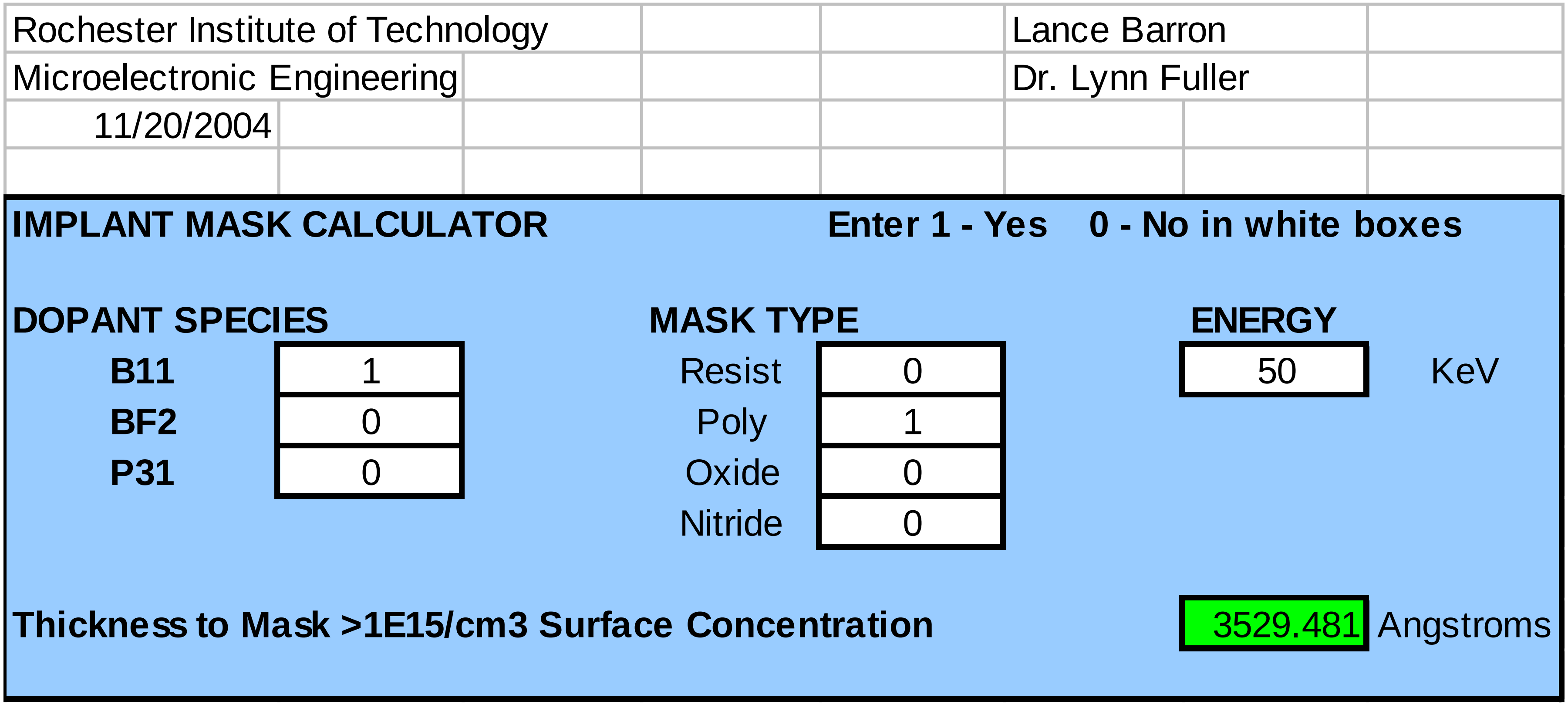


IMPLANT P+ D/S

B11, Dose = 2 E15, E = 50 KeV



IMPLANT MASKING THICKNESS CALCULATOR



Rochester Institute of Technology

Microelectronic Engineering

11/20/2004

Lance Barron

Dr. Lynn Fuller

IMPLANT MASK CALCULATOR **Enter 1 - Yes 0 - No in white boxes**

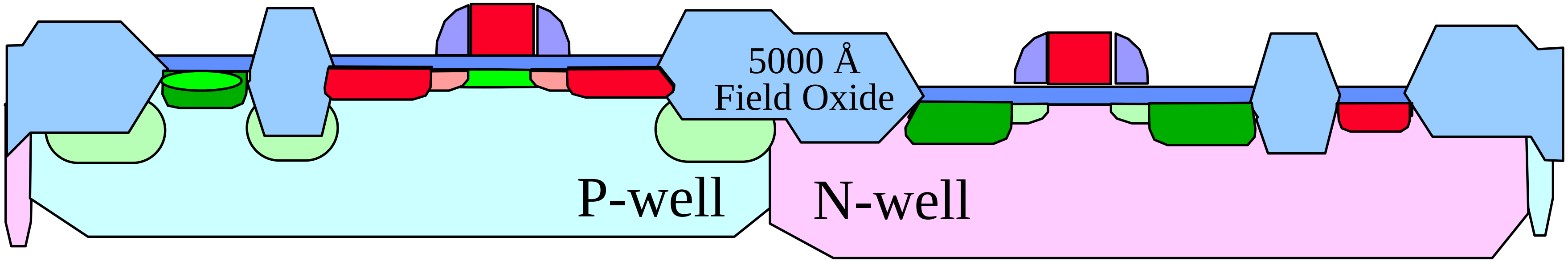
DOPANT SPECIES	
B11	1
BF2	0
P31	0

MASK TYPE	
Resist	0
Poly	1
Oxide	0
Nitride	0

ENERGY 50 KeV

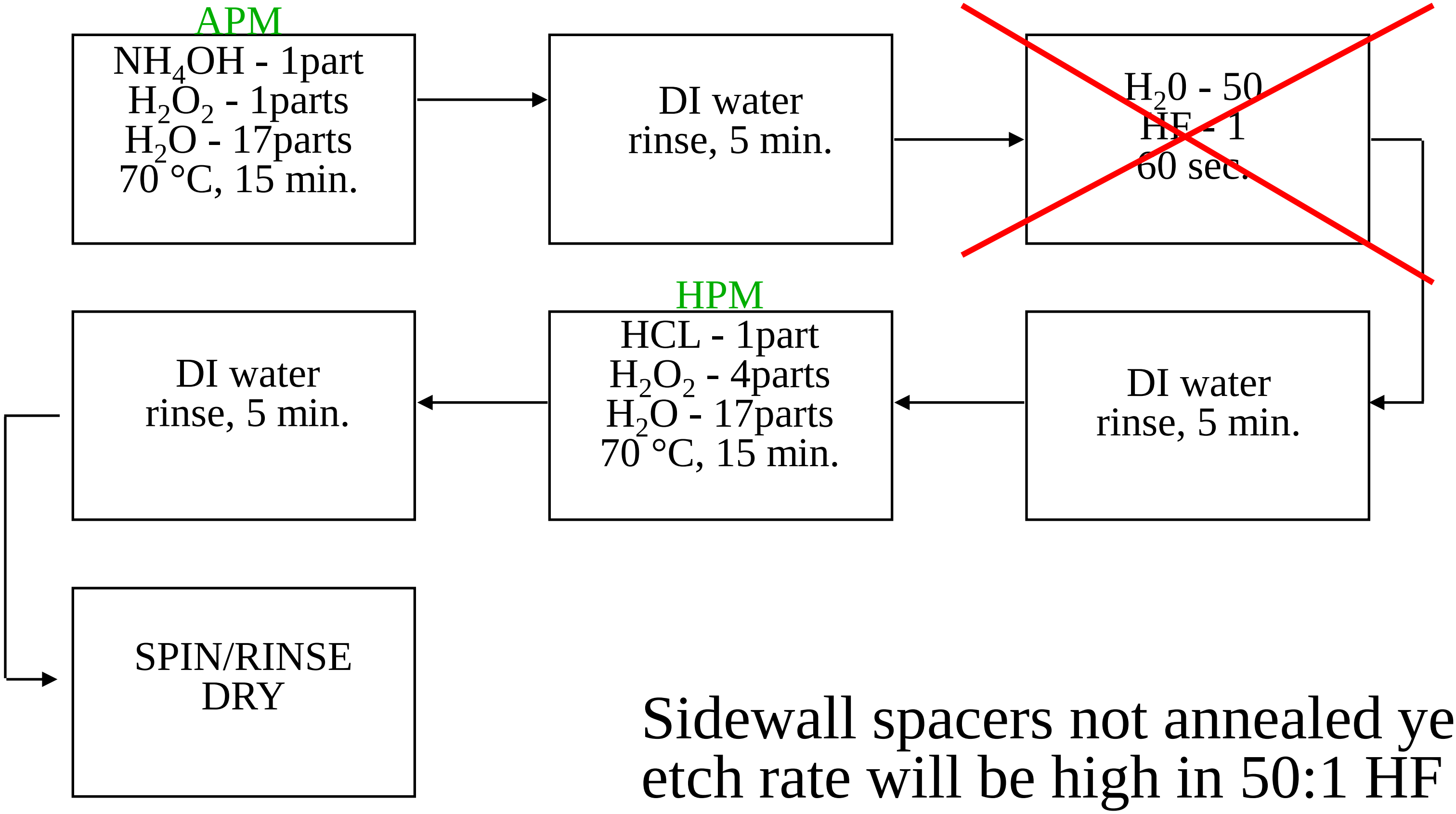
Thickness to Mask >1E15/cm3 Surface Concentration 3529.481 Angstroms

STRIP RESIST, RCA CLEAN



Strip Photresist in Gasonics Asher
Using Recipe FF

SPECIAL RCA CLEAN (NO 50:1 HF)



APM
NH_4OH - 1part
H_2O_2 - 1parts
H_2O - 17parts
70 °C, 15 min.

DI water
rinse, 5 min.

~~H_20 - 50~~
~~HF - 1~~
~~60 sec.~~

DI water
rinse, 5 min.

HPM
HCL - 1part
H_2O_2 - 4parts
H_2O - 17parts
70 °C, 15 min.

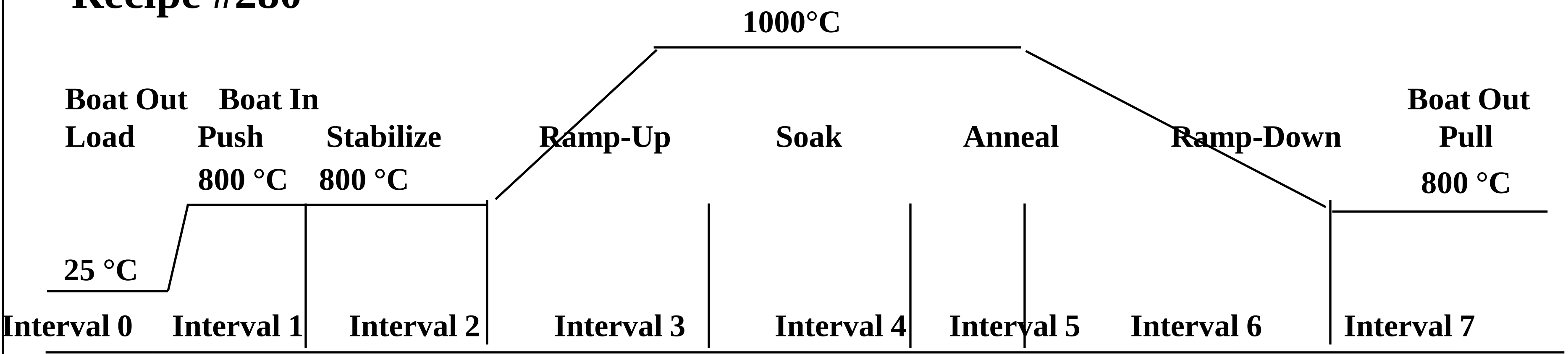
DI water
rinse, 5 min.

SPIN/RINSE
DRY

Sidewall spacers not annealed yet so etch rate will be high in 50:1 HF

ANNEAL DRAIN/SOURCE IMPLANTS

Recipe #280



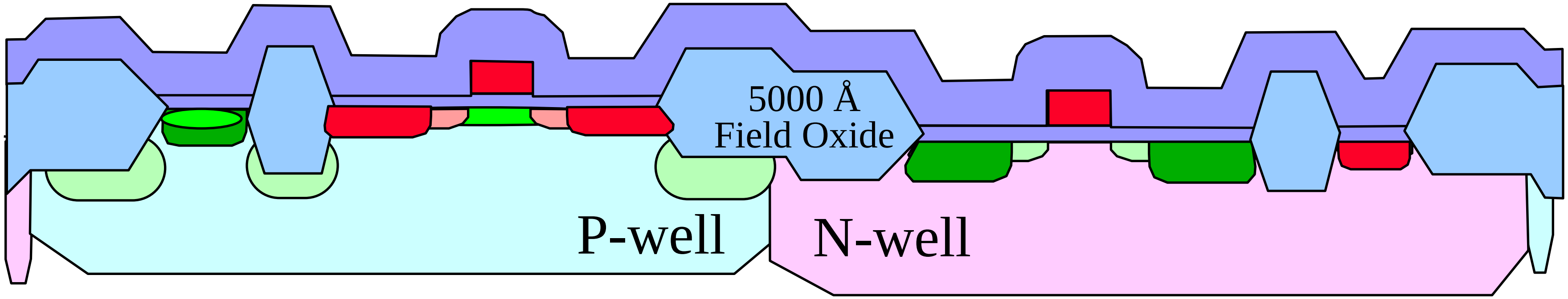
Interval 0	Interval 1	Interval 2	Interval 3	Interval 4	Interval 5	Interval 6	Interval 7
Any	12 min	15 min	20 min	20 min	5 min	40 min	15 min
0 lpm	10 lpm	10 lmp	5 lpm	10 lpm	15 lpm	10 lpm	5 lpm
none	N2	N2	O2	O2/	N2	N2	N2

At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

DS Implant Anneal, Oxide Growth

RCA CLEAN AND DEPOSIT CVD OXIDE

Target 5000 Å



Oxide by LTO CVD or PECVD from TEOS

PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)

Step 1

- Setup Time = 15 sec
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 0 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

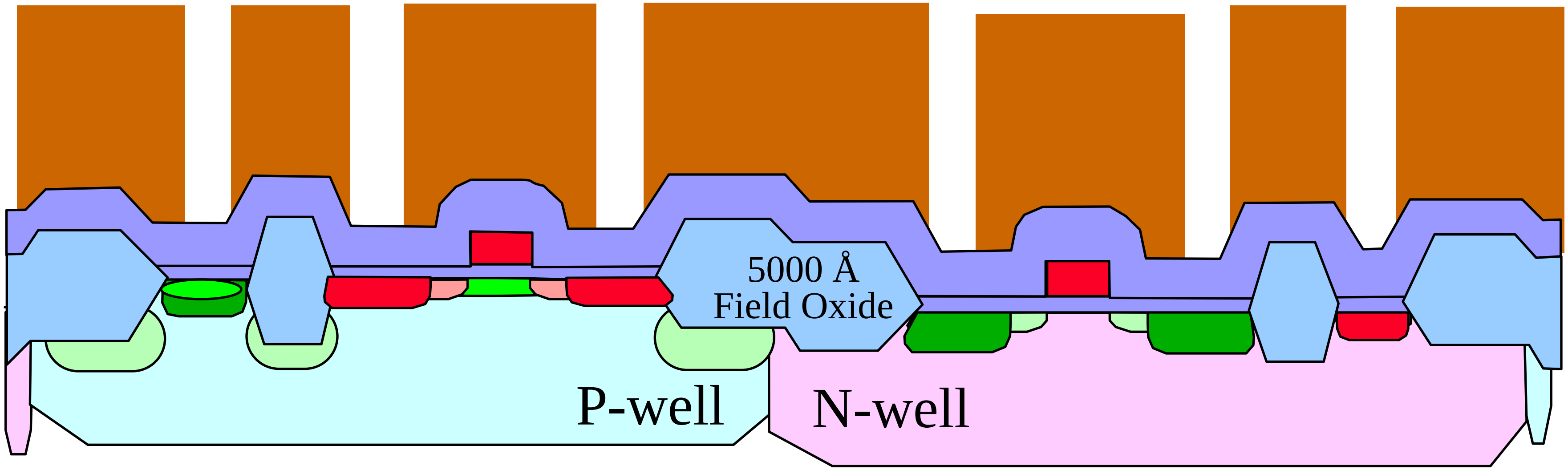
Step 2 – Deposition

- Dep Time = 60 sec (5000 Å)
- Pressure = 9 Torr
- Susceptor Temperature= 390 C
- Susceptor Spacing= 220 mils
- RF Power = 205 watts
- TEOS Flow = 400 scc
- O2 Flow = 285 scc

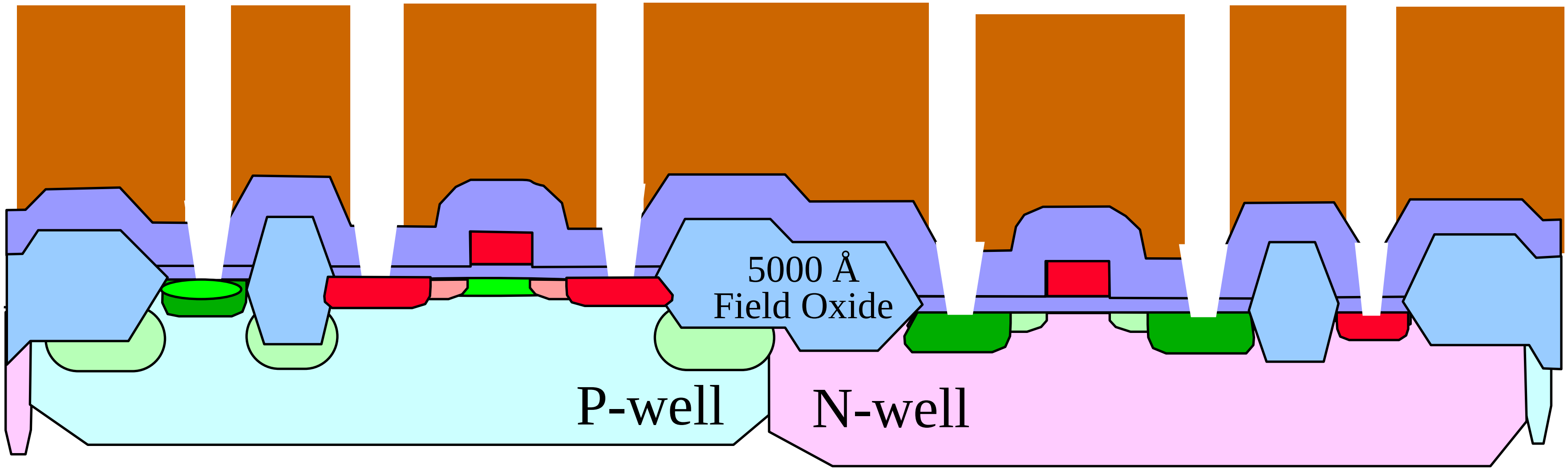
Step 3 – Clean

- Time = 10 sec
- Pressure = Fully Open
- Susceptor Temperature= 390 C
- Susceptor Spacing= 999 mils
- RF Power = 50 watts
- TEOS Flow = 0 scc
- O2 Flow = 285 scc

PHOTO 10 CONTACT CUTS



ETCH CONTACT CUTS



Plasma Etch
Using FACCUT in Drytek Quad
200 Watt, 100 mTorr
50 sccm CHF3, 10 sccm CF4
100 sccm Ar

DRYTEK QUAD ETCH RECIPE FOR CC AND VIA

Recipe Name:		FACCUT
Chamber		3
Power		200W
Pressure		100 mTorr
Gas 1	CHF3	50 sccm
Gas 2	CF4	10 sccm
Gas 3	Ar	100 sccm
Gas 4	O2	0 sccm

(could be changed to N2)

TEOS Etch Rate	494	Å/min
Annealed TEOS	450	Å/min
Photoresist Etch Rate:	117	Å/min
Thermal Oxide Etch Rate:	441	Å/min
Silicon Etch Rate	82	Å/min
TiSi2 Etch Rate	1	Å/min

US Patent 5935877 - Etch process for forming contacts over titanium silicide

Drytek Quad

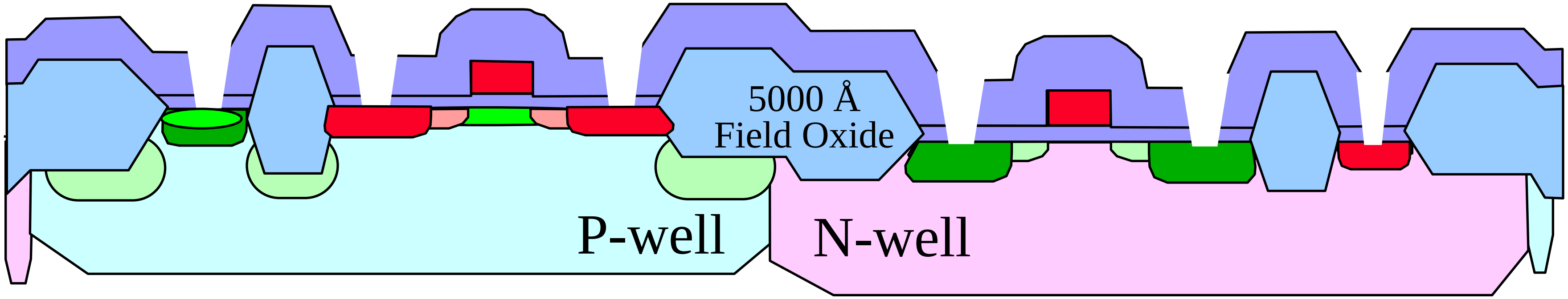
CONTACT CUT ETCH RECIPE

Theory: The CHF3 and CF4 provide the F radicals that do the etching of the silicon dioxide, SiO2. The high voltage RF power creates a plasma and the gasses in the chamber are broken into radicals and ions. The F radical combines with Si to make SiF4 which is volatile and is removed by pumping. The O2 in the oxide is released and also removed by pumping. The C and H can be removed as CO, CO2, H2 or other volatile combinations. The C and H can also form hydrocarbon polymers that can coat the chamber and wafer surfaces. The Ar can be ionized in the plasma and at low pressures can be accelerated toward the wafer surface without many collisions giving some vertical ion bombardment on the horizontal surfaces. If everything is correct (wafer temperature, pressure, amounts of polymer formed, energy of Ar bombardment, etc.) the SiO2 should be etched, polymer should be formed on the horizontal and vertical surfaces but the Ar bombardment on the horizontal surfaces should remove the polymer there. The O2 (O radicals) released also help remove polymer. Once the SiO2 is etched and the underlying Si is reached there is less O2 around and the removal of polymer on the horizontal surfaces is not adequate thus the removal rate of the Si is reduced. The etch rate of SiO2 should be 4 or 5 times the etch rate of the underlying Si. The chamber should be cleaned in an O2 plasma after each wafer is etched.

US Patent 5935877 - Etch process for forming contacts over Titanium Silicide

STRIP RESIST, RCA CLEAN

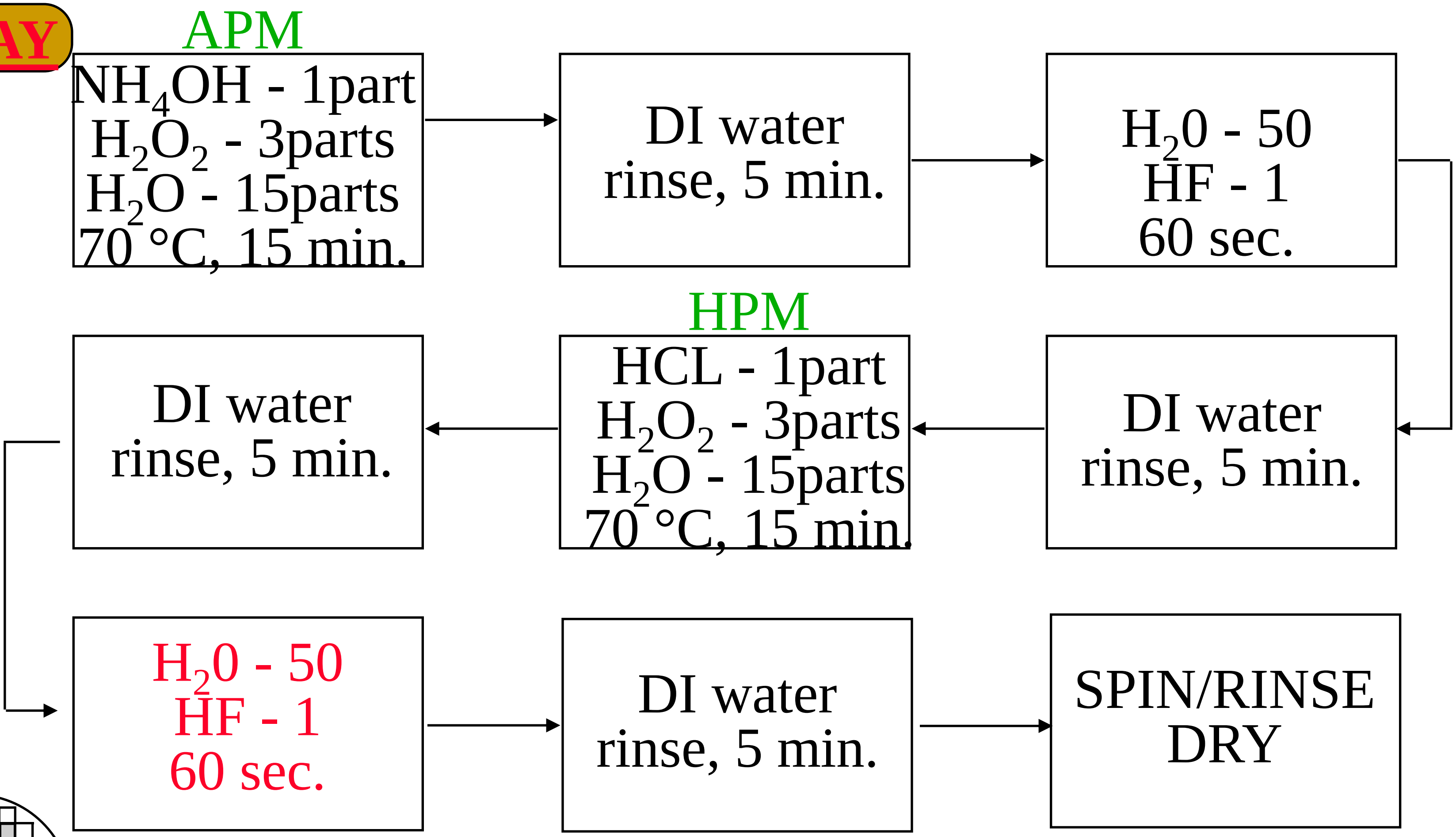
Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide



Include D1-D3
Strip Photresist in Asher

SPECIAL RCA CLEAN (TWO 50:1 HF STEPS)

PLAY



APM
NH_4OH - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

H_20 - 50
HF - 1
60 sec.

DI water
rinse, 5 min.

HPM
HCL - 1part
H_2O_2 - 3parts
H_2O - 15parts
70 °C, 15 min.

DI water
rinse, 5 min.

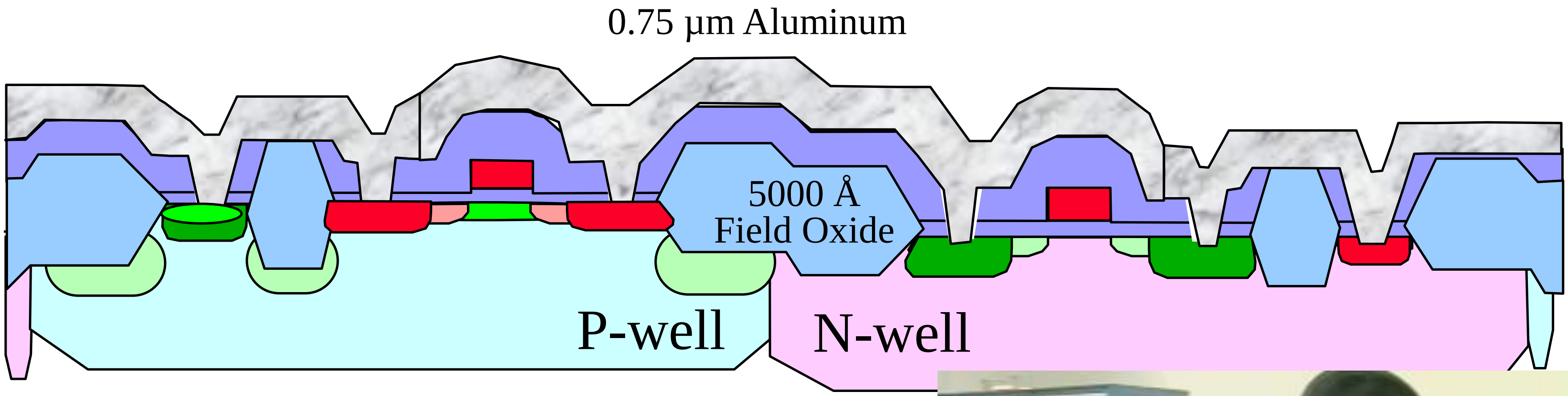
H_20 - 50
HF - 1
60 sec.

DI water
rinse, 5 min.

SPIN/RINSE
DRY

Clean includes 50:1 HF Dip twice once after each bath to remove chemically grown oxide

DEPOSIT METAL



CVC 601 Sputter Tool

CVC 601 SPUTTER THICKNESS UNIFORMITY

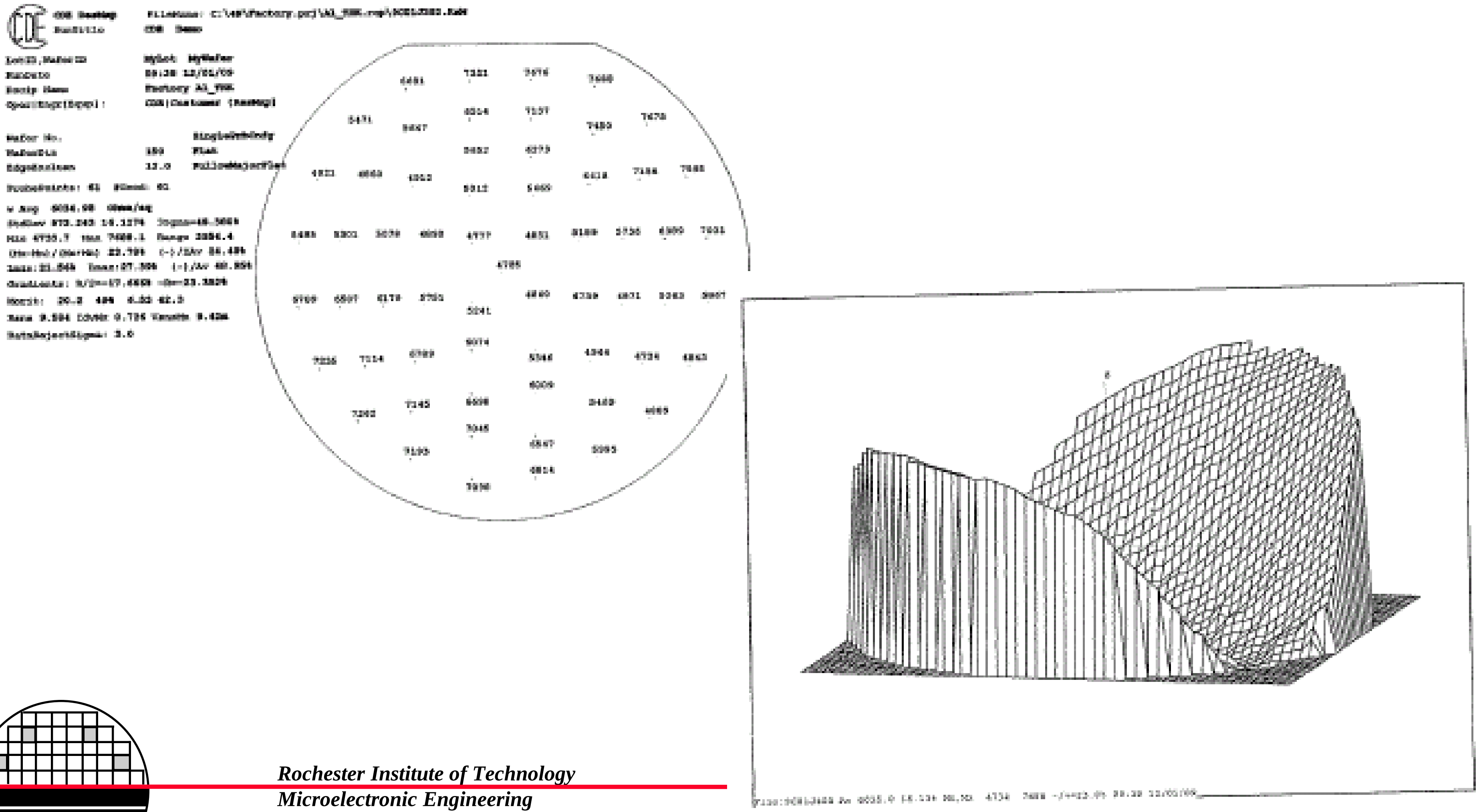
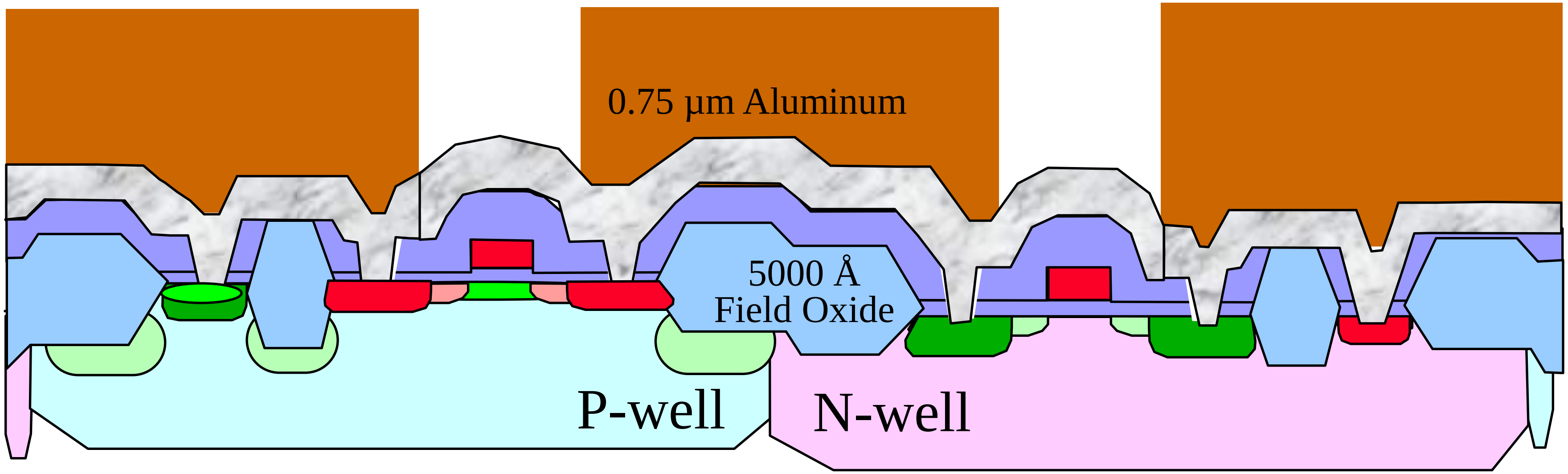
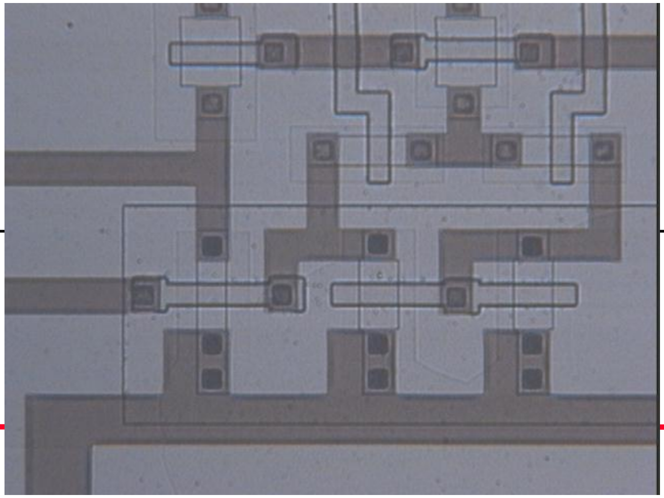


PHOTO 11 METAL





- **Coat (Recipe: COATMTL.RCP)**
  - 400RPM for 2 seconds
  - 2000RPM for 30 seconds
  - Thickness of 13127A
- **Exposure**
  - Energy: 140mJ/cm2
  - Focus: 0.24um
- **Develop (Recipe: DEVMTL.RCP)**
  - Dispense 7 seconds
  - Wait 68 seconds
  - Hard Bake 2 min.

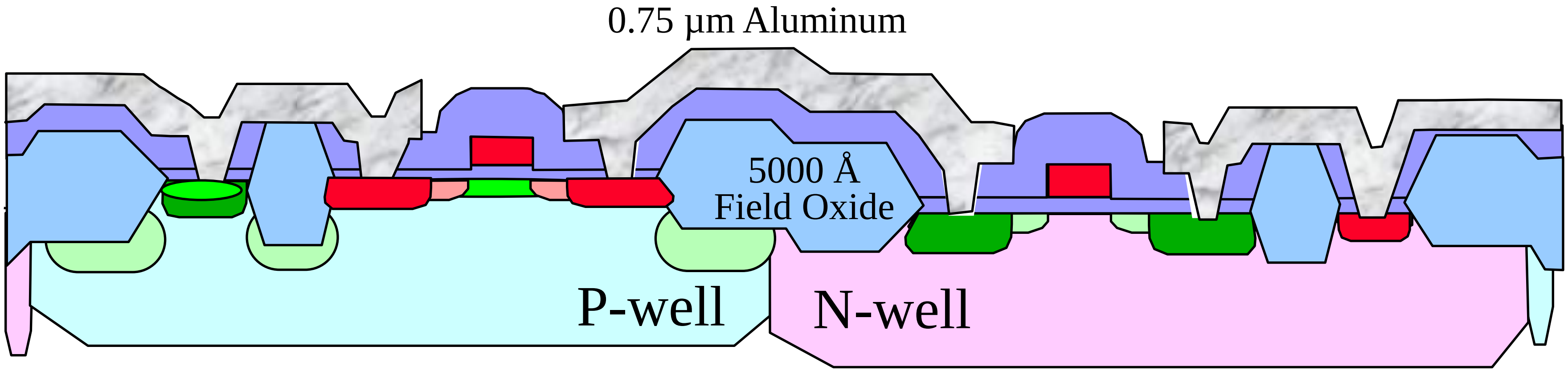
LAM4600 ANISOTROPIC ALUMINUM ETCH

Step	1	2	3	4	5
Pressure	**100**	**100**	**100**	**100**	**0**
RF Top (W)	**0**	**0**	**0**	**0**	**0**
RF Bottom	**0**	**250**	**125**	**125**	**0**
Gap (cm)	**3**	**3**	**3**	**3**	**5.3**
O2 111	**0**	**0**	**0**	**0**	**0**
N2 222	**13**	**13**	**20**	**25**	**25**
BCl 333	**50**	**50**	**25**	**25**	**0**
Cl2 444	**10**	**10**	**30**	**23**	**0**
Ar 555	**0**	**0**	**0**	**0**	**0**
CFORM666	**8**	**8**	**8**	**8**	**8**
Complete	**Stabl**	**Time**	**Time**	**Oetch**	**Time**
Time (s)	**15**	**8**	**230**	**10%**	**15**

Channel	**B**
Delay	**130**
Normalize	**10 s**
Norm Val	**5670**
Trigger	**105%**
Slope	**+**

Fuller, May 2010

ALUMINUM ETCH, ASH RESIST, SINTER



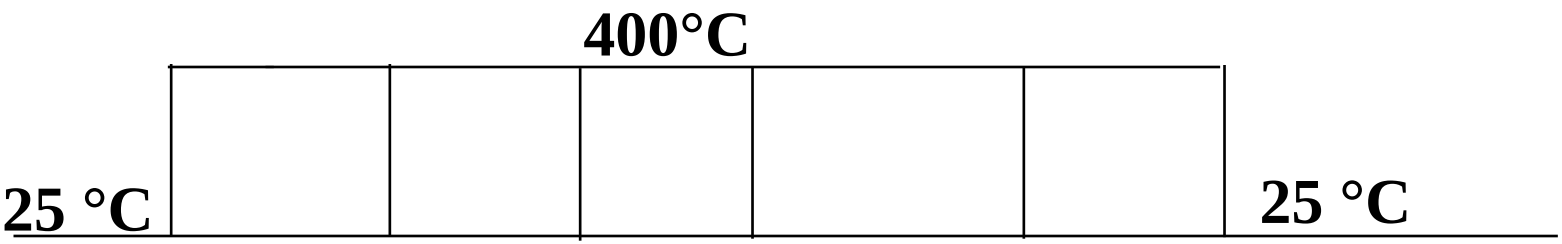
Bruce Furnace 02

Recipe 101: 400C, H_2/N_2, 30min

BRUCE FURNACE RECIPE 101 SINTER

SINTER Recipe #101

Verified:2-24-04



		Warm	**Push**	**Stabilize**	**Soak**	**Anneal**	**Pull**	
Interval	**0**	**1**	**2**	**3**	**4**	**5**	**6**	
	Any`	90	12	15	30	5	15	min
	0 lmp	10	10	10	5	10	5	lpm
	None	N2	N2/H2	N2/H2	N2/H2	N2	N2	

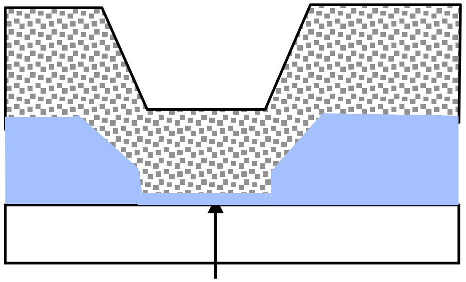
At the end of a run the furnace returns to Interval 0 which is set for boat out, 25 °C and no gas flow. The furnace waits in that state until someone aborts the current recipe or loads a new recipe.

Rochester Institute of Technology
Microelectronic Engineering

Sinter, Tube 2

SINTER

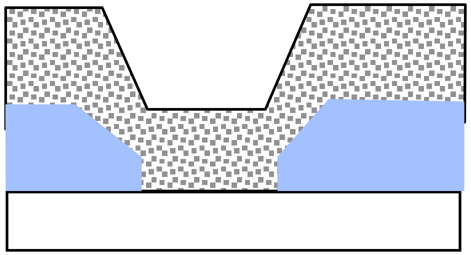
Before Sinter

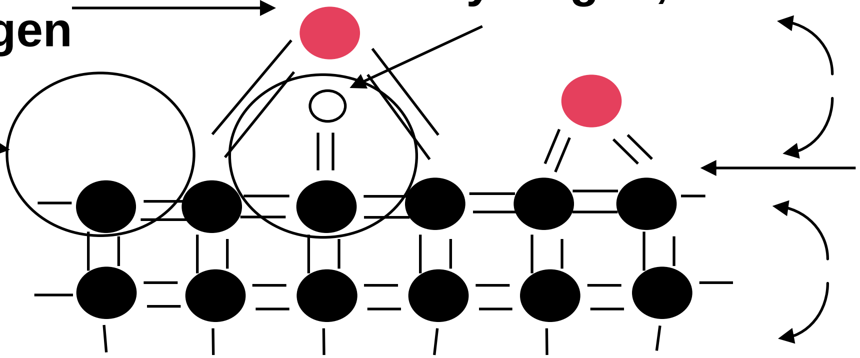


Native Oxide

Reduce Contact Resistance

After Sinter





Hydrogen, neutral region

Oxygen

+ charge region silicon atom that lost an electron

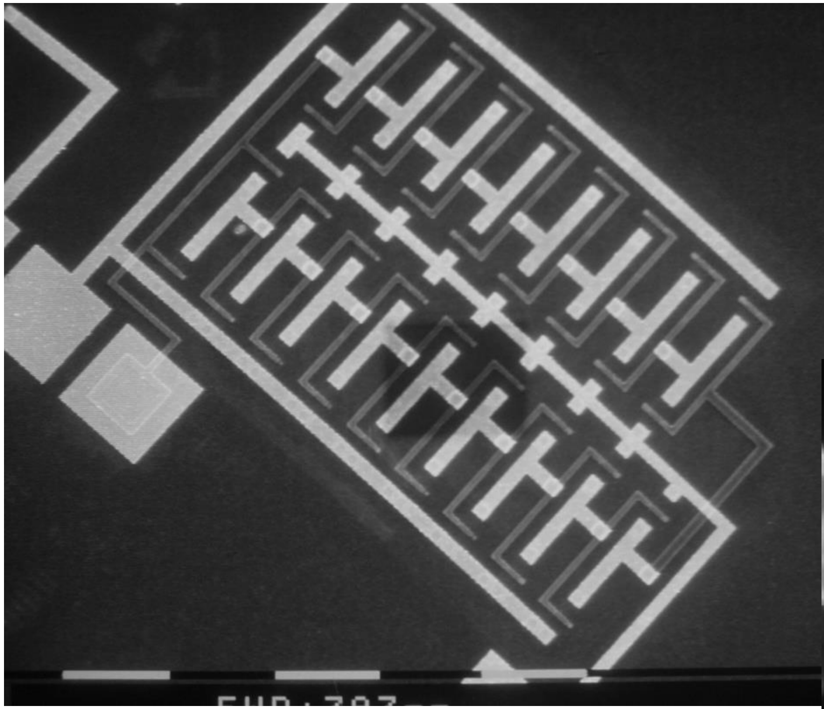
Silicon DiOxide

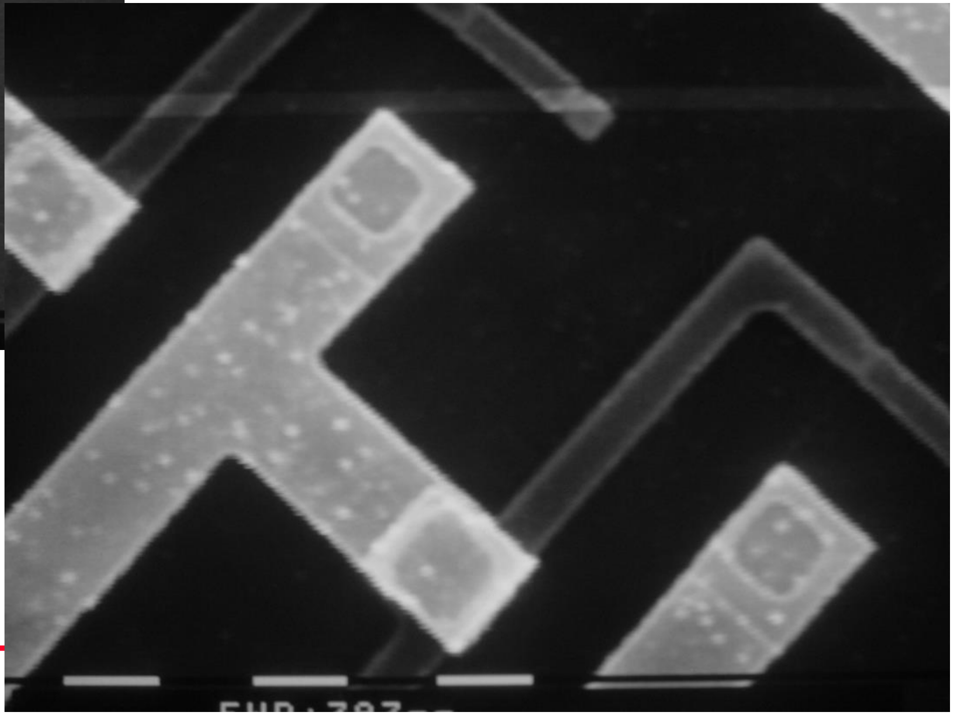
Interface

Silicon Crystal

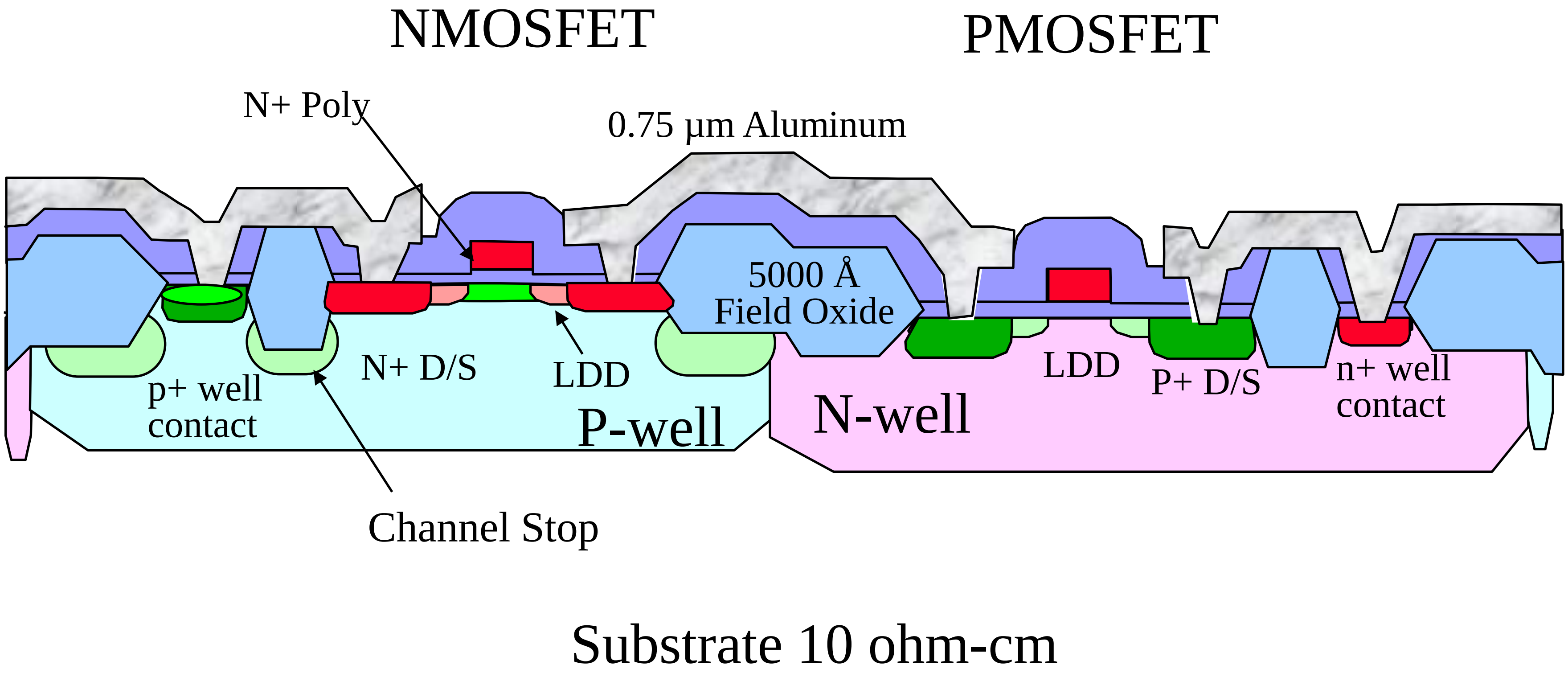
Reduce Surface States

TAKE SEM PICTURES OF RING OSCILLATOR





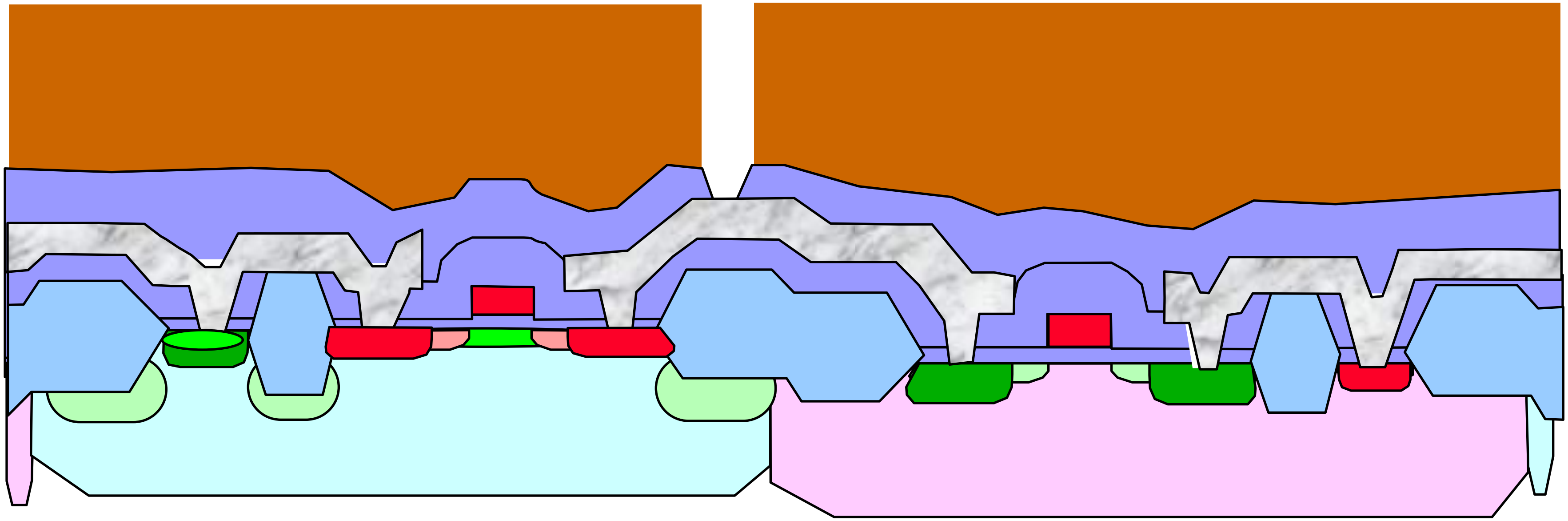
SUBμ CMOS SINGLE LAYER METAL



SEVERAL MORE STEPS FOR SECOND LAYER METAL

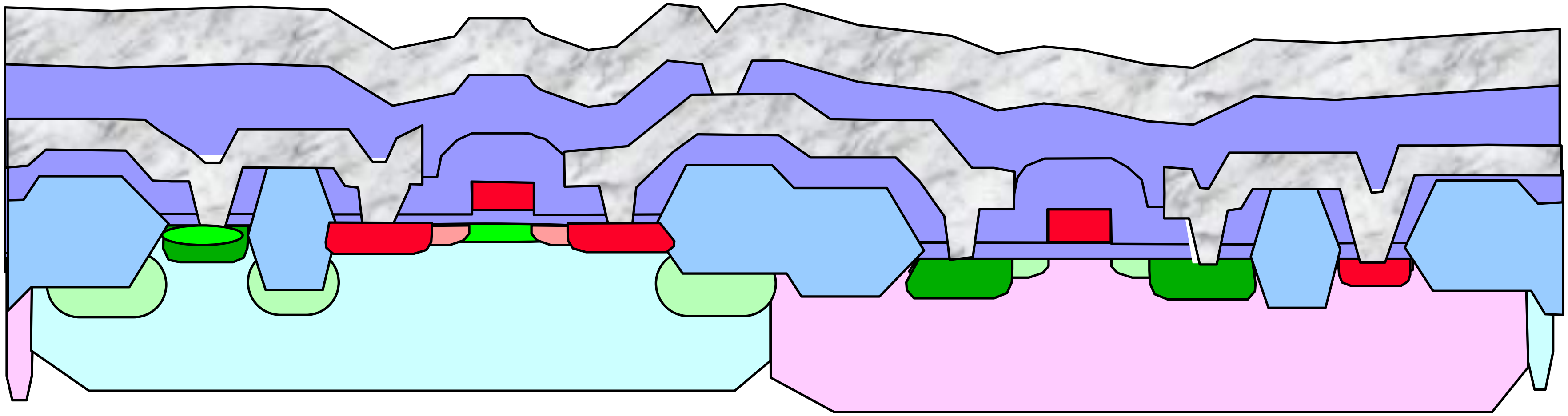
CV03 – TEOS Deposition (5000Å)
PH03 – Via One Photo
ET26 – Plasma Etch of Via
ET07 – Strip Resist
ME01 – Sputter Etch then Sputter Aluminum (7500Å)
PH03 – Metal Two Photo
ET15 – Plasma Etch Metal Two
ET17 – Strip Resist (Solvent plus Plasma)
Repeat for third layer of metal

ETCH VIAS



Plasma Etch
Using FACCC in Drytek Quad

SPUTTER 2ND LAYER METAL



Aluminum deposition using PE4400
Base pressure: 1E-6 Torr
Sputter Etch 15 min.
Power: 400W for Aluminum target
Sputter pressure: 5 mTorr
Argon flow: 40 sccm
Deposition time: 200 min
Dep rate: 37 Å/min

PE4400

SUMMARY - FOR SPUTTERING IN PE4400

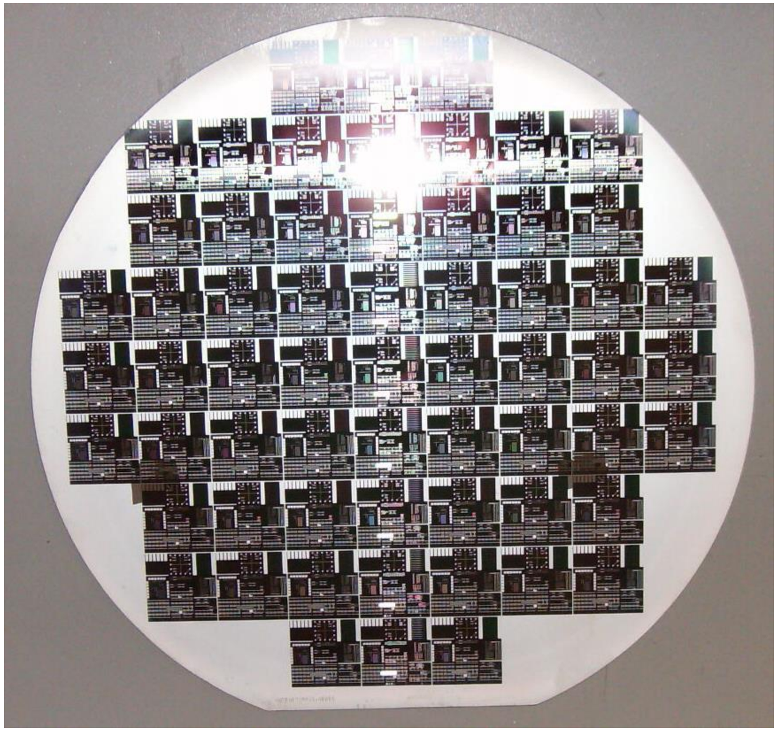
1. Smoother films can be deposited at lower powers.
2. Thinner films are smoother.
3. To quantify the roughness/smoothness the Veeco Wyco Optical Surface Profilometer is useful.
4. The deposition rate is lower at lower powers.
5. Deposition times become many hours for low power and film thickness approaching 1 micron.
6. Moving the wafers closer to the target increases sputter rate and surface roughness. (The height is as close as possible now “C”)
7. Rough films give problems for lithography and etching.
8. Surface roughness needs to be less than 10nm RMS for successful lithography and plasma etching.
9. Best conditions observed so far are, 300 watts, 5 mT, 40 sccm, to give a deposition rate of 37Å/min and surface roughness of ~11nm RMS for a film thickness of ~7500 Å. after 180 min sputter time.
10. Non uniformity is 22%. Wafers are thinner toward the flat.

VEECO WYCO NT1100 OPTICAL PROFILOMETER

Used to measure RMS surface roughness

ALUMINUM ETCH USING LAM4600


LAM4600



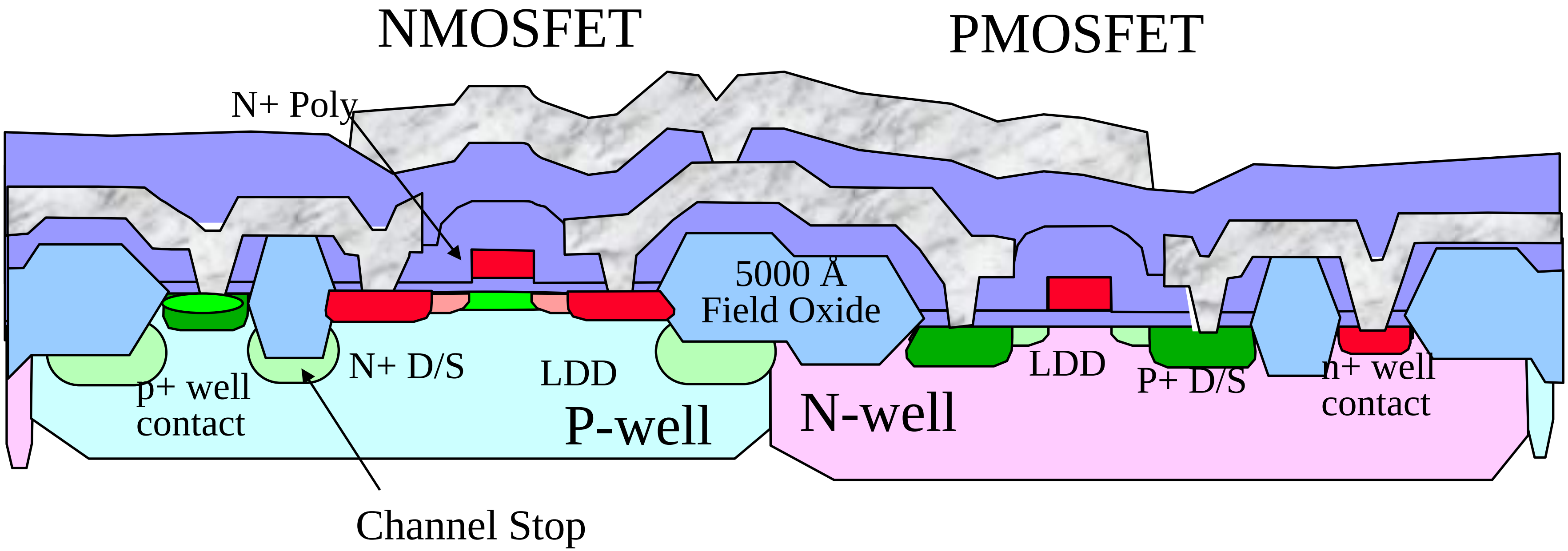
LAM4600 ANISOTROPIC ALUMINUM ETCH

Step	1	2	3	4	5
Pressure	**100**	**100**	**100**	**100**	**0**
RF Top (W)	**0**	**0**	**0**	**0**	**0**
RF Bottom	**0**	**250**	**125**	**125**	**0**
Gap (cm)	**3**	**3**	**3**	**3**	**5.3**
O2 111	**0**	**0**	**0**	**0**	**0**
N2 222	**13**	**13**	**20**	**25**	**25**
BCl 333	**50**	**50**	**25**	**25**	**0**
Cl2 444	**10**	**10**	**30**	**23**	**0**
Ar 555	**0**	**0**	**0**	**0**	**0**
CFORM666	**8**	**8**	**8**	**8**	**8**
Complete	**Stabl**	**Time**	**Time**	**Oetch**	**Time**
Time (s)	**15**	**8**	**230**	**10%**	**15**

Channel	**B**
Delay	**130**
Normalize	**10 s**
Norm Val	**5670**
Trigger	**105%**
Slope	**+**

Fuller, May 2010

FINAL DEVICE CROSSECTION



Substrate 10 ohm-cm

MESA WIPTRACKING SYSTEM

The process is long and complicated and will take many months to complete each lot. A computerized record keeping system is required to provide instructions and collect data. MESA (Manufacturing Execution System Application) from Camstar, Inc. runs on our AS/400 computer.

SUMMARY

The process described can be used down to ~1.0 µm gate length.

A new process for gate lengths down to 0.5 µm is being developed that involves shallow trench isolation, dual doped gates and other process advances.

Several lots have been processed and final process adjustments are being made.

REFERENCES

1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.
3. The Invention of LOCOS, Else Kooi, Institute of Electrical and Electronic Engineers, Inc., NY, NY 1991

HOMEWORK – RIT CMOS2014

1. Calculate the junction depth for both wells.
2. Estimate the well doping by calculating dose divided by junction depth.
3. Using the calculated well doping and a surface state density of 1E11 calculate the threshold voltage for nmos and pmos FETs.
4. Calculate the threshold adjust implant dose to give 0.75 and –0.75 volts for Vth.
5. Calculate the width of the space charge layer for the drain when it is reverse biased by 3 volts.