Introduction to Modeling MOSFETS in SPICE

Dr. Lynn Fuller
Electrical and Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
Dr. Fuller’s Webpage: http://people.rit.edu/lffeee
Email: Lynn.Fuller@rit.edu
Dept Webpage: http://www.microe.rit.edu
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INTRODUCTION

PSpice Lite 9.2 is one of the OrCAD family of products, from Cadence Design Systems, Inc., offering a complete suite of electronic design tools. It is free and includes limited versions of OrCAD Capture, for schematic capture, PSpice for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSpice Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSpice Users Guide.

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSpice Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components.
MOSFET Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 8, Level 49, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.

In general first generation models are recommended for MOSFETs with gate lengths of 10um or more. If not specified most SPICE MOSFET Models default to level=1 (Shichman and Hodges)
where ID is a dependent current source using the equations on the next page
\[
I_{D_{\text{sat}}} = \frac{\mu W \cdot Cox'}{2L} (V_g - V_t)^2
\]

Saturation Region

\[
I_D = \frac{\mu W \cdot Cox'}{L} (V_g - V_t - V_d/2)V_d
\]

Non Saturation Region

where \(\mu\), Cox’ and Vt are given in equations on the next pages.
**Introduction to Modeling MOSFETS in SPICE**

**SPICE LEVEL-1 EQUATIONS FOR UO, VTO AND COX’**

### Mobility:
\[
\mu = \mu_{\text{min}} + \frac{(\mu_{\text{max}} - \mu_{\text{min}})}{\{1 + (N/N_{\text{ref}})^\alpha}\}}
\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Arsenic</th>
<th>Phosphorous</th>
<th>Boron</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\mu_{\text{min}})</td>
<td>52.2</td>
<td>68.5</td>
<td>44.9</td>
</tr>
<tr>
<td>(\mu_{\text{max}})</td>
<td>1417</td>
<td>1414</td>
<td>470.5</td>
</tr>
<tr>
<td>(N_{\text{ref}})</td>
<td>9.68X10^16</td>
<td>9.20X10^16</td>
<td>2.23X10^17</td>
</tr>
<tr>
<td>(\alpha)</td>
<td>0.680</td>
<td>0.711</td>
<td>0.719</td>
</tr>
</tbody>
</table>

### Threshold Voltage:
\[
V_{\text{TO}} = \Phi_{\text{ms}} - q \frac{N_{\text{SS}}}{C_{\text{ox}}'} - 2[\Phi F] + \frac{2(q\varepsilon_o\varepsilon_{\text{rsi}} N_{\text{SUB}} [\Phi F])^{0.5}}{C_{\text{ox}}'}
\]

\[
[\Phi F] = \frac{(KT/q)}{\ln (N_{\text{SUB}}/n_i)} \quad \text{where } n_i = 1.45\times10^{10} \text{ and } KT/q = 0.026
\]

### Gate Capacitance
\[
C_{\text{ox}}' = \varepsilon_{\text{ro}} \frac{\varepsilon_o}{\text{TOX}} = 3.9 \frac{\varepsilon_o}{\text{TOX}}
\]

**where**
- \(\varepsilon_{\text{si}} = 11.7\) and \(\varepsilon_{\text{ox}} = 3.9\)
- \(\varepsilon_o = 8.85\times10^{-12} \text{ F/m or } 8.8\times10^{-14} \text{ F/cm}\)
- \(q = 1.6\times10^{-19}\)
MOBILITY MODEL

Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration (N). The values plotted are the results of the curve fitting measurements from several sources. The mobility curves can be generated using the equation below with the parameters shown:

\[
\mu(N) = \mu_{mi} + \frac{(\mu_{max} - \mu_{min})}{\left\{1 + (N/N_{ref})^\alpha\right\}}
\]

Parameter | Arsenic | Phosphorous | Boron |
---|---|---|---|
\(\mu_{min}\) | 52.2 | 68.5 | 44.9 |
\(\mu_{max}\) | 1417 | 1414 | 470.5 |
\(N_{ref}\) | 9.68X10^16 | 9.20X10^16 | 2.23X10^17 |
\(\alpha\) | 0.680 | 0.711 | 0.719 |

From Muller and Kamins, 3rd Ed., pg 33
LONG CHANNEL THRESHOLD VOLTAGE, $V_T$

Flat-band Voltage

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C'_{ox}} - \frac{1}{C'_{ox}} \int_0^{X_{ox}} \frac{X \rho(x)}{X_{ox}} dx$$

- p-type substrate (n-channel)
- n-type substrate (p-channel)

$$Q_{ss} = qN_{ss}$$

Bulk Potential:

$$\phi_p = -\frac{KT}{q} \ln \left( \frac{N_A}{n_i} \right)$$

$$\phi_n = +\frac{KT}{q} \ln \left( \frac{N_D}{n_i} \right)$$

Work Function:

$$\phi_{MS} = \phi_M - (X + Eg/2q + [\phi_p])$$

$$\phi_{MS} = \phi_M - (X + Eg/2q - [\phi_n])$$

Maximum Depletion Width:

$$W_{dmax} = \sqrt{\frac{4 \varepsilon_s \phi_p}{qN_A}}$$

$$W_{dmax} = \sqrt{\frac{4 \varepsilon_s \phi_n}{qN_D}}$$

Threshold Voltage:

- p-type substrate

$$V_T = V_{FB} + 2[\phi_p] + \frac{1}{C'_{ox}} \sqrt{2 \varepsilon_s q N_A (2[\phi_p] + V_{sb})}$$

- n-type substrate

$$V_T = V_{FB} - 2[\phi_n] - \frac{1}{C'_{ox}} \sqrt{2 \varepsilon_s q N_D (2[\phi_n] + V_{bs})}$$
Body Effect coefficient GAMMA or $\gamma$:

$$\gamma = \frac{1}{C_{ox}} \sqrt{2q\varepsilon_{Si}N_{sub}}$$

$$V_T = \Phi_{MS} - \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \gamma \sqrt{2\phi_F + V_{SB}}$$

where $\varepsilon_{Si} = 11.7$ and $\varepsilon_{ox} = 3.9$

$\varepsilon_0 = 8.8 \times 10^{-14} \text{F/cm}$

$q = 1.6 \times 10^{-19}$
The threshold voltage can be adjusted with an ion implant. If total implant dose is shallow (within \( W_{d_{\text{max}}} \)) then the change in \( V_t \) is:

\[
+/- \Delta V_t = q \text{ Dose}^*/Cox'
\]

where \( \text{Dose}^* \) is the dose that is added to the Si
\( Cox' = \frac{\epsilon_0 \epsilon_r}{X_{ox}} \)

Boron gives + shift
Phosphorous gives - shift

Maximum Depletion Width:
\[
W_{d_{\text{max}}} = \sqrt{\frac{4 \epsilon_s [\phi_p]}{qN}}
\]
**CHANNEL LENGTH MODULATION - LAMBDA**

Channel Length Modulation Parameter \( \lambda \)

\[ \lambda = \text{Slope/ Idsat} \]

\[ I_{D_{sat}} = \mu W \, Cox' \, (V_g - V_t)^2 \, (1 + \lambda V_d) \, \frac{2L}{2L} \]

**Saturation Region**

\[ I_D = \mu W \, Cox' \, (V_g - V_t - V_d/2) V_d \, (1 + \lambda V_d) \]

**Non Saturation Region**

NMOS Transistor

DC Model, \( \lambda \) is the channel length modulation parameter and is different for each channel length, \( L \). Typical value might be 0.02
TRANSISTOR PROPERTIES OR ATTRIBUTES

L = 2u
W = 8u
Ad = 8u x 10u = 80p
As = Ad = 80p
Pd = 8u + 10u + 8u + 10u = 36u
Ps = Pd = 36u
Nrs = 1
Nrd = 1
MOSFETS are four terminal devices (Drain, Gate, Source and Substrate). L and W are channel length and width in meters, Ad and As are area of drain and source in square meters. If not specified default values are used. (see next page) Perimeter of Drain and source (PD and PS) in meters is used to calculate drain and source side wall capacitance. If PD and PS are not given the default is zero. NRD and NRS are multiplied by the drain and source sheet resistance to give series resistance RD and RS. The default value for NRD and NRS is one.
### LTSPICE MOSFET ATTRIBUTE DEFAULT VALUES

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Unit</th>
<th>Default</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Default Length</td>
<td>m</td>
<td>defl</td>
<td>100u</td>
</tr>
<tr>
<td>W</td>
<td>Default Width</td>
<td>m</td>
<td>defw</td>
<td>100u</td>
</tr>
<tr>
<td>Ad</td>
<td>Default drain area</td>
<td>m2</td>
<td>defad</td>
<td>1000p</td>
</tr>
<tr>
<td>As</td>
<td>Default source area</td>
<td>m2</td>
<td>defas</td>
<td>1000p</td>
</tr>
<tr>
<td>Pd</td>
<td>Default drain perimeter</td>
<td>m</td>
<td>0</td>
<td>200u</td>
</tr>
<tr>
<td>Ps</td>
<td>Default source perimeter</td>
<td>m</td>
<td>0</td>
<td>200u</td>
</tr>
<tr>
<td>Nrd</td>
<td>Default drain squares</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Nrs</td>
<td>Default source squares</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Nrg</td>
<td>Default gate squares</td>
<td>-</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Nrb</td>
<td>Default bulk squares</td>
<td>-</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Lmin</td>
<td>Bin length lower limit</td>
<td>m</td>
<td>0</td>
<td>10u</td>
</tr>
<tr>
<td>Lmax</td>
<td>Bin length upper limit</td>
<td>m</td>
<td>0</td>
<td>20u</td>
</tr>
<tr>
<td>Wmin</td>
<td>Bin width lower limit</td>
<td>m</td>
<td>0</td>
<td>10u</td>
</tr>
<tr>
<td>Wmax</td>
<td>Bin width upper limit</td>
<td>m</td>
<td>0</td>
<td>20u</td>
</tr>
</tbody>
</table>
**MOSFET DEFINITION - LTSPICE**

For example:

* SPICE Input File
* MOSFET names start with M…. **M2** is the name for the MOSFET below and its drain, gate, source and substrate is connected to nodes 3,2,0,0 respectively. The model name is **RITSUBN7**.
* The parameters/attributes is everything after that.

**M2 3 2 0 0 RITSUBN7 L=2U W=16U ad=96e-12 as=96e-12 pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0**

**LTSPICE schematic showing .Include and .dc sweep commands. Properties dialog box to define L and W values. Note: attributes with no entry field **nrs** and **nrd** are typed in bottom box. Attribute Editor (CTRL R-click on the transistor) allows attributes with Vis.=X to be displayed on the schematic.**
MOSFET DEFINITION - PSPICE

For example:
* SPICE Input File
* MOSFET names start with M…. M2 is the name for the MOSFET below and its drain, gate, source
* and substrate is connected to nodes 3,2,0,0 respectively. The model name is RITSUBN7.
* The parameters/attributes is everything after that.

M2 3 2 0 0 RITSUBN7 L=2U W=16U ad=96e-12 as=96e-12 pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0

* In PSPICE the Attribute Editor (CTRL R-click on the transistor) allows attributes values to be set, new attribute columns to be created, and attributes can be selected to be displayed on the schematic..
In SPICE a transistor is defined by its name and associated properties or attributes and its model. MOSFET names start with M, attributes (L, W, Ad, As, etc.) are specified by the user and shown in the input file net list. Some attributes can be displayed on the schematic. The model is specified in a file in a given location or is defined in a library.
There are several ways to change the MOSFET SPICE model. A good way to do it is create a text file on your computer and put your models in that text file and save it in some folder. You can copy models from Dr. Fuller’s webpage to start your collection of models.

See: [http://people.rit.edu/lffeee/CMOS.htm](http://people.rit.edu/lffeee/CMOS.htm)

Example contents of that file is shown on the page below.

Next you change the model name for your transistor by right click on the model name shown in your schematic and typing the model name used in the model file. (for example: RITSUBN7)

Finally you place a SPICE directive on your schematic by clicking on the .op icon on the top banner and type the following command:

```
.include Drive:\path\folder\filename
```

For example

```
.include C:\SPICE\RIT_Models_For_LTSPICE.txt
```
SIMPLE AND ADVANCED SPICE MODELS

* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSN NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*

* From Electronics II EEEE482 FOR ~100nm Technology
.model EECMOSP PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*

* From Electronics II EEEE482 SIMPLE MODEL
.model EENMOS NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
*

* From Electronics II EEEE482 SIMPLE MODEL
.model EEPMOS PMOS (VTO=-0.4 KP=122E-6 GAMMA=0.2 PHI=.88)
CHANGING THE MOSFET SPICE MODEL IN PSpICE

Right click and select EDIT SPICE MODEL to type in underlined parameters

L and W shown on the schematic over ride default values

View output file to see this listing of spice model parameters including default values for L and W
CHANGING THE MOSFET SPICE MODEL IN PSPICE

In PSPICE models saved in a text file can be included as a configuration file in the Simulation Settings dialog box as shown above. Change the component model name to the model name in the text file.

"Add to Design" is selected.

In PSpice the models saved in a text file can be included as a configuration file in the Simulation Settings dialog box as shown above. Change the component model name to the model name in the text file.
COMPARISON OF MOSFET CHARACTERISTICS

The circuit shown can be used to see the transistor family of Ids-Vds curves, Ids-Vgs plot and Ids-Vgs (Ids on log scale) Subthreshold plot. We can investigate the effect of changing attributes, SPICE model and model parameters.

V1 is stepped to get family of curves or is swept to get Ids-Vgs and Sub-Vt plots

V2 is swept to get family of curves or is held constant to get Ids-Vgs plots
95 mosfet model parameters used by cadence PSPICE for Level 8 BSIM

31 mosfet model parameters used by cadence PSPICE for Level 1 Shichman and Hodges

View Output File
Three transistors all the same $L=2\mu m$ and $W=16\mu m$ but with different SPICE models. (SIMPLE, RIT SUB-MICRON and 100nm DEEP SUB-MICRON)
THREE DIFFERENT NMOS SPICE MODELS

* From Sub-Micron CMOS Manufacturing Classes in MicroE
  .MODEL RITSUBN7 NMOS (LEVEL=7
  +VERSION=3.1 CAPMOD=2 MOBMOD=1
  +TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
  +VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
  +NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
  +CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
  +CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)

* From Electronics II EEEE482 FOR ~100nm Technology Deep Sub-Micron
  .model EECMOSN NMOS (LEVEL=8
  +VERSION=3.1 CAPMOD=2 MOBMOD=1
  +TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
  +VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
  +NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
  +CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
  +CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)

* From Electronics II EEEE482 SIMPLE MODEL
  .model EENMOS NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
Model is EECMOSN
L=2u W=16u
Model not good. Current low and only good out to 3 volts.

Model is RITSUBN7
L=2u W=16u
Model good for RIT Sub-Micron MOSFETs

Model is EENMOS
L=2u W=16u
Model not good current too large
MEASURED MOSFET ID-VDS AND ID-VGS

\[ \text{Imax} = 9.5\text{mA} \]
LTSPICE OUTPUT FOR SUBTHRESHOLD ID-VGS

Model is EECMOSN
L=2u W=16u

Model not good MOSFET does not turn off, Vt too low

Model is RITSUBN7
L=2u W=16u

Model good

Model is EENMOS
L=2u W=16u

Model incorrect in subthreshold region. Subthreshold slope not possible.
DEEP SUB-MICRON TRANSISTOR MODELS

Model is EECMOSN
L=0.25u W=1.6u
Model good for Deep Sub-Micron MOSFETs

Model is RITSUBN7
L=0.25u W=1.6u
Model not good too much short channel effects

Model is EENMOS
L=0.25u W=1.6u
Model not good current too large does not show mobility degradation
Model is EECMOSN  
L=0.25u W=1.6u  
Model good for Deep Sub-Micron MOSFETs

Model is RITSUBN7  
L=0.25u W=1.6u  
Model not good too much DIBL

Model is EENMOS  
L=0.25u W=1.6u  
Model incorrect in subthreshold region
Deep sub-micron transistors show punch through at drain voltages over 3.3 volts. Which is correct.

Problem is worse in the sub-micron transistor because the channel is lighter doped.

Simple model is incorrect.
LTSPICE uses several different types of MOSFET models including simple, deep submicrometer, Silicon On Insulator (SOI), Vertical double diffused Power MOSFET. Level = 1 is the default if a model level is not specified.

Level
1  Shichman and Hodges
2  MOS2, Vladimirescu and Liu, UC Berkeley, October 1980
3  MOS3, a semi-emperical model, UC Berkeley
4  BSIM UC Berkeley, May 1985
5  BSIM2, UC Berkeley, October 1990
6  MOS6, UC Berkeley, March 1990
8  BSIM3V3.3.0, UC Berkeley 2005
9  BSIMSOI3.2, Silicon on Insulator (SOI), UC Berkeley 2004
14 BSIM4.6.1, UC Berkeley 2007

1st generation models

2nd generation models

3rd generation models

more…..
**SIMPLE AND ADVANCED SPICE MODEL**

* From Electronics II EEEE482 FOR ~100nm Technology
  .model EECEMOSN   NMOS (LEVEL=8
  +VERSION=3.1 CAPMOD=2 MOBMOD=1
  +TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
  +VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
  +NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
  +CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
  +CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
  *

* From Electronics II EEEE482 FOR ~100nm Technology
  .model EECEMOSP   PMOS (LEVEL=8
  +TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
  +VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
  +NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
  +CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
  +CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
  *

* From Electronics II EEEE482 SIMPLE MODEL
  .model EENMOS    NMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)
  *

* From Electronics II EEEE482 SIMPLE MODEL
  .model EEPMOS    PMOS (VTO=-0.4 KP=122E-6 GAMMA=0.2 PHI=.88)
CMOS INVERTER WITH LEVEL 1 SPICE MODEL

Level = 1 model
CMOS INVERTER WITH LEVEL 8 SPICE MODEL

VTC

Level = 8 model

.include c:\SPICE\RIT_Models_For_LTSPICE.txt

L=0.1u W=.7u
M2

EECMOSP

V1

Vin

1.5

V2

0

EECMOSN

L=0.1u W=.4u

M1

Vout

Level = 8 model
MEASURED VTC L=2um W=40um CMOS INVERTER

L=2u and W=40u
The Advanced Linear Devices ALD1103 is a dual NMOS and PMOS matched pair in a 14 pin package. The ALD 1101 is a dual NMOS matched pair and the ALD 1102 is a dual PMOS matched pair. The 1101/1102 are in an 8 pin package. One chip design for all three products.

8 of the donut shaped MOSFETs in parallel form one transistor.
ALD1103 LAYOUT

PIN CONFIGURATION

- DN1, GN1, SN1, V-, DP1, GP1, SP1
- DN2, GN2, SN2, V+, DP2, GP2, SP2

DB, PB, SB PACKAGE

4 V-
4 DP1
4 GP1
4 SP1

PMOS P2

ESD

4 DP2
4 GP2
4 SP2

Rochester Institute of Technology
Microelectronic Engineering
ELECTROSTATIC DISCHARGE - INPUT PAD

Simulation for Vpad sweep from -100 to +100 volts
Vin is between -1 and +6 Volts and I is through M1 and M2 if Vpad exceeds supply voltages

100mA
0 mA
-100mA

Rochester Institute of Technology
Microelectronic Engineering
ALD1103 MATCHED NMOS AND PMOS MOSFETS

.RMODEL RITALDN3 NMOS (LEVEL=3
+TPG=1 TOX=6.00E-8 LD=2.08E-6 WD=4.00E-7
+U0= 1215 VTO=0.73 THETA=0.222 RS=0.74 RD=0.74 DELTA=2.5
+NSUB=1.57E16 +XJ=1.3E-6 VMAX=4.38E6 ETA=0.913 KAPPA=0.074 NFS=3E11
+CGSO=5.99E-10 CGDO=5.99E-10 CGBO=4.31E-10 PB=0.90 XQC=0.4)

Using a LEVEL=3 model should give good results since L is long,
LEVEL 1 OR 2 will not work

From Dr. Fullers SPICE MOSFET Model Parameter Calculator. xls.
ALD1103 LEVEL=3 NMOS SPICE MODEL AND SIMULATION

This SPICE model gives good matching between measured and simulated curves.
Figure 4(a). Enlarged CD4007 Pin-Out Diagram
CD4007 DUAL COMPLEMENTARY PAIR + INVERTER
CD4007 DUAL COMPLEMENTARY PAIR + INVERTER

MODEL RIT4007N8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
CD4007 DUAL COMPLEMENTARY PAIR + INVERTER

```plaintext
.MODEL RIT4007N8 NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.34E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.6 U0= 600 WINT=2.0E7 LINT=1E-7
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+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
```

```
.V2 0 5 .001 V1 0 5 0.5

RIT4007N8
L=1u W=10u
```

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SUMMARY

All of these examples are for DC characteristics but similar results would be shown for examples that depend on internal capacitors and resistors such as a study of rise-time, fall time, gate delay, oscillators, multi-vibrators, etc.

In general the third generation SPICE models for MOSFETS give better results.

Level=1 models are not good for MOSFETS with L less than 10um.

Large MOSFETS, SUB-MICRON MOSFETS and DEEP SUB MICRON MOSFET models have been introduced.

Models should be verified by comparing measured ID-VDS, ID-VGS, and Ring Oscillator output with SPICE simulated results.
RING OSCILLATOR, \( t_d \), THEORY

Seven stage ring oscillator with two output buffers

\[ t_d = \frac{T}{2N} \]

- \( t_d \) = gate delay
- \( N \) = number of stages
- \( T \) = period of oscillation

\( T \) = period of oscillation

Vout

Buffer  Vout

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73 Stage Ring at 5V

\[ td = \frac{104.8\text{ns}}{2(73)} = 0.718 \text{ ns} \]
The parameters that effect the AC response of a MOSFET are the resistance and capacitance values.

- **RS, RS**: Source/Drain Series Resistance, ohms
- **RSH**: Sheet Resistance of Drain/Source, ohms
- **CGSO, CGDO**: Zero Bias Gate-Source/Drain Capacitance, F/m of width
- **CGBO**: Zero Bias Gate-Substrate Capacitance, F/m of length
- **CJ**: DS Bottom Junction Capacitance, F/m2
- **CJSW**: DS Side Wall Junction Capacitance, F/m of perimeter
- **MJ**: Junction Grading Coefficient, 0.5
- **MJSW**: Side Wall Grading Coefficient, 0.5

These are combined with the transistors
- **L, W**: Length and Width
- **AS, AD**: Area of the Source/Drain
- **PS, PD**: Perimeter of the Source/Drain
- **NRS, NRD**: Number of squares Contact to Channel
RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output
L/W=2/30 Buffered Output

Rochester Institute of Technology
Microelectronic Engineering
MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

nmosfet

pmosfet

73 Stage Ring Oscillator
FIND DIMENSIONS OF THE TRANSISTORS

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>2u</td>
<td>2u</td>
</tr>
<tr>
<td>W</td>
<td>12u</td>
<td>30u</td>
</tr>
<tr>
<td>AD</td>
<td>12ux12u=144p</td>
<td>12ux30u=360p</td>
</tr>
<tr>
<td>AS</td>
<td>12ux12u=144p</td>
<td>12ux30u=360p</td>
</tr>
<tr>
<td>PD</td>
<td>2x(12u+12u)=48u</td>
<td>2x(12u+30u)=84u</td>
</tr>
<tr>
<td>PS</td>
<td>2x(12u+12u)=48u</td>
<td>2x(12u+30u)=84u</td>
</tr>
<tr>
<td>NRS</td>
<td>1</td>
<td>0.3</td>
</tr>
<tr>
<td>NRD</td>
<td>1</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Use Ctrl Click on all NMOS on OrCad Schematic
Use Ctrl Click on all PMOS on OrCad Schematic
Then Enter Dimensions
Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts

\[ td = T / 2N = 5.5\text{nsec} / 2 / 3 \]

Measured \( td = 0.718 \text{nsec @ 5 V} \)

\[ td = 0.92 \text{nsec} \]
CONCLUSION

Since the measured and the simulated gate delays, $td$ are close to correct, then the SPICE model must be close to correct. The inverter gate delay depends on the values of the internal capacitors and resistances of the transistor.

Specifically:
$RS, RS, RSH$
$CGSO, CGDO, CGBO$
$CJ, CJSW$

These are combined with the transistors:
$L, W$  Length and Width
$AS, AD$  Area of the Source/Drain
$PS, PD$  Perimeter of the Source/Drain
$NRS, NRD$  Number of squares Contact to Channel
REFERENCES

7. **ICCAP Manual**, Hewlet Packard
8. **PSpice Users Guide.**
Do SPICE for one of the following:

1. Inverter gate delay is the time it takes for the output voltage to get to $\frac{1}{2}$ of the supply voltage. Use SPICE to get a value for gate delay for rising and falling output. Let $L=2\mu m$ and $W=40\mu m$ for both NMOS and PMOS transistors. State other assumptions. Compare these values to gate delay measured from a ring oscillator.

2. Do a SPICE simulation for the CMOS inverter shown on page 38 and compare to measured VTC and I vs Vin.