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MICROELECTRONIC ENGINEERING

SPICE Model Parameters for RIT MOSFET's

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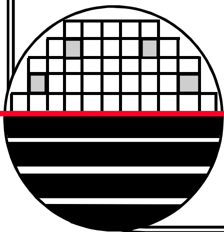

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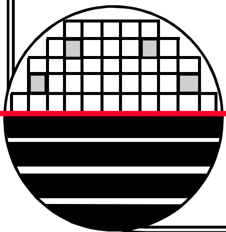

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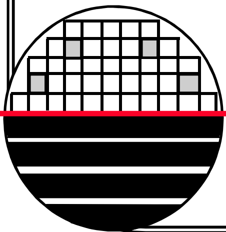
SIMULATION PROGRAM FOR INTEGRATED CIRCUIT ENGINEERING

Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 48, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.



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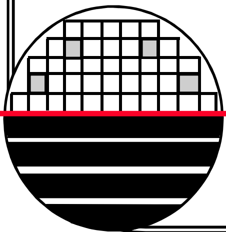
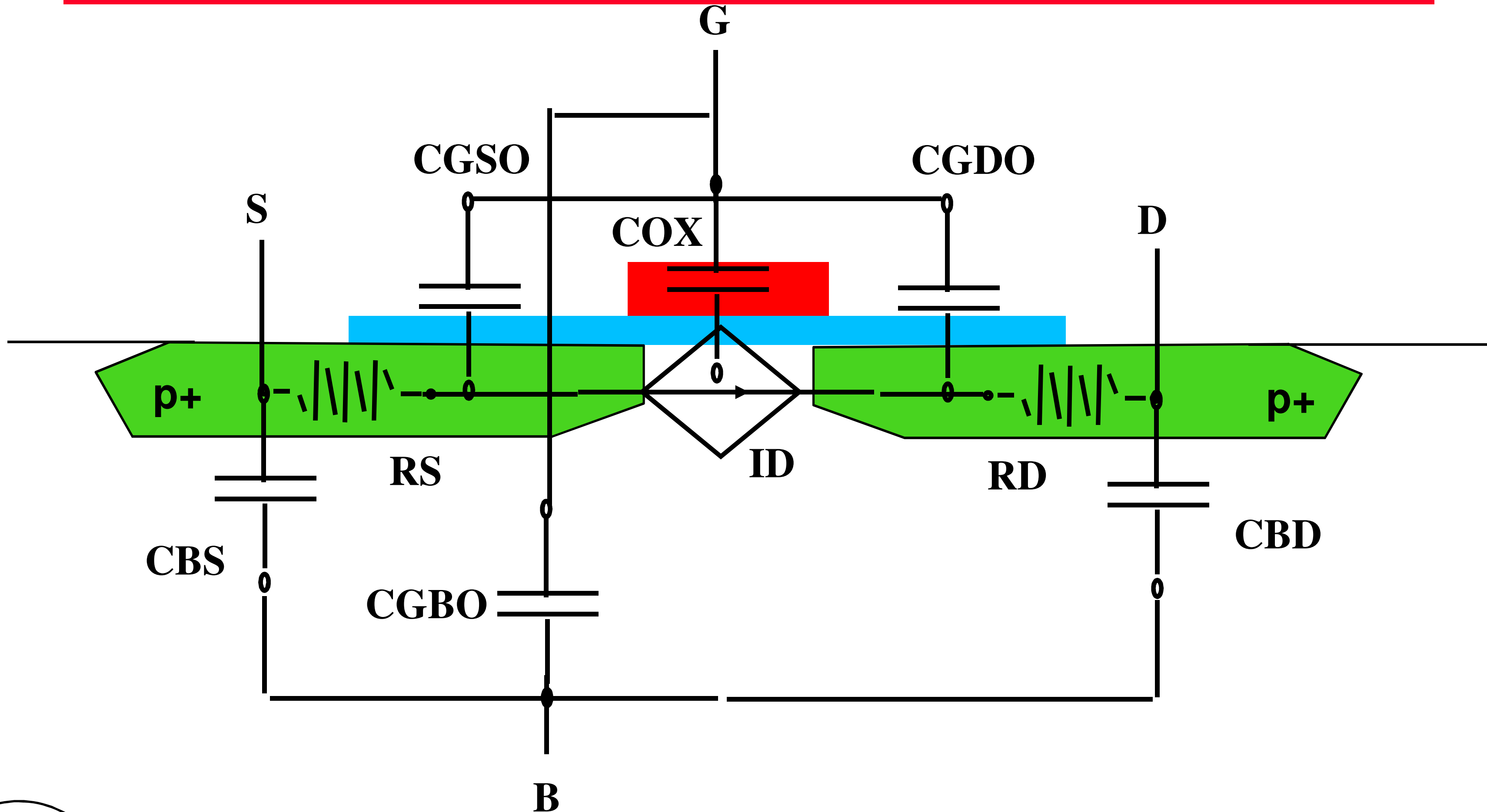
SPICE LEVEL-1 PARAMETERS FOR MOSFET's

If we understand the Level 1 model we can better understand the other models. The Level 1 model by Schichman and Hodges uses basic device physics equations for MOSFET threshold voltage and drain current in the saturation and non-saturation regions of operation. Mobility is assumed to be a function of total doping concentration only and a parameter called LAMBDA is used to model channel length modulation.



SPICE LEVEL-1 MOSFET MODEL



where ID is a dependent current source using the equations on the next page

SPICE LEVEL-1 EQUATIONS FOR UO, VT AND ID

Mobility:

$$\mu = \mu_{min} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^{\alpha}\}}$$

Parameter	Arsenic	Phosphorous	Boron
μ_{min}	52.2	68.5	44.9
μ_{max}	1417	1414	470.5
N_{ref}	9.68X10^16	9.20X10^16	2.23X10^17
α	0.680	0.711	0.719

Threshold Voltage:

+/-
nmos/pmos

$$VTO = \Phi ms - q\ NSS/Cox' +/- 2[\Phi F] +/-2\ (q\varepsilon s\ NSUB\ [\Phi F])^{0.5}/Cox'$$

$[\Phi F] = (KT/q)\ \ln(NSUB/ni)$ where ni = 1.45E10 and KT/q = 0.026
Absolute value

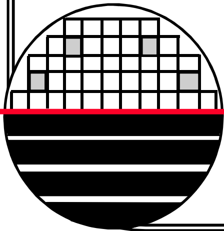
Drain Current:

Non-Saturation

$$I_D = \frac{\mu W\ Cox'}{L}(Vg-Vt-V_d/2)V_d\ (1+\lambda Vds)$$

Saturation

$$I_{Dsat} = \frac{\mu W\ Cox'}{2L}(Vg-Vt)^2\ (1+\lambda Vds)$$



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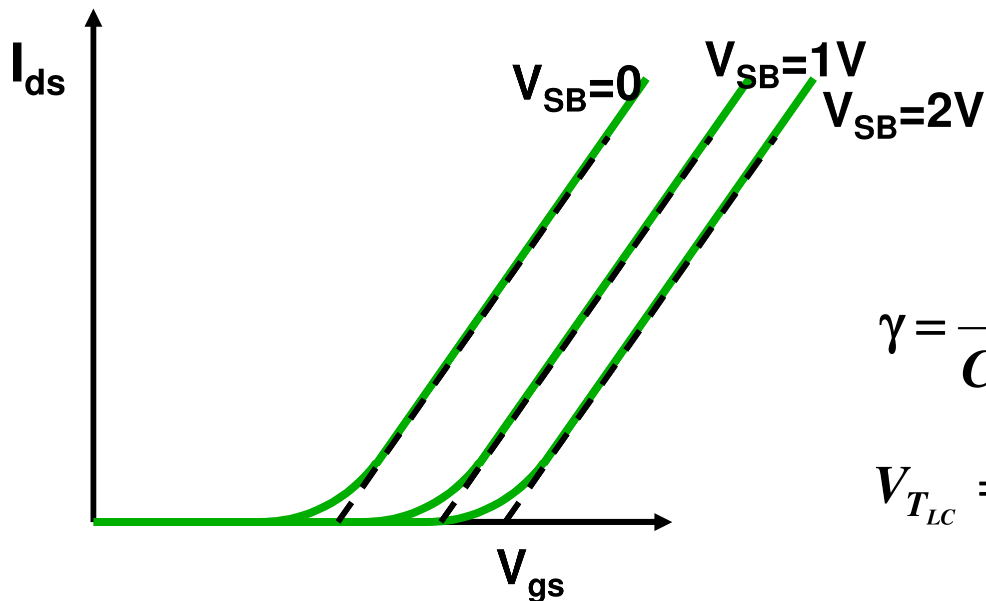
$Cox' = \varepsilon r \varepsilon o/TOX = 3.9\varepsilon o/TOX$

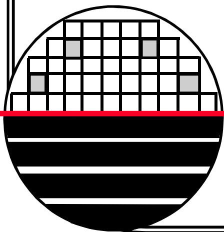
BACK-BIASING EFFECTS – EXTRACT GAMMA

Body Effect coefficient GAMMA or γ :



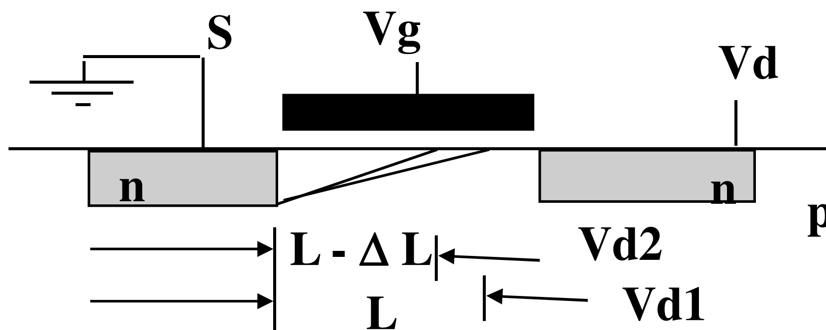
$$\gamma = \frac{1}{C'_{ox}} \sqrt{2q\varepsilon_{Si} N_A}$$

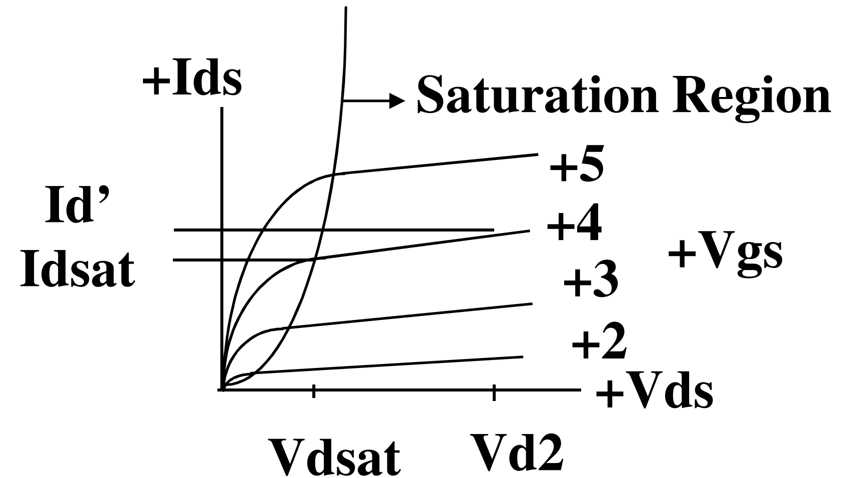
$$V_{T_{LC}} = \Phi_{MS} - \frac{Qss}{C'_{ox}} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}}$$



CHANNEL LENGTH MODULATION

Channel Length Modulation Parameter λ
λ = Slope/ Idsat

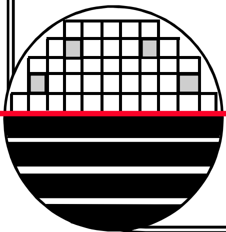




$$I_{Dsat} = \frac{\mu W\, Cox'}{2L} (Vg-Vt)^2 (1+ \lambda Vds)$$

NMOS Transistor in Saturation Region DC Model, λ is the channel length modulation parameter and is different for each channel length, L. Typical value might be 0.02.

λ = LAMBDA in SPICE models



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LAMBDA VERSUS CHANNEL LENGTH

µA					LAMBDA	
UNIT	SLOPE	IDSAT	W	L	PMOS	NMOS
205	4.9	6.8	32	2	0.144118	0.132308
71	2	7.1	32	4	0.056338	0.026761
56	1.8	7.3	32	6	0.049315	0.011429
34	1.2	7.5	32	8	0.032	0.013889
21	1	7	32	16	0.028571	0.005556
8.8	0.8	7.6	32	32	0.021053	0.004196
415	4.3	6.5	32	2	0.132308	
137	0.95	7.1	32	4	0.026761	
91	0.4	7	32	6	0.011429	
137	0.5	7.2	32	8	0.013889	
27	0.2	7.2	32	16	0.005556	
15	0.15	7.15	32	32	0.004196	

LAMBDA

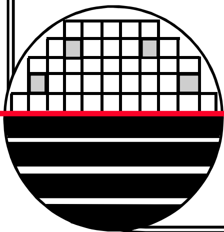
LAMBDA (y-axis: 0 to 0.16)

LENGTH (x-axis: 2, 4, 6, 8, 16, 32)

PMOS

NMOS

Need different model for each different length transistor

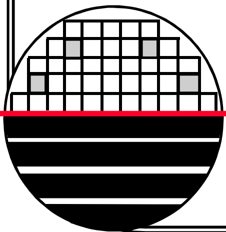


SPICE LEVEL-1 PARAMETERS

SPICE LEVEL 1 MODEL FOR MOS TRANSISTORS:

1. LEVEL=1
2. VTO
3. KP
4. GAMMA
5. PHI
6. LAMBDA
7. RD
8. RS
9. CBD
10. CBS
11. IS
12. PB
13. CGSO
14. CGDO
15. CGBO
16. RSH
17. CJ
18. MJ
19. CJSW
20. MJSW
21. JS
22. TOX
23. NSUB
24. NSS
25. NFS
26. TPG
27. XJ
28. LD
29. UO

30.-41. PARAMETERS FOR SHORT CHANNEL AND NOISE (Use Defaults)



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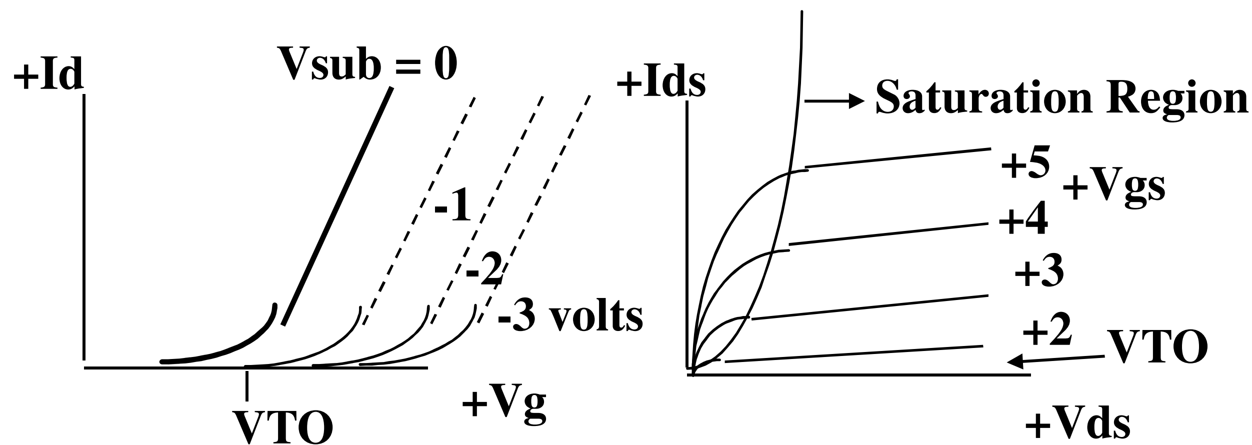
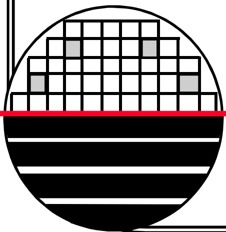
SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

1. LEVEL=1 Schichman-Hodges Model
2. VTO zero bias threshold voltage (Do not use, let SPICE calculate from Nsub,TOX unless an VT adjust ion implant is used to set VTO at some value)



3. KP transconductance parameter (Do not use, let SPICE calculate from UO, COX')

$$KP = UO\ COX' = UO\ \varepsilon_r \varepsilon_o / TOX$$



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SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

4. GAMMA bulk threshold parameter (Do not use, let SPICE calculate from UO,COX')

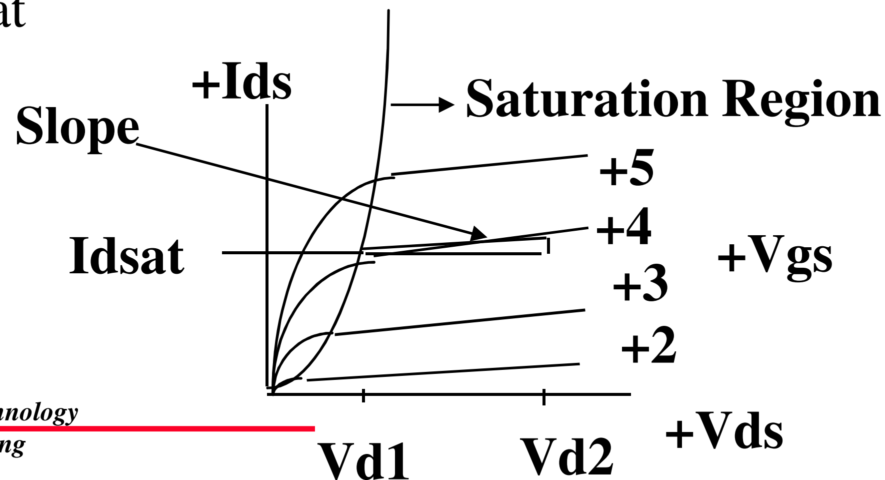
   GAMMA = [2q εrsiεo NSUB/C'ox^2]$^{1/2}$ where εsiεo = (11.7)(8.85E-12) and q = 1.6E-19

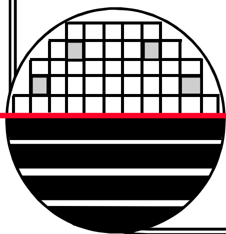
5. PHI is the semiconductor potential, Intrinsic Level to Fermi Level difference in Volts (Do not use, let SPICE calculate from NSUB)

   PHI = 2[ΦF] = 2 (KT/q) ln (NSUB/ni) where KT/q = 0.026 ni = 1.45E10

6. LAMBDA is the channel length modulation parameter, Slope in saturation region divided by Idsat

λ = Slope/ Idsat





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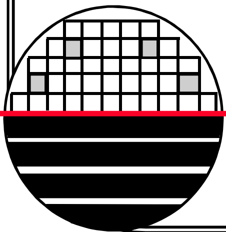
SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

7. RD the series drain resistance can either be given as a resistance value or through RSH the drain/source sheet resistance and the number of squares NRS. NRS: Is from the device layout. RSH: Is measured by four point probe or Van Der Pauw structures
(Do not use, let SPICE calculate from sheet resistance, RSH, and number of squares in drain, NRD)
8. RS is the series source resistance can either be given as a resistance value or through RSH the drain/source sheet resistance and the number of squares NRS. NRS: Is from the device layout. RSH: Is measured by four point probe or Van Der Pauw structures
(Do not use, let SPICE calculate from sheet resistance, RSH, and number of squares in source, NRS)



SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

9. CBD zero bias bulk to drain junction capacitance (Do not use, let SPICE calculate from CJ and CJSW and AD (Area of Drain) and PD (Perimeter of Drain)

   CBD = CJ AD + CJSW PD

10. CBS zero bias bulk to source junction capacitance (Do not use, let SPICE calculate from CJ and CJSW and AS (Area of Source) and PD (Perimeter of Source)

    CBS = CJ AS + CJSW PS

11. IS is the bulk junction saturation current in the ideal diode equation.

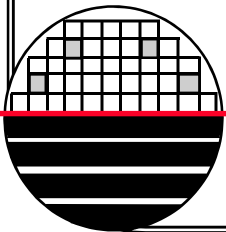
    $I = IS\ (\exp^{qVA/KT} - 1)$

(Do not use, let SPICE calculate from JS and AD (Area of Drain) and AS (Area of Source)

IS = JS (AD + AS)

12. PB is the junction built in voltage

    PB = (KT/q)ln (NSUB/ni) + 0.56



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SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

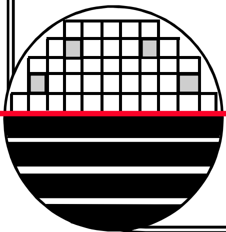
$$Cox' = \varepsilon r \varepsilon o/TOX = 3.9 \varepsilon o/TOX$$

13. CGSO is the gate-to-source overlap capacitance (per meter channel width)
    CGSO = Cox' (mask overlap in L direction + LD)   F/m

14. CGDO is the gate-to-drain overlap capacitance (per meter channel width)
    CGDO = Cox' (mask overlap in L direction + LD)   F/m

15. CGBO is the gate-to-bulk overlap capacitance (per meter channel length)
    CGBO = C_{field_oxide} * mask overlap in W direction   F/m

$$C_{field_oxide} = \varepsilon r \varepsilon o/XFieldOX$$



SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

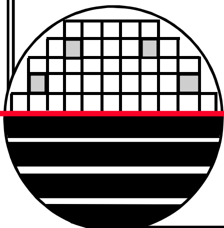
16. RSH is the drain and source diffusion sheet resistance. Measured from four point probe or Van Der Pauw structures.
17. CJ is the zero bias bulk junction bottom capacitance per square meter of junction area. $CJ = \varepsilon r \varepsilon o / W$ where W is width of space charge layer.

$$CJ = \varepsilon r \varepsilon o \, [2 \varepsilon r \varepsilon o \, (\Psi o - VA)/qNsub]^{-m} \qquad F/m2$$

where $\Psi o = PB = (KT/q) \ln (NSUB/ni) + 0.56$
m = junction grading coefficient = 0.5

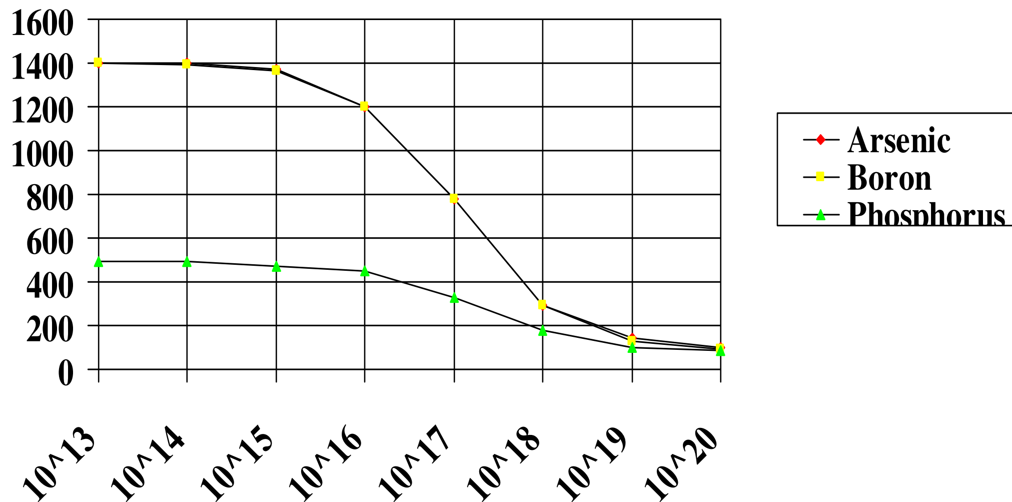
18. MJ is the junction grading coefficient = 0.5
19. CJSW is the zero bias bulk junction sidewall capacitance per meter of junction perimeter. CJSW = CJ XJ
20. MJSW is the junction grading coefficient = 0.5
21. JS is the bulk junction saturation current density in Amperes per square meter

$$JS = q\, ni^2 \,(Dp/NdLp + Dn/ NaLn) \text{ where } D = (KT/q)\, \mu \text{ and } L = (D\tau)^{0.5}$$



SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

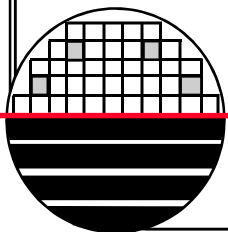
22. TOX is the gate oxide thickness, measured by ellipsometer or reflectance spectroscopy (Nanospec).
23. NSUB the substrate doping is given by the wafer manufacturer or measured by four point probe technique. In both cases NSUB is given indirectly by the resistivity, Rho. Rho = $1/(q\mu(N)N)$ where q = 1.6E-19 coul, N is the substrate doping NSUB, $\mu(N)$ is the mobility, a function of N.



Emperical Equation:

$$\mu = \mu min + \frac{\mu max - \mu min}{\{1+(N/Nref)^{\alpha}\}}$$

	Electrons	Holes
μmin	92	47.7
μmax	1360	495
Nref	1.3E17	6.3E16
α	0.91	0.76



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SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

24. NSS: The surface state density is a parameter used in the calculation of the zero-bias threshold voltage (ie. Vsource = Vsubstrate), VT0 is obtained from transistor curves.

$$VTO = \Phi ms - q\ NSS/Cox' - 2\ \Phi F - 2\ (q\varepsilon s\ NSUB\ \Phi F)^{\wedge}0.5/Cox'$$

$\Phi F = (KT/q)\ \ln (NSUB/ni)$ where ni = 1.45E10 and KT/q = 0.026

$\Phi ms = \Phi m - (X + Eg/2 - \Phi F)$ where Φm=gate work function

X = 4.15 eV, Eg = 1.12 eV

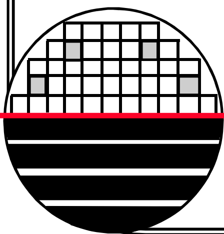
$\varepsilon s = \varepsilon r \varepsilon o = 11.7 \varepsilon o$

Since everything is known

$Cox' = \varepsilon r \varepsilon o/TOX = 3.9 \varepsilon o/TOX$

in equations above, NSS can be calculated

25. NFS is the fast surface state density, usually left at zero.



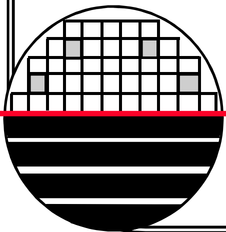
SPICE LEVEL-1 PARAMETERS FOR MOSFET (cont.)

26. TPG is the type of gate. for aluminum TPG=0, for n+ poly TPG = 1, for p+ poly TPG= -1
27. XJ metallurgical junction depth, measured by groove and stain techniques.
28. LD lateral diffusion distance, inferred from process knowledge
29. UO is the surface mobility taken as 1/2 the bulk mobility or extracted to give correct Id value on measured Id vs Vds characteristics

in the saturation region. For best results make measurements on a transistor with large channel length so that λ is small and the lateral diffusion can be neglected.

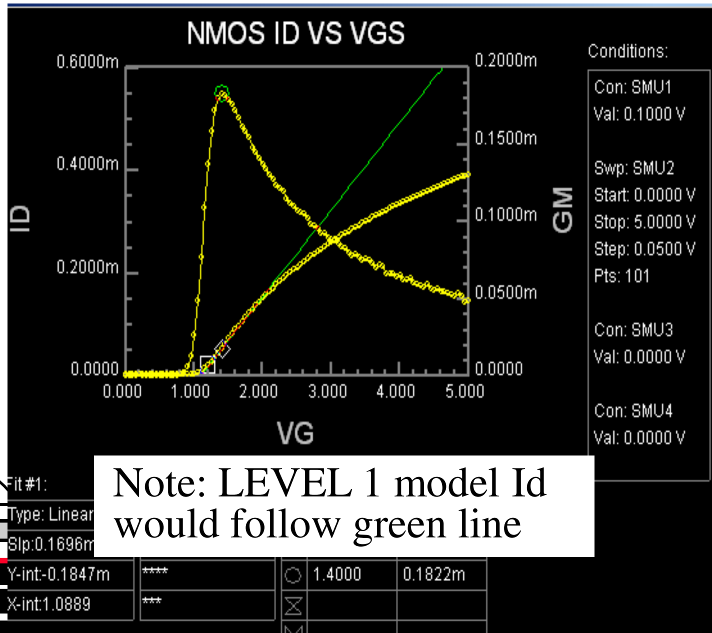
$$I_{Dsat} = \frac{\mu W\, Cox'}{2L} (Vg-Vt)^2 (1+ \lambda Vds)$$

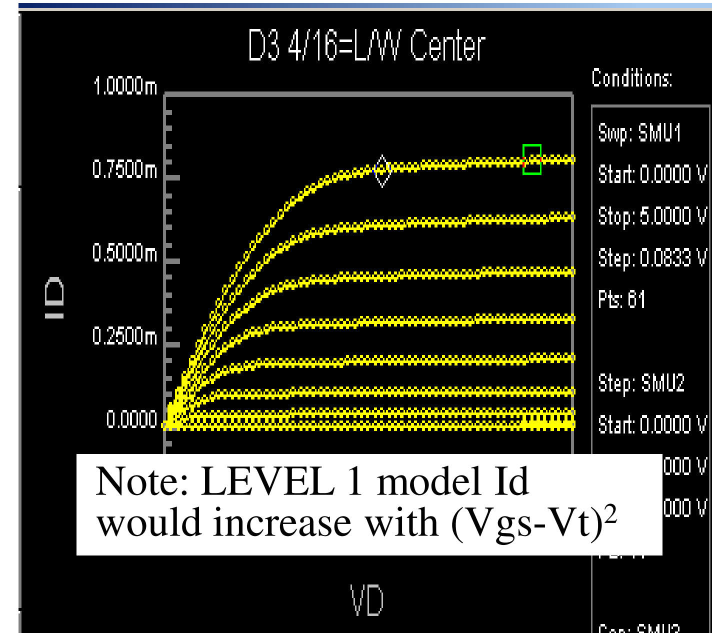
30\. - 41. Parameters associated with short channel devices and noise in MOSFETs



SPICE 2ND GENERATION MODELS AND PARAMETERS

2ND generation MOSFET models improve over the Level 1 models because they model sub-threshold current, mobility as a function of vertical and lateral electric field strength, threshold voltage reduction as a function drain voltage or drain induced barrier lowering (DIBL). This model has separate equations for drain current for different regions of operation. The discontinuity at the transition points can make problems in program convergence during circuit simulation.





TERADA-MUTA METHOD FOR EXTRACTING Leff and Rds

Terada-Muta Method for Leff and Rds

In the linear region (V_D is small):

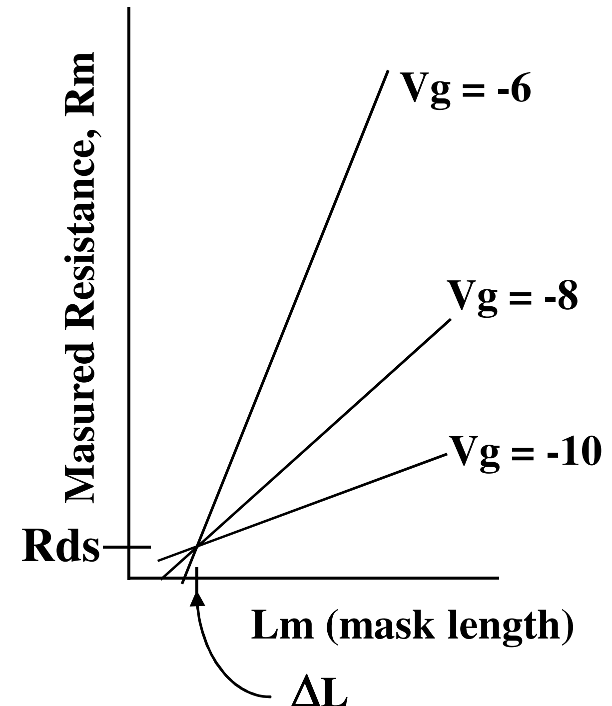
$$I_D = \frac{\mu W\, Cox'}{Leff} (Vg - Vt - V_d/2)\ V_D$$

$$I_D = 1/R_m\ V_D$$

Leff = Lm - ΔL

where ΔL is correction due to processing

Lm is the mask length



$Rm = V_D/I_D$ = measured resistance

$= Lm/ (\mu W\, Cox' (Vg-Vt)) - \Delta L/ \mu W\, Cox' (Vg-Vt)$

so measure Rm for different channel length transistors and plot Rm vs Lm where Rm = intersect find value for ΔL and Rds

Then Leff can be calculated for each different length transistor from Leff = Lm - ΔL

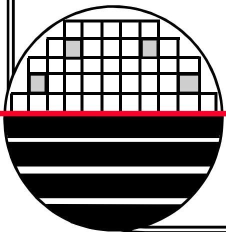
2nd GENERATION MODELS EQUATIONS FOR MOBILITY

The mobility used in the equations for Ids is the effective mobility , Ueff. Starting with UO from level 1, Ueff is found. The parameter THETA is introduced to model mobility degradation due to high vertical electric fields (larger values of Vgs - VTO).

$$Ueff^* = \frac{UO}{(1+THETA\,(Vgs-VTO))}$$

Measure Ids for a wide transistor with low value of Vds and large value of Vgs and using Leff from Terata-Muta method and LAMBDA from level 1, calculate THETA from these two equations.

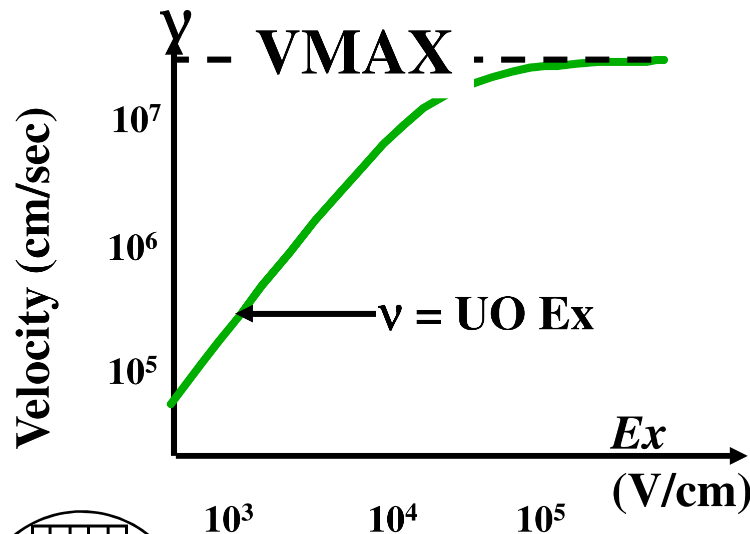
$$I_{dsat} = \frac{Ueff\ W\ Cox'}{2Leff}(Vg-Vt)^2\,(1+\lambda Vds)$$



Warning: Curvature also due to R_{DS} so Vds is (Vapplied – Rds*Idsat) requires an iterative approach to find THETA

2ND GENERATION EQUATIONS FOR MOBILITY (cont.)

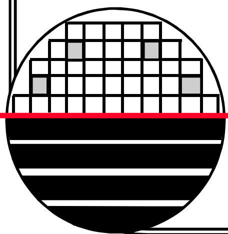
The parameter VMAX is introduced to model the decrease in mobility at higher Vds due to velocity saturation. Ideally, carrier velocity is directly proportional to the applied electric field. However, at very high lateral electric fields, Ex, this relationship ceases to be accurate - the carrier velocity saturates at VMAX.



$$\text{Ueff} = \frac{\text{UO}}{\left(1+\text{THETA}\,(\text{Vgs-VTO})\right)\left(1 + \text{UO}\,\dfrac{\text{vde}}{\text{VMAX Leff}}\right)}$$

Where, Vde = min (Vds, Vdsat)

Note: other models (equations) for mobility exist and use parameters such as UCRIT, UEXP, ULTRA, ECRIT, ESAT



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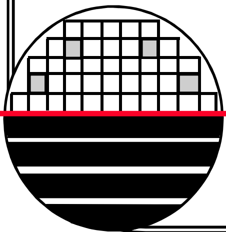
2ND GENERATION MODEL EUATIONS FOR THRESHOLD VOLTAGE

The parameter ETA is used to describe DIBL (Drain Induced Barrier Lowering) resulting in a modification to the LEVEL 1 equation for threshold voltage.

$$\mathbf{VTO = \Phi ms - \phi_{ETA} - q\ NSS/Cox' - 2\ \Phi F - 2\ (q\varepsilon s\ NSUB\ \Phi F)^{0.5}/Cox'}$$

$$\phi_{ETA} = \frac{(-\ 8.14E\text{-}22)*ETA}{Cox'Leff^{\ 3}}\ Vds$$



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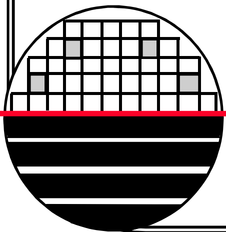
2ND GENERATION EQUATIONS FOR NARROW WIDTH

DELTA is introduced to model narrow channel effects on threshold voltage. The parameter WD (channel width reduction from drawn value) is used to calculate the effective channel width. DELTA is used in the calculation of threshold voltage.

$$DELTA = \frac{q\ NSUB\ Xds^2}{\varepsilon o\ \varepsilon si\ 2\ PHI}$$

Note: a dimensionless number typically ~3

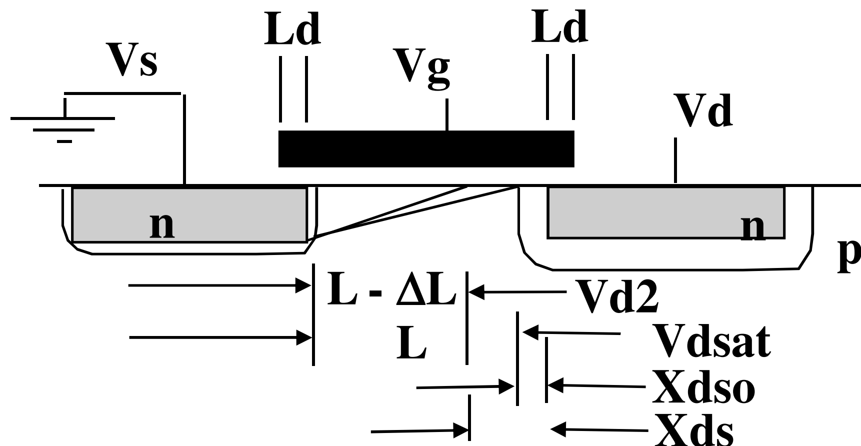


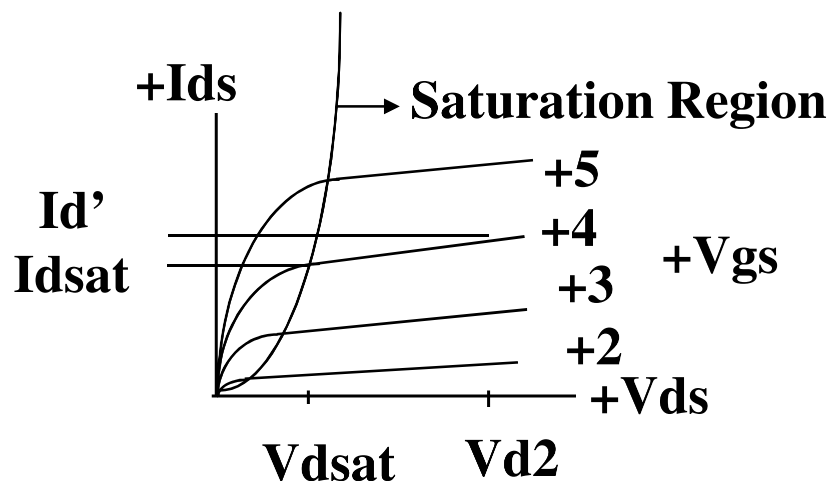
2ND GENERATION EQUATIONS FOR CHANNEL LENGTH MODULATION

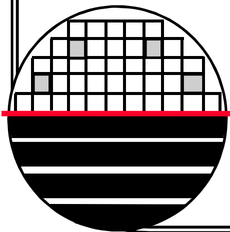
KAPPA is channel length modulation parameter.

KAPPA is calculated = [(qNsub/(2εoεr))((1-Idsat/Id')(L-2LD-Xdso-Xds))^2)/(Vd2-Vdsat)]^0.5

Measure Id’ at large Vds, and Idsat at Vdsat,
Kappa has units of 1/V typical value ~0.1







PARAMETERS FOR SPICE LEVEL 3

SPICE LEVEL 3 MODEL PARAMETERS FOR MOS TRANSISTORS:

Control	Level=3	
Process	TPG=1	1 if gate is doped opposite of channel, -1 if not
Process	TOX	Gate Oxide Thickness
Process	NSUB	Channel doping concentration
Process	XJ	Drain/Source Junction Depth
Process	PB	PB is the junction built in voltage
W and L	LD	Drain/Source Lateral Diffusion
W and L	WD	Decrease in Width from Drawn Value
DC	UO	Zero Bias Low Field Mobility
DC	VTO	Measured threshold voltage, long wide devices
DC	THETA	Gate Field Induced Mobility Reduction
DC	DELTA	Narrow Channel Effect on the Threshold Voltage
DC	VMAX	Maximum Carrier Velocity
DC	ETA	DIBL Coefficient
DC	KAPPA	Channel Length Modulation Effect on Ids
DC	NFS	Surface State Density

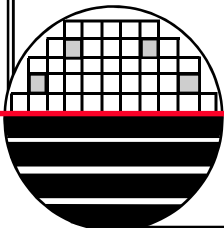
PARAMETERS FOR SPICE LEVEL 3

Diode & Resistor	RS	Source Series Resistance
Diode & Resistor	RD	Drain Series Resistance
AC	CGDO	Zero Bias Gate-Source Capacitance
AC	CGSO	Zero Bias Gate-Drain Capacitance
AC	CGBO	Zero Bias Gate-Substrate Capacitance
AC	CJ	

Temp
- more

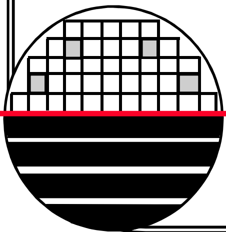
Noise
- more

Tunneling
-more



BSIM3 MODELS

Berkeley SPICE third generation SPICE models are called BSIM3. Theses models for transistors use equations that are continuous over the entire range of operation (sub-threshold, linear region and saturation region). The equations for mobility are improved. Equations for temperature variation, stress effects, noise, tunneling have been added and/or improved. BSIM3 is presently the industry standard among all these models. It represents a MOSFET with many electrical and structural parameters, among which, only *W* and *L* are under the control of a circuit designer. All the rest are fixed for all MOSFETs integrated in a given fabrication technology, and are provided to the designer as an “untouchable" deck of device parameters. (There are over 200 parameters in some versions of BISM3 models)



SPICE LEVEL-49 EQUATIONS FOR VT

$$V_{th} = VTH0 + K1 \cdot (\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}) - K2 \cdot V_{bseff}$$
$$+ K1 \cdot \left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1\right) \cdot \sqrt{\phi_s} + (K3 + K3_b \cdot V_{bseff}) \cdot \frac{TOX}{W'_{eff} + W_0} \cdot \phi_s$$
$$- DVT0 \cdot \left(\exp\left(-DVT1 \cdot \frac{L_{eff}}{2l_t}\right) + 2 \cdot \exp\left(-DVT1 \cdot \frac{L_{eff}}{l_t}\right)\right) \cdot (V_{bi} - \phi_s)$$
$$- \left(\exp\left(-DSUB \cdot \frac{L_{eff}}{2l_{t0}}\right) + 2 \cdot \exp\left(-DSUB \cdot \frac{L_{eff}}{l_{t0}}\right)\right) \cdot (ETA0 + ETAB \cdot V_{bseff}) \cdot V_{ds}$$
$$- DVT0W \cdot \left(\exp\left(-DVT1W \cdot \frac{L_{eff} \cdot W_{eff}}{2l_{tw}}\right) + 2 \cdot \exp\left(-DVT1W \cdot \frac{L_{eff} \cdot W_{eff}}{l_{tw}}\right)\right) \cdot (V_{bi} - \phi_s)$$

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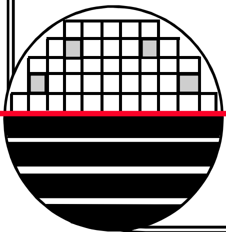


SPICE LEVEL-49 EQUATIONS FOR UO

MOBMOD = 1

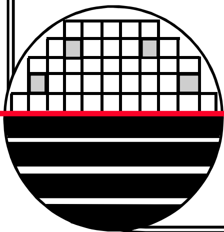
$$\mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{bseff}) \cdot \left(\frac{V_{gsteff} + 2 \cdot V_{th}}{TOX}\right) + UB \cdot \left(\frac{V_{gsteff} + 2 \cdot V_{th}}{TOX}\right)^2}$$

UA, UB and UC are emperically fit and replace THETA and VMAX used in LEVEL 3

Effective Vgs - Vth

$$V_{gsteff} = \frac{2 \cdot n \cdot V_t \cdot \ln\left[1 + \exp\left(\frac{V_{gs} - V_{th}}{2 \cdot n \cdot V_t}\right)\right]}{1 + 2 \cdot n \cdot COX \cdot \sqrt{\frac{2 \cdot \phi_s}{q \cdot \varepsilon_{si} \cdot NCH}} \cdot \exp\left(-\frac{V_{gs} - V_{th} - 2 \cdot VOFF}{2 \cdot n \cdot V_t}\right)}$$

n=1 + NFACTOR *Cd/COX + ((CDSC + CDSCD*Vds + CDSCB*Vbseff) – (exp(-DVT1*Leff/2lt) + 2exp(-DVT1*Leff/lt)))/COX + CIT/C0X



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SPICE LEVEL-49 EQUATIONS FOR ID

Effective Vds

$$V_{dseff} = V_{dsat} - \frac{1}{2} \cdot \left(V_{dsat} - V_{ds} - DELTA + \sqrt{(V_{dsat} - V_{ds} - DELTA)^2 + 4 \cdot DELTA \cdot V_{dsat}}\right)$$

Drain Current

$$I_{ds} = \frac{I_{dso}}{1 + \frac{R_{ds} \cdot I_{dso}}{V_{dseff}}} \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff} \cdot \mu_{eff} \cdot COX \cdot V_{gsteff} \cdot \left(1 - A_{bulk} \cdot \frac{V_{dseff}}{2 \cdot (V_{gsteff} + 2 \cdot V_t)}\right) \cdot V_{dseff}}{L_{eff} \cdot [1 + V_{dseff} / (E_{sat} \cdot L_{eff})]}$$

$$V_A = V_{Asat} + \left(1 + \frac{PVAG \cdot V_{gsteff}}{E_{sat} \cdot L_{eff}}\right) \cdot \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gsteff}}{PCLM \cdot Ab_{bulk} \cdot E_{sat} \cdot l_{itl}} \cdot (V_{ds} - V_{dseff})$$

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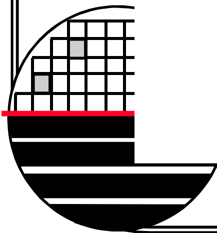

SPICE LEVEL-49 EQUATIONS FOR ID (cont)

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2 \cdot V_t)}{\theta_{rout} \cdot (1 + PDIBLCB \cdot V_{bseff})} \cdot \left(1 - \frac{A_{bulk} \cdot V_{dsat}}{A_{bulk} \cdot V_{dsat} + V_{gsteff} + 2 \cdot V_t}\right)$$

$$\theta_{rout} = PDIBLC1 \cdot \left[\exp\left(-DROUT \cdot \frac{L_{eff}}{2 \cdot l_{t0}}\right) + 2 \cdot \exp\left(-DROUT \cdot \frac{L_{eff}}{l_{t0}}\right)\right] + PDIBLC2$$

$$\frac{1}{V_{ASCBE}} = \frac{PSCBE2}{L_{eff}} \cdot \exp\left(\frac{-PSCBE1 \cdot l_{itl}}{V_{ds} - V_{dseff}}\right)$$

$$V_{Asat} = \frac{E_{sat} \cdot L_{eff} + V_{dsat} + 2 \cdot R_{ds} \cdot VSAT \cdot COX \cdot W_{eff} \cdot V_{gsteff} \cdot \left[1 - \frac{A_{bulk} \cdot V_{dsat}}{2 \cdot (V_{gsteff} + 2 \cdot V_t)}\right]}{2/\lambda - 1 + R_{ds} \cdot VSAT \cdot COX \cdot W_{eff} \cdot A_{bulk}}$$

$$l_{itl} = \sqrt{\frac{\varepsilon_{si} \cdot TOX \cdot XJ}{\varepsilon_{ox}}}$$

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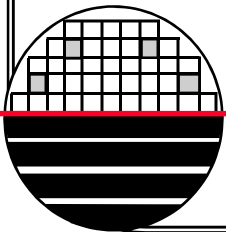
PARAMETERS FOR SPICE BSIM3 LEVEL 49

SPICE BSIM3 LEVEL 49 MODEL PARAMETERS FOR MOS TRANSISTORS:

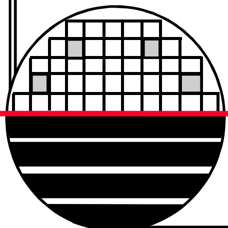
Control	LEVEL=49	
Control	MOBMOD=1	Mobility model selector choice
Control	CAPMOD=1	Capacitor model selector choice
Process	TOX	Gate Oxide Thickness
Process	XJ	Drain/Source Junction Depth
Process	NCH	Channel Surface doping concentration
Process	NSUB	Channel doping concentration
Process	XT	Distance into the well where NCH is valid
Process	NSF	Fast Surface State Density
Process	NGATE	Gate Doping Concentration
W and L	WINT	Isolation Reduction of Channel Width
W and L	LINT	Source/Drain Underdiffusion of Gate



Note: only some of the few hundred parameters

PARAMETERS FOR SPICE BSIM3 LEVEL 49

DC	VTH0	Threshold voltage, Long, Wide Device, Zero Substrate Bias = VTO in level 3
DC	U0	Low Field Mobility, UO in level 3
DC	PCLM	Channel Length Modulation Parameter
Diode & Resistor	RSH	Drain/Source sheet Resistance
Diode & Resistor	JS	Bottom junction saturation current per unit area
Diode & Resistor	JSW	Side wall junction saturation current per unit length
Diode & Resistor	CJ	Bottom Junction Capacitance per unit area at zero bias
Diode & Resistor	MJ	Bottom Junction Capacitance Grading Coeficient
Diode & Resistor	PB	PB is the junction built in voltage
Diode & Resistor	CJSW	Side Wall Junction Capacitance per meter of length
Diode & Resistor	MJSW	Side Wall Junction Capacitance Grading Coeficient
AC	CGSO	Zero Bias Gate-Source Capacitance per meter of gate W
AC	CGDO	Zero Bias Gate-Drain Capacitance per meter of gate W
AC	CGBO	Zero Bias Gate-Substrate Capacitance per meter of gate L



Note: only some of the few hundred parameters

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EXCEL SPREADSHEET SPICE PARAMETER CALCULATOR

	A	B	C	D	E	F	G	H	I	J	K	L
1	ROCHESTER INSTITUTE OF TECHNOLOGY								SPICE_Parameter_Calculator.xls			
2	MICROELECTRONIC ENGINEERING								1/18/2007			
3												
4	CALCULATION OF MOSFET SPICE PARAMETERS								DR. LYNN FULLER			
5												
6	To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless											
7	you are sure of the consequences. The calculated results are shown in the purple boxes.											
8												
9	CONSTANTS											
10												
11	T=	300	K		Boron D0	0.76	cm2/s					
12	KT/q =	0.026	volts		Boron Ea	3.46	eV					
13	ni =	1.45E+10	cm-3		Phosphorous D0	3.85	cm2/s					
14	Eo =	8.85E-14	F/cm		Phosphorous Ea	3.66	eV					
15	Er si =	11.7										
16	Er SiO2 =	3.9		Carrier Velocity Saturation occurs at ~ 5E6 to 2E7 cm/s, extracted values can be artificially 2 times higher								
17	E affinity =	4.15	volts		Critical value of electric field Ec of ~8E3 to 3E4 V/cm for electrons, ~2E4 to 1E5 V/cm for holes							
18	q =	1.60E-19	coul									
19	Eg =	1.124	volts									
20												
21	INTRODUCTION											
22												
23	This spreadsheet calculates nmos or pmos level one, three and BSIM3 SPICE parameters from details known about the process parameters, device layout and											
24	fabrication history. Level one spice parameters assume mobility is a function of total impurity concentration and temperature only. Level one uses the parameter											
25	LAMBDA for channel length modulation. Different equations are used to calculate Ids in the saturation and non-saturation regions of operation.											
26												
27	The level three SPICE model is derived from the level one model with some additional parameters to better account for the decrease in carrier mobility for											
28	high vertical and lateral electric fields. The level three model also allows the user to account for narrow channel effects, drain induced barrier lowering (DIBL),											
29	and gives better sub threshold characteristics. For example the parameter LAMBDA is replaced by a more complex model using the parameter VMAX and											
30	KAPPA. The low field mobility value UO is modified for high gate electric fields with parameter THETA and modified for high lateral electric fields through											
31	the VMAX parameter. Different equations are used to calculate Ids in the saturation, non-saturation and subthreshold regions of operation.											
32												
33	The BSM3 SPICE parameters are derived from the level one and three parameters. BSIM models have hundreds of parameters used to fully describe DC and AC											
34	deivce operation, temperature effects, noise, stress effects and more. Most of the parameters can only be determined from measured device performance. In											
35	this spreadsheet the BSIM3 parameters are derived from level one and level three parameters. All other parameters are not specified and the default values are											
36	invoked. The single equation for Ids is used that is valid in saturation, non-saturation and subthreshold regions of operation, making convergence during circuit											
37	simulation more reliable.											
38												
39												
40	References:	MOSFET Modeling with SPICE, Daniel Foty, 1997, Prentice Hall, ISBN-0-13-227935-5										
41		Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5										
42		UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.										
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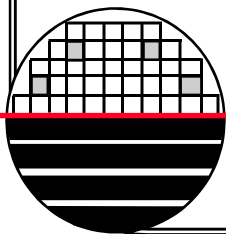
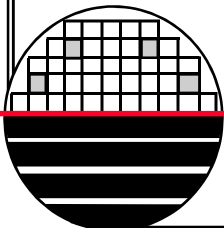
Page 1

SPICE Parameter Calculator.xls



INPUTS AND RESULTS

	A–C	D	E	F	G–J	K	L
44	**LAYOUT PARAMETERS**				**VALUES CALCULATED FROM PROCESS PARAMETERS**		
45	(assume source and drain are symmetrical)						
46	L	2	um		Diffusion Constant at Temp of Well Drive	1.43E-13	cm2/s
47	W	16	um		Starting wafer doping = 1/(q um ax Rho)	4.42E+14	cm-3
48	Area of Drain/Source	96	um2		Well Surface Concentration= Ns = Dose / (pi D t)^0.5	1.45E+17	cm-3
49	Perimeter of Drain/Source	44	um		Well Depth = ((4DdTd/Dose) ln(Nsub(piDdTd)^0.5))^0.5	3.75	um
50	# squares between Contact and Channel	0.143			Well average doping, Nave = Dose/xj	5.33E+16	cm-3
51	# squares between LDD/N+ and Channel	0.025			Bulk Well Majority Carrier Mobility at N=Nave	394.32	cm2/v-s
52					Bulk Well Minority Carrier Mobility at N=Nave	1004.52	cm2/v-s
53	**PROCESS PARAMETERS**	1=yes, 0=No			Well Sheet Resistance = 1/(q(µ(Nave))Dose)	792.50	ohms
54	Aluminum gate	0	} select one		Well surface mobility at Surface Doping Concentration	725.76	cm2/V-s
55	n+ Poly gate	1			Wdmax = (4 eoesi φs / q / Nave)^0.5	0.143	um
56	p+ Poly gate	0			Metal Work Function, φm	4.12	volts
57	N well (pMOSFET)	0	} select one		Magnitude of Semiconductor Potential (Fermi - Intrinsic), φs	0.419	volts
58	P well (nMOSFET)	1			Oxide Capacitance/cm2 = Cox'	2.30E-07	F/cm2
59	Vt adjust Dose (+ for Boron, - for Phos)	0.00E+00	cm-2		Metal Semi Work Function Diff, φms	-0.170	volts
60	Gate Oxide Thickness	150	Å		Flat Band Voltage, VFB =	-0.379	volts
61	NSS	3.00E+11	cm-2		Threshold Voltage, VTO	1.33	volts
62	Starting Wafer Resistivity	10	ohm-cm		Threshold Adjust, ΔV =q Dose/2/Cox'	0.00	volts
63	Well Dose	2.00E+13	cm-2		Ion Implanted Adjusted Threshold Voltage, VT	1.33	volts
64	Well Drive Time	710	min		Diffusion Constant at Temp of D/S Anneal	1.17E-14	cm2/s
65	Well Drive Temperature	1100	C		D/S Junction Depth, XJ =	0.18	um
66	LDD D/S Dose	2.50E+13	cm-2		D/S average doping, Nave = Dose/xj	1.36E+18	cm-3
67	LDD D/S Drive Time	30	min		Bulk Mobility in D/S at N=Nave	230.94	cm2/v-s
68	LDD D/S Drive Temperature	1000	C		D/S Sheet Resistance = 1/(q(µ(Nave))Dose)	1082.55	ohms
69	Field Oxide Thickness	6000	Å		Lateral Diffusion = LD = 0.8*Xj	0.15	µm
70	Minority Carrier Lifetime in the well	1	µs		Capacitance/cm2 for Field Oxide	5.75E-09	F/cm2
71	D/S Dose (N+ or P+)	2.00E+15	cm-2		D/S Width of Space Charge Layer at Zero Bias, Xdso =	0.152	µm
72					D/S Width of Space Charge Layer at Vdd, Bias Xds =	0.380	µm
73					Leff = Lmask - 2*LD - 2*Xdso	1.400	µm
74					Built in Voltage for D/S pn junction	0.95	volts
75					Junction reverse bias current density, JS	3.23E-08	A/m2
76					Junction Capacitance for D/S at zero bias	6.80E-08	F/cm2
77					Lambda, Calculated, ((Lmax/Lmin)-1)/Vdd	0.031	1/volt
78	**MEASURED TRANSISTOR VALUES**						
79	Vdd	5	volts		**CALCULATED SPICE PARAMETERS FROM MEASURED VALUES**		
80	Magnitude of IDS at Vgs=Vds=Vdd	5.41	mAmps	=I'ds	Ueff mobility to match IDS at Vgs=Vds=Vdd	286.44	cm2/v-s
81	Magnitude of IDS at Vgs=Vdd, Vds=Vdsat	5.12	mAmps	=Idsat	LAMBDA measured	0.03	1/volts
82	VTO (+ for nmos and - for pmos))	1.1	volts		VT0 measured	1.1	volts
83	Isub-min	0.001	nAmps		JS = Isub-min/Area of Drain measured	1.04E-02	A/m2
84	D/S Sheet Resistance	39.2	ohms		RSH measured	39.2	ohms
85	Lambda	0.03	1/volts	Page 2			
86							



PARAMETERS FOR SPICE LEVEL 1

SPICE PARAMETERS FOR LEVEL ONE MODEL

1 The parameters in the yellow boxes are calculated from the other parmaters and thus should not be entered in the SPICE model
2 If the SPICE parameters from measured values are different than the calculated SPICE parameters you might want to use them instead.
3 We assume the model definition has L, W, AD, AS, PD, PS, NRS, NRD specified for calculation of some of the parameters in the yellow boxes
4 Lambda is different for every different length transistor in the level one model, so a different model is needed for each different length mosfet

SPICE Parameter	Name	SPICE Parameters Using Process Parameters		note: most parameters use O not 0 at end of parameter name ("oh" not "zero")
1	Level	1		Schichman and Hodges Model
2	VTO	1.33	volts	Zero Bias Threshold Voltage, enter value if threshold adjust implant is used
3	KP	2.50E-04	F/s-volt	Transconductance Parameter, KP = $U0\ \varepsilon si\ \varepsilon o / Tox$
4	GAMMA	9.52E-01	$(volt)^{1/2}$	Bulk Threshold Parameter, GAMMA = $[2q\ \varepsilon si\ \varepsilon o\ NSUB/Cox^2]^{1/2}$
5	PHI	0.419	volts	PHI is the semiconductor potential, Intrinsic Level to Fermi Level difference
6	LAMBDA	0.031	1/volts	Channel length modulation parameter
7	RD	27.06	ohms	Series Drain Resistance
8	RS	27.06	ohms	Series Source Resistance
9	CBD	7.08E-14	F	CBD zero bias bulk to drain junction capacitance, CBD = CJ AD + CJSW PD
10	CBS	7.08E-14	F	CBD zero bias bulk to source junction capacitance, CBD = CJ AD + CJSW PD
11	IS	3.10E-18	A	D/S junction leakage current
12	PB	0.95	volts	PB is the junction built in voltage, PB = (KT/q)ln(NSUB/ni) + 0.56
13	CGSO	3.40E-10	F/m	G-to-S overlap C (per m channel width) CGSO=Cox'(mask overlap in L direction + LD)
14	CGDO	3.40E-10	F/m	G-to-D overlap C (per m channel width) CGDO=Cox'(mask overlap in L direction + LD)
15	CGBO	5.75E-10	Fm	G-to-well overlap C (per meter channel length) CGSO=Cox'(mask overlap in W direction)
16	RSH	1082.55	ohms	Sheet resistance of D/S
17	CJ	6.80E-04	F/m2	D/S Bottom junction capacitance/m2,
18	MJ	0.5		Junction Grading Coeficient for bottom of D/S Junction
19	CJSW	1.26E-10	F/m	D/S side wall junction capacitance per meter of D/S permeter
20	MJSW	0.5		Junction Grading Coeficient for side of D/S Junction
21	JS	3.23E-08	A/m2	D/S junction leakage current
22	TOX	1.50E-08	m	Gate Oxide Thickness
23	NSUB	1.45E+17	cm-3	Well Doping Nave
24	NSS	3.00E+11	cm-2	Surface State Density as known from process knowledge
25	NFS	0		Fast Surface States, Always set to zero
26	TPG	1		+1 if gate doped opposite of channel, -1 if gate doped same as channel, 0 if gate is aluminum
27	XJ	0.18	um	D/S Junction Depth
28	LD	0.15	um	Lateral Diffusion of D/S into the channel arbitrarly set to 80% of XJ
29	UO	363	cm2/v-s	Well surface minority carrier mobility at well surface concentration divided by two

```
.MODEL RITSUBN1 NMOS (LEVEL=1
+VTO=1.0 LAMBDA= 0.031 PB=0.95 CGSO=3.4E-10 CGDO=3.4E-10
+CGBO=5.75E-10 RSH=1082 CJ=6.8e-4 MJ=0.5  CJSW=1.26e-10
+MJSW=0.5 JS=3.23e-8 TOX=150E-10  NSUB=1.45e17  NSS=3E11
+TPG=+1 XJ=0.18U LD=0.15U UO=363)
```

```
.MODEL RITSUBP1 PMOS (LEVEL=1
+VTO=1.0 LAMBDA= 0.05 PB=0.94 CGSO=5.08E-10 CGDO=5.08E-10
+CGBO=5.75E-10 RSH=33.7 CJ=5.01e-4 MJ=0.5  CJSW=1.38e-10
+MJSW=0.5 JS=6.43e-8 TOX=150E-10  NSUB=7.23e16  NSS=1E11
+TPG=+1 XJ=0.28U LD=0.22U UO=363)
```

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PARAMETERS FOR SPICE LEVEL 3

SPICE PARAMETERS FOR LEVEL THREE MODEL

1 WD is estimated to be 1/2 the field oxide thickness for a LOCOS process
2 THETA is calculated from Ueff = UO/(1+THETA(Vgs-Vt)) and Ids=Ueff (Cox'/2) (W/L)(Vgs-Vt)^2(1+λVds) using measured Ids and Vt values
3 DELTA is calculated = q*Nave*(Xds)^2 / (εo εsi (2 φs))
4 KAPPA is calculated = [(qNsub/(2 εoεr))((1-I/I')(L-2LD-Xdso-Xds))^2)/(Vds-Vdsat)]^0.5
5 VMAX is calculated from effective mobility times electric field at Vgs=Vds=Vdsat, where E=Vdsat/Leff
6 ETA is calculated from the ratio of charge in the channel at Vds=Vdd to charge in the channel at Vds=zero

note: Parameters in Red come directly from SPICE Level One
note: most parameters use O not 0 at end of parameter name ("oh" not "zero")

Parameter	Name	Value	Units	
1	Level	3		
2	TPG	1		Type of Gate Material
3	TOX	1.50E-08	m	Gate Oxide Thickness
4	LD	2.95E-07	m	Channel Length Reduction from Drawn Value
5	WD	3.00E-07	m	Channel Width Reduction From Drawn Value
6	UO	726	cm2/V-s	Zero Bias Low Field Mobility
7	VTO	1.33	V	Measured threshold voltage for long wide devices with zero substrate bias
8	THETA	0.393	1/V	Gate Field Induced Mobility Reduction Parameter
9	RS	27.06	ohm	In level 3 only lumped resistance is available, each different width FET has a different model
10	RD	27.06	ohm	In level 3 only lumped resistance is available, each different width FET has a different model
11	DELTA	2.27		Narrow Channel Effect on the Threshold Voltage
12	NSUB	1.45E+17	cm-3	Effective Substrate Doping
13	XJ	1.84E-07	m	Drain/Source junction depth
14	VMAX	1.02E+07	m/s	Maximum Carrier Velocity (extraction can gvie 1.2 to 2 times expected saturation velocity)
15	ETA	0.837		DIBL Coefficient
16	KAPPA	0.509	1/V	Channel Length Modulation Effect on the Drain Current
17	NFS	3.00E+11	cm-2	Surface State Density
18	CGSO	3.40E-10	F/m	Zero Bias Gate-Source Capacitance
19	CGDO	3.40E-10	F/m	Zero Bias Gate-Drain Capacitance
20	CGBO	5.75E-10	F/m	Zero Bias Gate-Substrate Capacitance
21	PB	0.95	V	PB is the junction built in voltage, PB = (KT/q)ln(NSUB/ni) + 0.56
22	XQC	0.40		Charge Partitioning Parameter (from Ward and Dutton)

A different model is needed for each transistor of different length or width. Example models shown below.

```
*.MODEL RITSUBN3 NMOS (LEVEL=3 TPG=1 TOX=1.5E-8 LD=2.95E-7 WD=3.00E-7
*+U0= 726 VTO=0.5 THETA=0.393 RS=27 RD=27 DELTA=2.27 NSUB=1.45E17
*+XJ=1.84E-7 VMAX=1.10E7 ETA=0.837 KAPPA=0.509 NFS=3E11
*+CGSO=3.4E-10 CGDO=3.48E-10 CGBO=5.75E-10 PB=0.95 XQC=0.4)

*.MODEL RITSUBP3 PMOS (LEVEL=3 TPG=1 TOX=1.5E-8 LD=3.61E-7 WD=3E-7
+UO=377 VT0=-0.93 THETA=0.32 RS=33.7 RD=33.7 DELTA=2.35 NSUB=7.12E16
+XJ=2.26E-7 VMAX=3.84E6 ETA=0.897 KAPPA=4.481 NFS=3E11
+CGSO=4.15E-10 CGD0=4.15E-10 CGBO=5.75E-10 PB=0.94 XQC=0.40)
```

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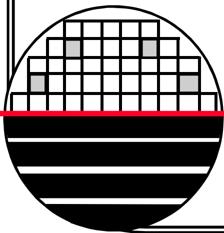
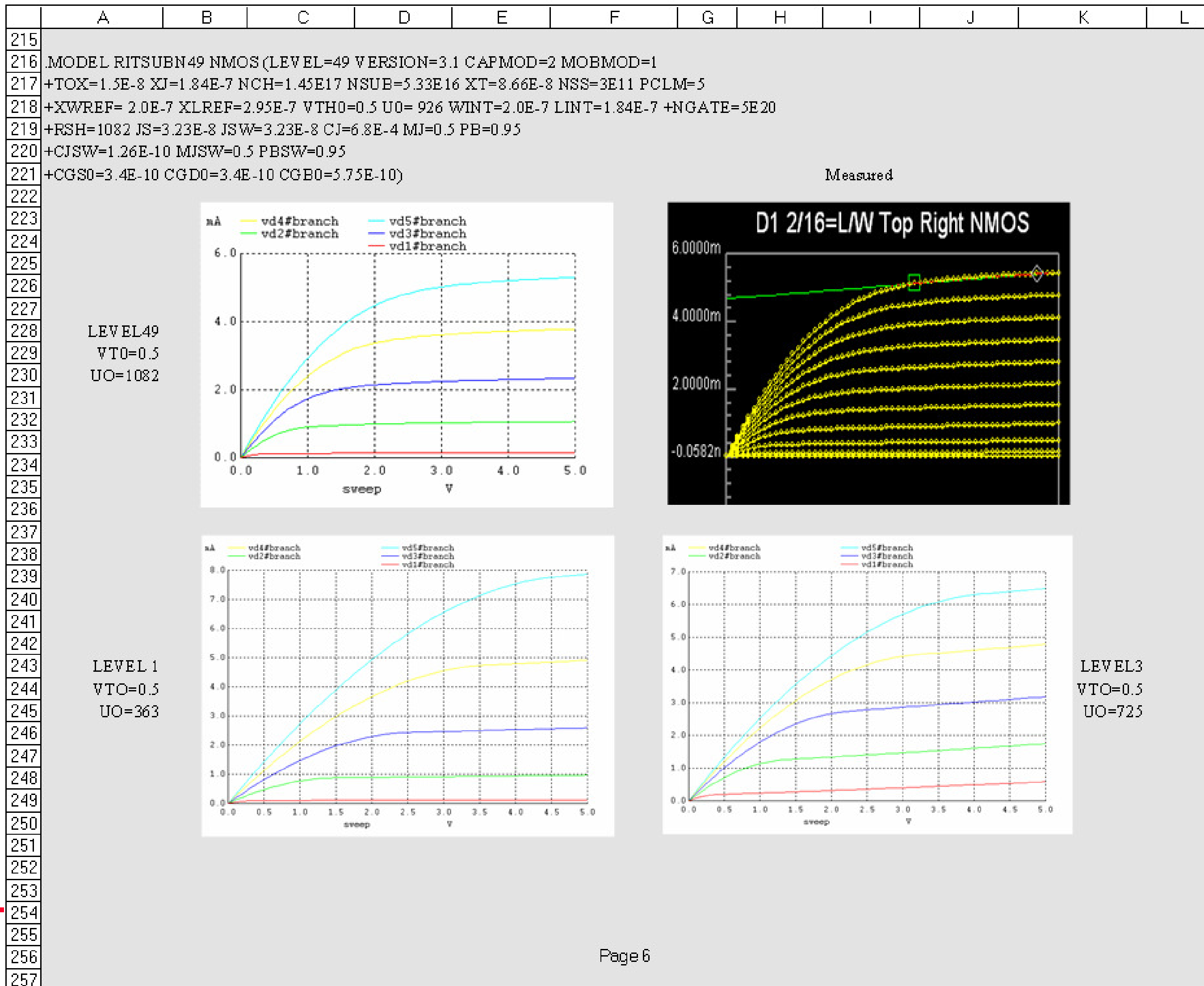


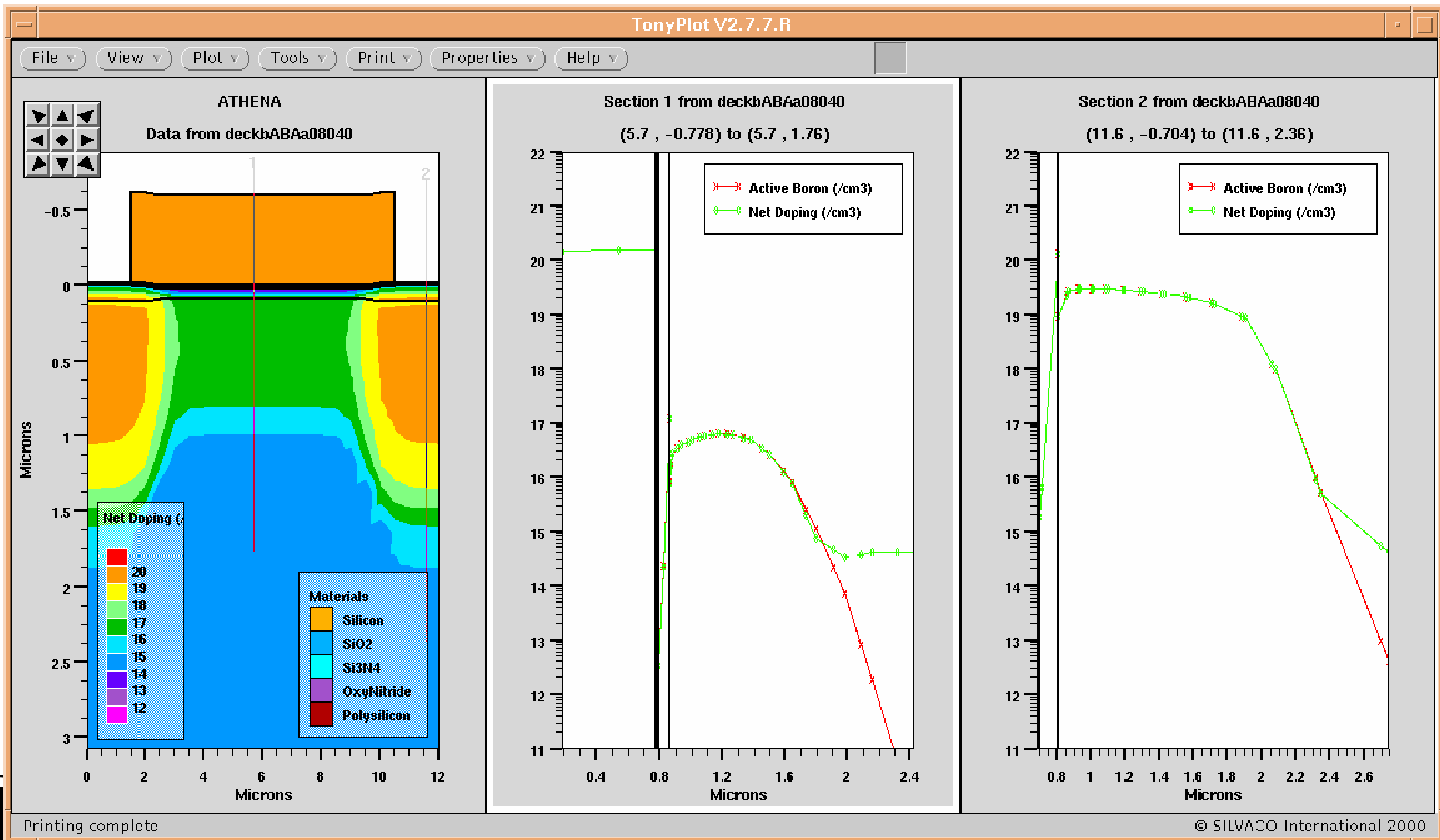
PARAMETERS FOR SPICE LEVEL 49

	A	B	C	D	E	F
172	**SPICE PARAMETERS FOR BISIM3 VER 3.1, LEVEL 49**					
173	BSIM3V3 is the industry standard, physics-based, deep submicron MOSFET SPICE model for digital and analog circuit design from the Device Group at the					
174	University of California at Berkeley. Level 8 is the origional Berkeley version, Level 81 is a slightly modified Silvaco version, Level 49 and 53 are Hspice versions.					
175						
176						note: most parameters use 0 not O at end of parameter name ("zero" not "oh")
177						note: Parameters in Red come directly from SPICE Level One and/or Three
178	Parameter	Name		Value	Units	
179	Control	Level		49		Level 8, 81, 49 or 53
180	Control	VERSION		3.1		3.0, 3.1 or 3.2 versions, default is the newest version
181	Control	MOBMOD		1		Mobility model selector (1,2,3,4... selects slightly different equations for calculation of Ueff)
182	Control	CAPMOD		2		Capacitance model selector (1,2,3,4... selects slightly different equations for gate Ceff)
183	Process	TOX		1.50E-08	m	Gate oxide thickness
184	Process	XJ		1.84E-07	m	Junction Depth
185	Process	NCH		1.45E+17	cm-3	Well surface doping concentration
186	Process	NSUB		5.33E+16	cm-3	Well doping concentration below the surface
187	Process	XT		1.43E-07	m	Distance into well where surface concentration is valid, Default = 1.5E-7m
188	Process	NSS		3.00E+11	cm-2	Surface State Density, Level 3 NFS or Level 1 NSS treated as equal
189	W and L	XWREF		2.0E-07	m	Isolation Reduction of Channel Width (from process knowledge)
190	W and L	XLREF		2.95E-07	m	Source/Drain Underdiffusion of Gate
191	DC	VTH0		1.33	V	Threshold voltage, Long Wide Device, Zero Substrate Bias = VTO in level 3
192	DC	U0		725.76	cm2/v-s	Low Field Mobility
193	DC	WINT		2.0E-07	m	Isolation Reduction of Channel Width (from process knowledge)
194	DC	LINT		1.84E-07	m	Source/Drain Underdiffusion of Gate (set equal to XJ)
195	DC	PCLM		5.00		Channel Length Modulation Parameter, default = 1.3 (select to fit Ids vs. Vds family)
196	DC	NGATE		5.00E+20	m-3	Gate Doping (5E20 if Diffusion Doped, Dose/Poly Thickness if Ion Implanted with D/S)
197	Diode/Resistor	RSH		1082.55	ohm/sq	Drain/Source sheet Resistance
198	Diode/Resistor	JS		3.23E-08	A/m2	Bottom junction saturation current per unit area
199	Diode/Resistor	JSW		3.23E-08	A/m	side wall junction saturation current per unit length
200	Diode/Resistor	CJ		6.80E-04	F/m2	Bottom Junction Capacitance per unit area at zero bias
201	Diode/Resistor	MJ		0.5		Bottom Junction Capacitance Grading Coeficient
202	Diode/Resistor	PB		0.95	V	PB is the junction built in voltage, PB = (KT/q)ln (NSUB/ni) + 0.56
203	Diode/Resistor	CJSW		1.26E-10	F/m	Side Wall Junction Capacitance per meter of length at zero bias
204	Diode/Resistor	MJSW		0.5		Side Wall Junction Capacitance Grading Coeficient
205	Diode/Resistor	PBSW		0.95	V	PBSW is the side wall junction built in voltage, PB = (KT/q)ln (NSUB/ni) + 0.56
206	AC	CGS0		3.40E-10	F/m	Zero Bias Gate-Source Capacitance per meter of gate width
207	AC	CGD0		3.40E-10	F/m	Zero Bias Gate-Drain Capacitance per meter of gate width
208	AC	CGB0		5.75E-10	F/m	Zero Bias Gate-Substrate Capacitance per meter of gate length
209						
210						
211						
212						
213						Page 5
214						

RESULTS USING SPICE LEVELS 49, 3, 1



SILVACO ATHENA SIMULATIONS OF D/S IMPLANT



SILVACO ATHENA (SUPREM)

```
go athena
# set grid
line x loc=0.0 spac=0.1
line x loc=1.0 spac=0.05
line x loc=10.0 spac=0.05
line x loc=12.0 spac=0.1

line y loc=0.0 spac=0.01
line y loc=2.2 spac=0.01
line y loc=3.5 spac=0.3
line y loc=6.0 spac=0.5

init silicon phosphor resistivity=11.3 orientation=100 space.mult=5.0

# ramp up from 800 to 900°c soak 50 min dry o2, ramp down to 800 n2
diff time=10 temp=800 t.final=900 dryo2 press=1.0 hcl.pc=0
diff time=50 temp=900 weto2 press=1.0 hcl.pc=0
diff time=20 temp=900 t.final=800 nitro press=1.0 hcl.pc=0

deposit photoresist thickness=1.0
etch phtotoresist left ;1.x=2.0
etch photoresist right p1.x=10.00

# ion implant drain and source
implant boron dose=1e15 energy=70 tilt=0 rotation=0 crysatal lat.ratio1=1.0 lat.ratio2=1.0

Etch photoresist all

# ramp up from 800 to 1000°c soak 90 min, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 nitro press=1.0 hcl.pc=0
diff time=90 temp=1000 nitro press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

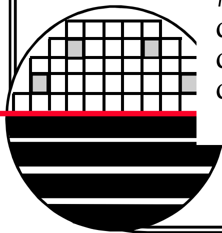
Starting wafer resistivity = 11.3 ohm-cm

Grow Kooi oxide 1000 Å

Ion Implant P-type D/S at Dose = 1E15

Strip photoresist

Anneal D/S implant



SILVACO ATHENA (SUPREM)

Ion Implant P-type channel at
Dose = 0, 4e11, 1e12, 4e12

```
# ion implant channel
implant boron dose=4e12 energy=60 tilt=0 rotation=0 crysatal lat.ratio1=1.0 lat.ratio2=1.0

etch oxide all

# ramp up from 800 to 1000°c soak 90 min dry o2, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 dryo2 press=1.0 hcl.pc=0
diff time=90 temp=1000 dryo2 press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

Grow 700 Å gate oxide

```
deposit nitride thick=0.010
```

Deposit 100 Å nitride

```
# ramp up from 800 to 1000°c soak 50 min dry o2, ramp down to 800 n2
diff time=10 temp=800 t.final=1000 dryo2 press=1.0 hcl.pc=0
diff time=50 temp=1000 dryo2 press=1.0 hcl.pc=0
diff time=20 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

Temp cycle for growth of oxynitride

```
deposit oxynitride thick=0.01
```

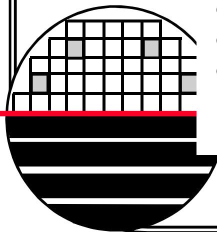
Deposit 100 Å oxynitride

```
deposit poly thick=0.60 c.boron=4e20
```

Deposit 6000 Å poly

```
# ramp up from 800 to 1000°c soak 30 min, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 nitro press=1.0 hcl.pc=0
diff time=30 temp=1000 nitro press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0
```

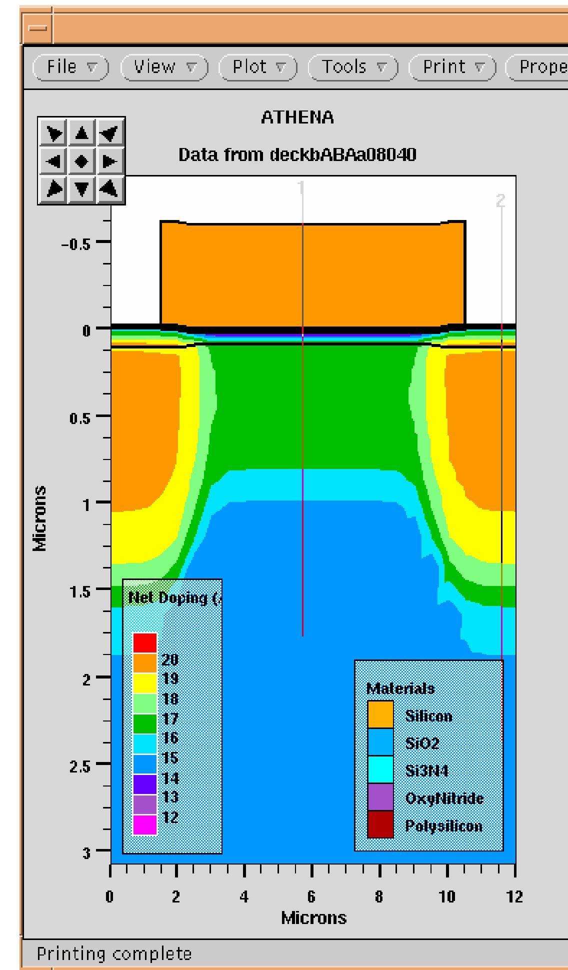
Temp cycle for poly dope



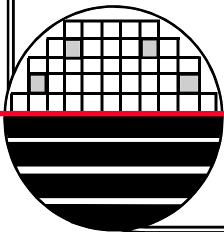
SILVACO ATHENA (SUPREM)

```
etch poly left p1.x=1.5
etch poly right p1.x=10.5

etch oxynitride left p1.x=1.5
etch oxynitride right p1.x=10.5

etch nitride left p1.x=1.5
etch nitride right p1.x=10.5

etch oxide left p1.x=1.5
etch oxide right p1.x=10.5

deposit alumin thick=0.5

etch alum start x=1.0 y= -2.0
etch cont x=1.0 y= 2.0
etch x=11.0 y= 2.0
etch done x=11.0 y= -2.0

struct outfile=UofH.str

tonyplot UofH.str

quit
```

Deposit 5000 Å aluminum



Tonyplot example Only



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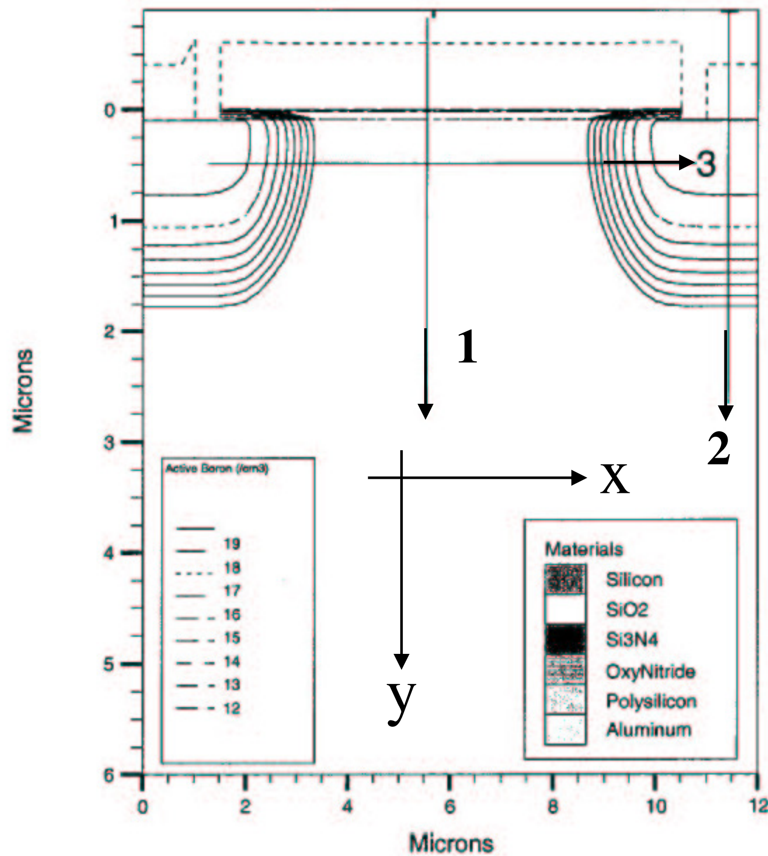
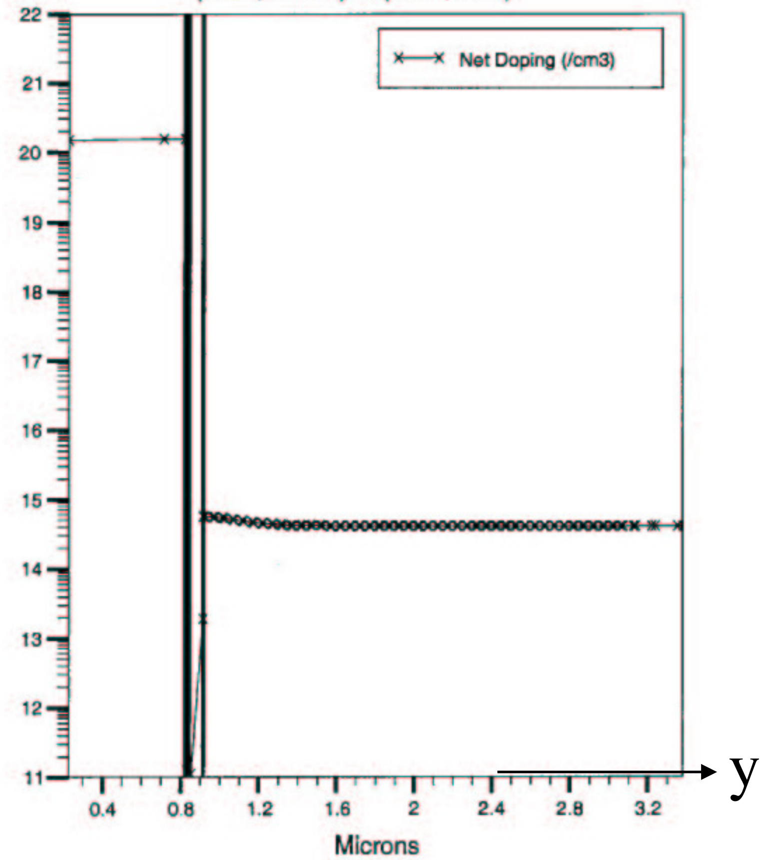
SILVACO ATHENA (SUPREM)

Channel Implant Dose = 0

Crossection of MOSFET



Channel Doping Profile 1



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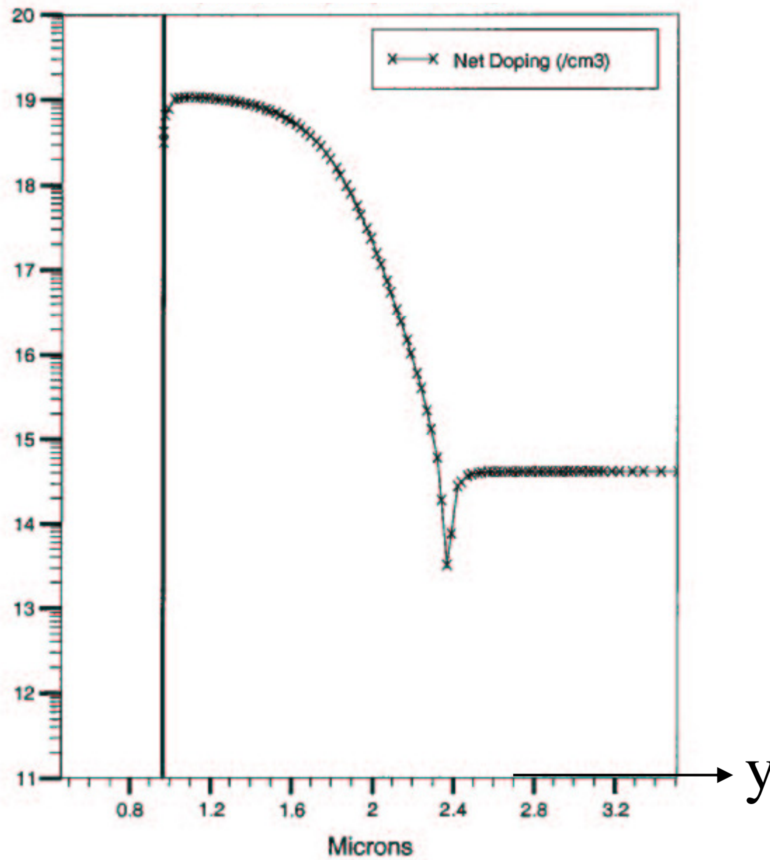
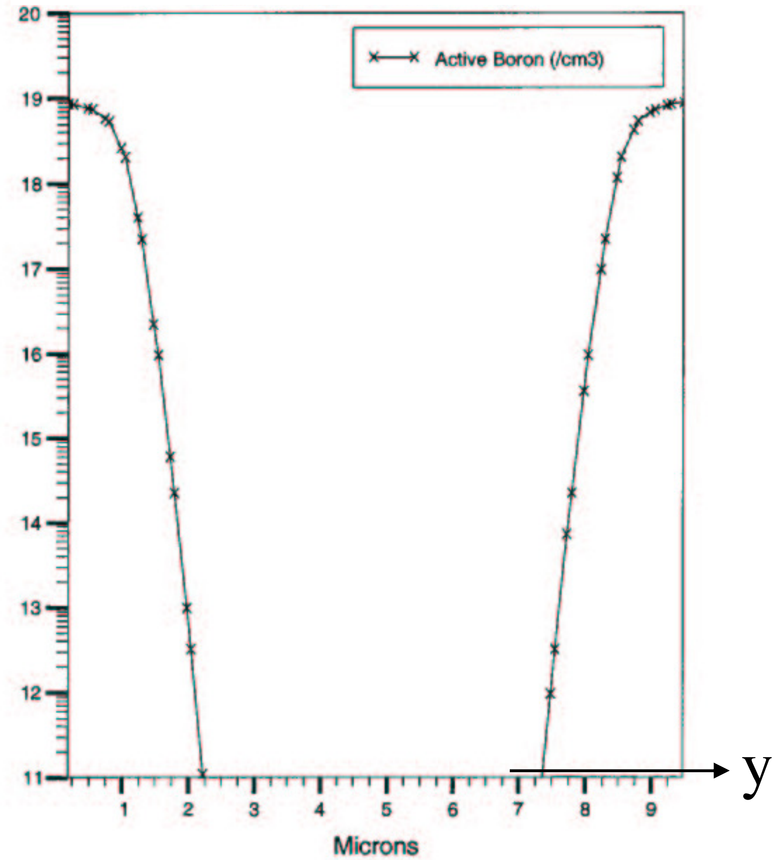
SILVACO ATHENA (SUPREM)

Channel Implant Dose = 0

D/S Doping Profile 2



Channel Doping Profile 3



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SILVACO ATLAS (DEVICE SIMULATOR)

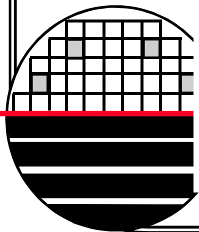
```
Go athena
Init infile=UofH.str

#name the electrodes…
Electrode name=gate x=6
Electrode name=source x=0
Electrode name=drain x=12
Electrode name=substrate backside

Extract name="vt" 1dvt ptype qss=1e11 workfunc=5.1 x.val=6

Go atlas

# define the gate workfunction
Contact name=gate p.poly
# define the Gate qss
Interface qf=1e11

# use the cvt mobility model for MOS
Models cvt srh

# set gate biases with Vds=0.0
Solve init
Solve vgate=0 vsubstrate=0 outf=solve_temp0
Solve vgate=-1 vsubstrate=0 outf=solve_temp1
Solve vgate=-1 vsubstrate=0 outf=solve_temp2
Solve vgate=-3 vsubstrate=0 outf=solve_temp3
Solve vgate=-4 vsubstrate=0 outf=solve_temp4
Solve vgate=-5 vsubstrate=0 outf=solve_temp5

# load in temporary file and ramp Vds
Load infile=solve_temp0
Log outf=Vg_0.log
Solve name=drain vdrain=0 vfinal=-5 vstep=-0.5
```

Read in structure file created by Athena

Define location of gate, source, drain and substrate

Do calculations for given gate voltage and substrate voltage (Vg=0,-1,-2,-3,-4,-5 and Vsub=0,+5,+10+15)

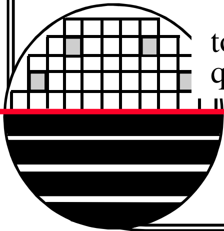
Sweep drain voltage from 0 to –5 volts In –0.5 volt steps



SILVACO ATLAS (DEVICE SIMULATOR

```
# load in temporary file and ramp vds
load infile=solve_temp1
log outf=vg_1.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp2
log outf=vg_2.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp3
log outf=vg_3.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp4
log outf=vg_4.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp5
log outf=vg_5.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# extract max current and saturation slope
extract name="pidsmax" max(abs(i."drain"))
extract name="p_sat_slope" slope(minslope(curve(abs(v."drain"), abs(i."drain")))

tonyplot –overlay vg_0.log vg_1.log vg_2.log vg_3.log vg_4.log vg_5.log –setmos1ex09_1.set
quit
```

Sweep drain voltage from 0 to –5 volts in -0.5 volt steps



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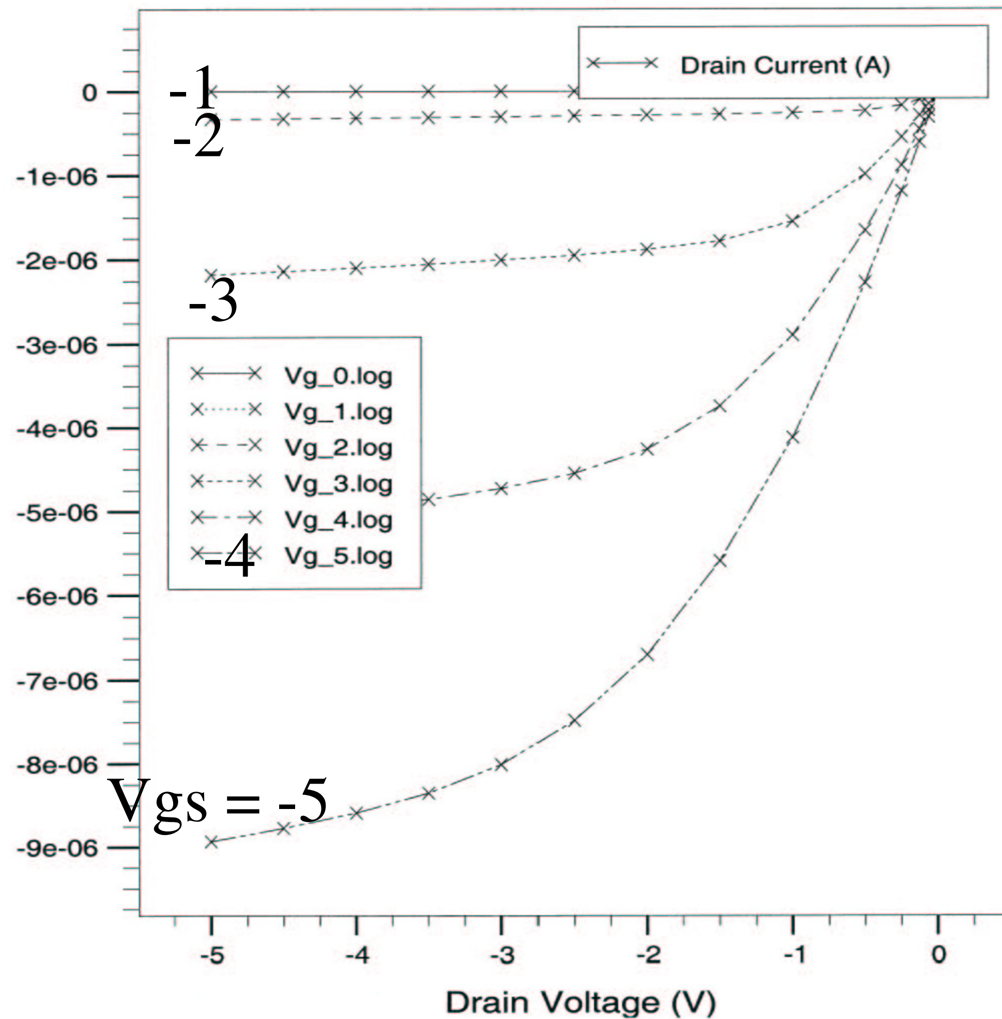
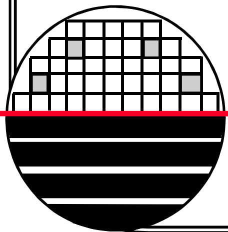
ATLAS SIMULATED FAMILY OF CURVES

Channel Implant
Dose = none
Vsub = 0





SILVACO ATHENA > ATLAS > UTMOST > SPICE

Extraction of SPICE Model Parameters from *ATLAS* Device Simulation Using *UTMOST*

Many users would like to extract SPICE models from their process and device simulation using *ATHENA* and *ATLAS* to be used in actual circuit simulation without actually fabricating the device.

Using SILVACO's *UTMOST* you can extract SPICE model parameters from the simulation results of *ATHENA* and *ATLAS*.

To guide users on how to go about extracting SPICE model parameters an example which extracts BSIM3v3 model from process/device simulation is used in this article.

All these commands can be executed from a single software – *DeckBuild*.

The commands are heavily commented so that you know their functions and purpose.

Here we will concentrate on the *UTMOST* batch mode commands. Here we only cover a very simple case and there is no local optimization. The *UTMOST* interactive mode can be used save the *UTMOST* setup into a file . *UTMOST* interactive cannot be executed from *DeckBuild*.

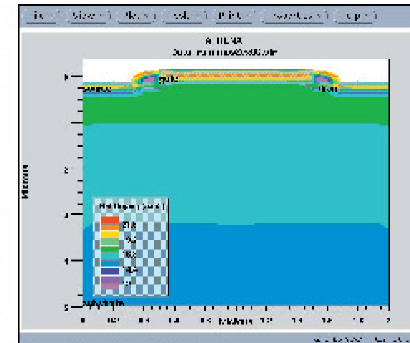


Figure 1. *TonyPlot* of Device structure.

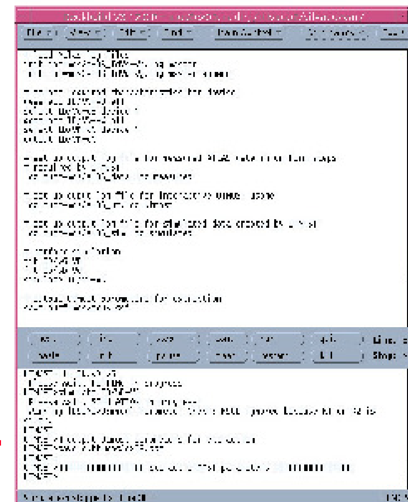
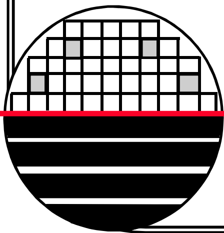


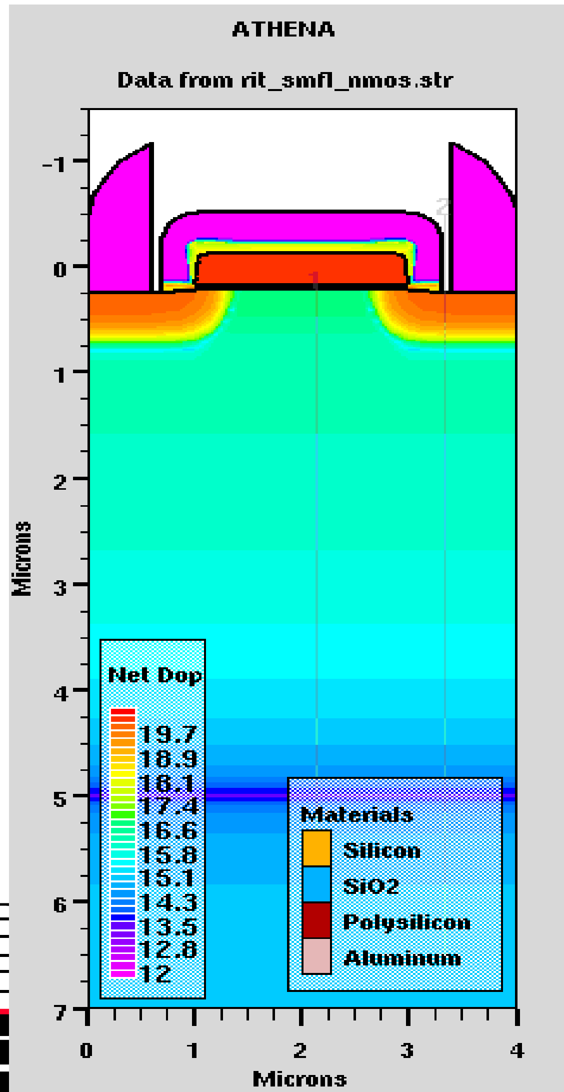
Figure 2. *DeckBuild* screen.

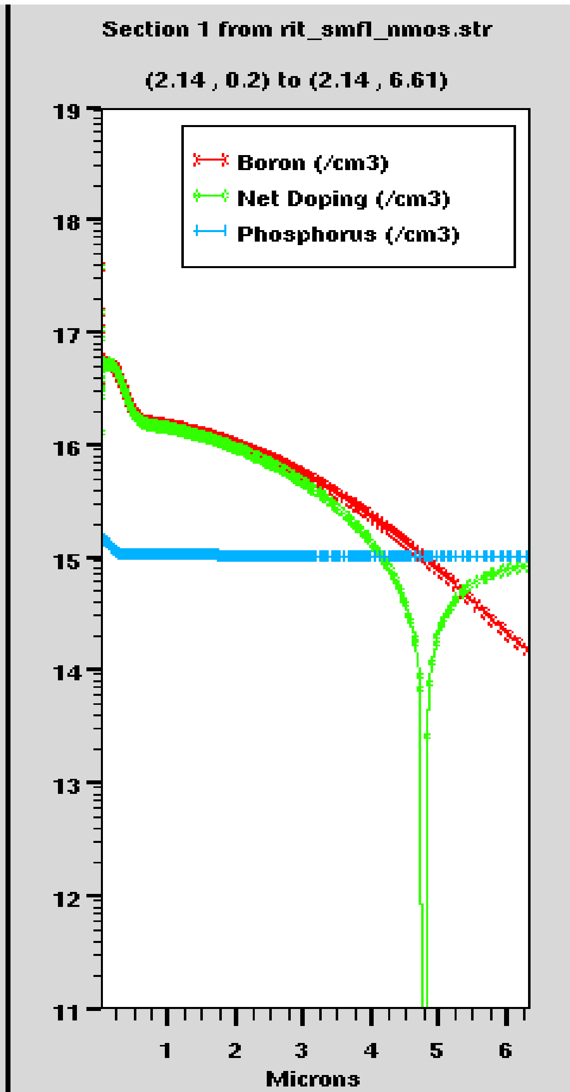
```
.---------- start of deckbuild commands ------------

# Commands that can be used in deckbuild to extract
# Spice model Parameters. The deck for TCAD is
# not complete . Below are examples of commands that
# maybe used in VWF Athena and Atlas to obtain the
# device characteristics

###### START ATHENA SIMULATION ###
# Run process simulation
go athena

# Extract the poly length LD

extract name="ld" thick poly y.val=0
extract name="utmost_ld"($ld*1.0e-4)
....
extract thickness oxide mat.occno=1 name="tox"
extract name="utmost_tox" ($tox*1.0e-10)
....

###### START ATLAS DEVICE SIMULATION ##

go atlas
```

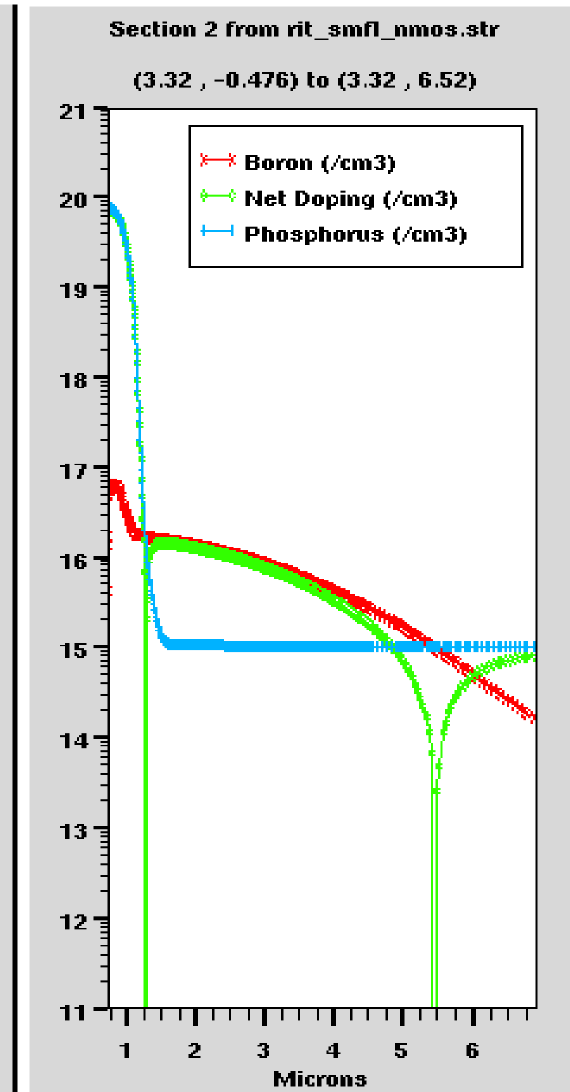


Rochester Institute of Technology
Microelectronic Engineering

SILVACO ATHENA GENERATED IMPURITY PROFILES







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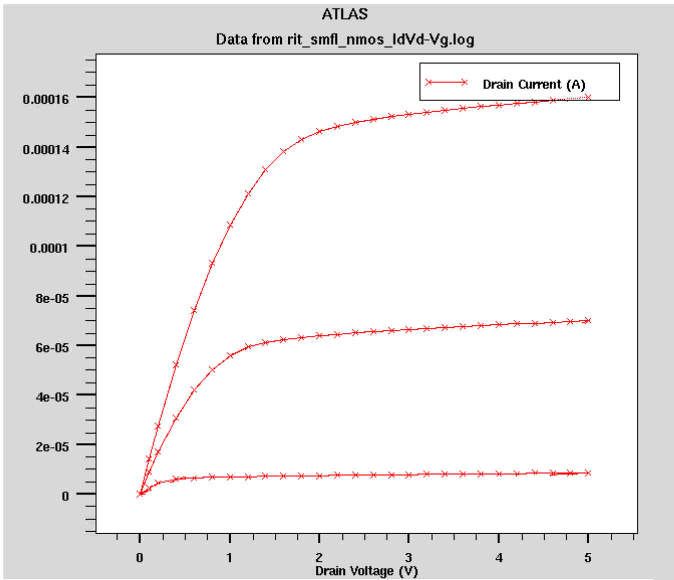
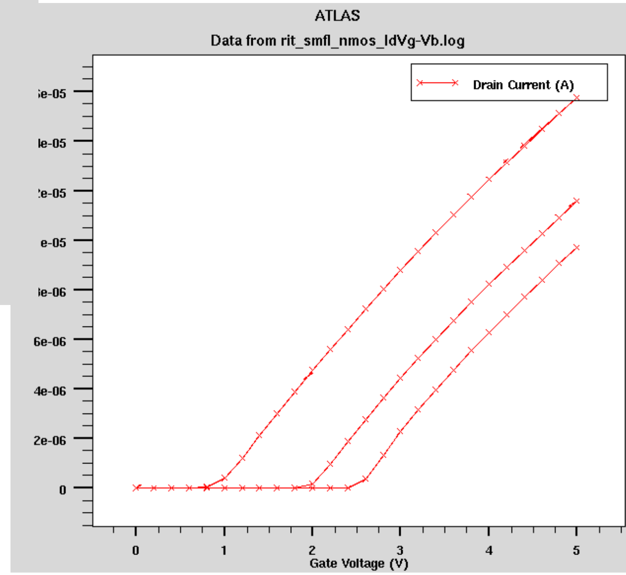
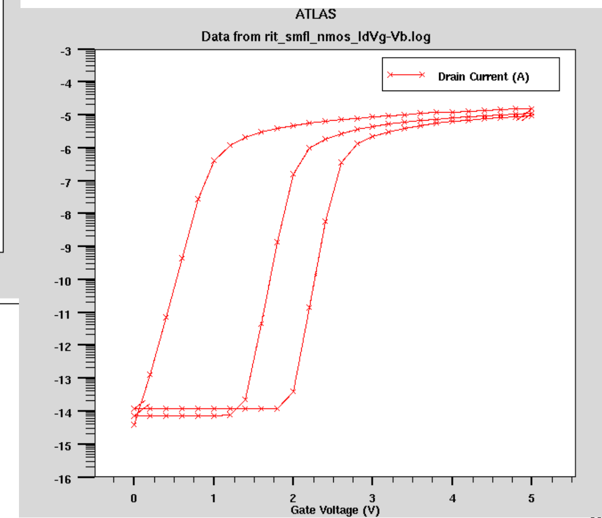
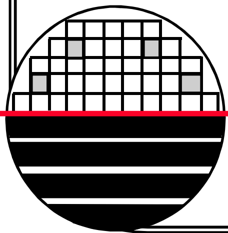
ATLAS GENERATED DEVICE CHARACTERISTICS









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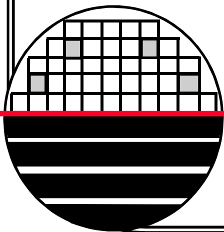
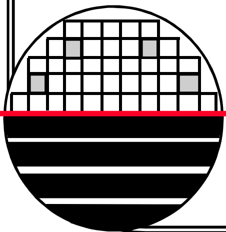
UTMOST GENEREATED SPICE PARAMETERS

NMOS PARAMETER DECK:
*2-27-2007 UTMOST EXTRACTIONS.MODEL CMOSN NMOS (LEVEL=49
VERSION=3.1 CAPMOD=2 MOBMOD=1+TOX=328.4E-10 XJ=3.5E-7 NCH=7.0E19
VTH0=0.8627+K1=0.5 K2=-0.0186 K3=80 WO=2.5E-6 NLX=1.740E-7+DVT0W=0
DVT1W=0 DVT2W=-0.032 DVT0=2.2 DVT1=0.53 DVT2=0.1394+U0=670 UA=2.25E-9
UB=5.87E-19 UC=-4.65E-11 VSAT=80000+A0=1 AGS=0 B0=0 B1=0 KETA=-0.047
A1=0 A2=1+RDSW=0 PRWG=0 PRWB=0 WR=1 WINT=2.58E-8 LINT=1.86E-8+XL=0
XW=0 DWG=0 DWB=0 VOFF=-0.06464 NFACTOR=1.3336+CIT=0 CDSC=0.00024
CDSCD=0 CDSCB-0 ETA0=0.08 ETAB=-0.07+DSUB=0.56 PCLM=1.39267
PDIBLC1=0.39 PDIBLC2=0.0086 PDIBLCB=0 +DROUT=0.19093 PSCBE1=4.00E8
PSCBE2=6E-6 PVAG=0 DELTA=0.01 PRT=0+UTE=-1.5 KT1=0 KT1L=0 KT2=0
UA1=4.3E-9 UB1=-7.6E-18+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0
WWN=1+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0+XPART=0 +CGD0=1.99E-10
CGS0=1.99E-10 CGB0=5.75E-10 CJ=4.23E-4+PB=0.99 MJ=0.4496 CJSW=3.83
PBSW=0.1083 MJSW=0.1084+PVTH0=0.02128 PRDSW=-16.155 PK2=0.0253
WKETA=0.01886 LKETA=0.0205)**



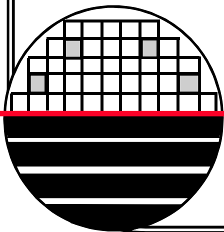
UTMOST GENEREATED SPICE PARAMETERS FROM ATHENA SIMULATED DEVICE CHARACTERISTICS

PMOS PARAMETER DECK:
2-27-2007 UTMOST EXTRACTIONS.MODEL CMOSP PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1+TOX=328.7E-10 XJ=3.5E-7 NCH=3.0E19 VTH0=-0.6322+K1=0.6423 K2=-0.0856046 K3=80 K3B=0 WO=2.0E-6 NLX=1.0E-7+DVT0W=0 DVT1W=0 DVT2W=-0.032 DVT0=1.5 DVT1=0.50 DVT2=-0.0193+U0=187.362 UA=1.1762E-9 UB=1.0E-22 UC=5.003E-3 VSAT=4.835E6+A0=3.9669 AGS=0 B0=0 B1=0 KETA=-0.0385 A1=0.19469 A2=0.40150+RDSW=0 PRWG=0 PRWB=0 WR=1 WINT=1.67E-8 LINT=3.150E-7+XL=0 XW=0 DWG=0 DWB=0 VOFF=-0.06464 NFACTOR=1.3336+CIT=0 CDSC=0.00024 CDSCD=0 CDSCB=0 ETA0=0.08 ETAB=-0.07+DSUB=0.56 PCLM=1.39267 PDIBLC1=0 PDIBLC2=1E-5 PDIBLCB=0 +DROUT=0.19093 PSCBE1=4E8 PSCBE2=6E-6 PVAG=0 DELTA=0.01 PRT=0+UTE=-1.5 KT1=0 KT1L=0 KT2=0 UA1=4.3E-9 UB1=-7.6E-18+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0+XPART=0 +CGD0=2.4E-10 CGS0=2.4E-10 CGB0=5.75E-10 CJ=7.27E-4+PB=0.97 MJ=0.496 CJSW=3.115 PBSW=0.99 MJSW=0.2654+PVTH0=0.00942 PRDSW=-231.3 PK2=1.397 WKETA=1.863 LKETA=5.729)



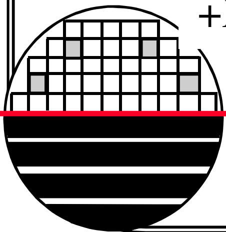
UTMOST GENERATED SPICE DECK FROM MEASURED SMFL CMOS PROCESS DEVICE CHARACTERISTICS

```
*1-15-2007 FROM ROB SAXER UTMOST EXTRACTIONS
.MODEL RITSMFLN49 NMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=310E-10 XJ=9.0E-7 NCH=8.2E16 VTH0=1.026
+K1=1.724 K2=-0.1212 K3=0 K3B=0 WO=2.5E-6 NLX=4.80E-9
+DVT0W=0 DVT1W=0 DVT2W=-0.032 DVT0=0.1466 DVT1=0.038 DVT2=0.1394
+U0=687.22 UA=2.34E-9 UB=-1.85E-18 UC=-1.29E-11 VSAT=1.64E5
+A0=0.4453 AGS=0 B0=0 B1=0 KETA=-0.0569 A1=0 A2=1
+RDSW=376.9 PRWG=0 PRWB=0 WR=1 WINT=2.58E-8 LINT=1.86E-8
+XL=0 XW=0 DWG=0 DWB=0 VOFF=-0.1056 NFACTOR=0.8025
+CIT=0 CDSC=-2.59E-5 CDSCD=0 CDSCB-0 ETA0=0 ETAB=0
+DSUB=0.0117 PCLM=0.6184 PDIBLC1=0.0251 PDIBLC2=0.00202 PDIBLCB=0
+DROUT=0.0772 PSCBE1=2.77E9 PSCBE2=3.11E-8 PVAG=0 DELTA=0.01 PRT=0
+UTE=-1.5 KT1=0 KT1L=0 KT2=0 UA1=4.3E-9 UB1=-7.6E-18
+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1
+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0
+XPART=0 +CGD0=1.99E-10 CGS0=1.99E-10 CGB0=5.75E-10 CJ=4.23E-4
+PB=0.99 MJ=0.4496 CJSW=3.83 PBSW=0.1083 MJSW=0.1084
+PVTH0=0.02128 PRDSW=-16.155 PK2=0.0253 WKETA=0.01886 LKETA=0.0205)
```



UTMOST GENERATED SPICE DECK FROM MEASURED SMFL CMOS PROCESS DEVICE CHARACTERISTICS

```
*1-15-2007 FROM ROB SAXER UTMOST EXTRACTIONS
.MODEL RITSMFLP49 PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=310E-10 XJ=8.8E-7 NCH=3.1E16 VTH0=-1.166
+K1=0.3029 K2=0.1055 K3=0 K3B=0 WO=2.5E-6 NLX=2.01E-8
+DVT0W=0 DVT1W=0 DVT2W=-0.032 DVT0=2 DVT1=0.5049 DVT2=-0.0193
+U0=232.53 UA=4E-9 UB=-2.26E-18 UC=-6.80E-11 VSAT=4.40E4
+A0=0.6045 AGS=0 B0=0 B1=0 KETA=-0.0385 A1=0 A2=1
+RDSW=1230 PRWG=0 PRWB=0 WR=1 WINT=1.67E-8 LINT=6.50E-8
+XL=0 XW=0 DWG=0 DWB=0 VOFF=-0.0619 NFACTOR=1.454
+CIT=0 CDSC=-4.30E-4 CDSCD=0 CDSCB-0 ETA0=0 ETAB=0
+DSUB=0.2522 PCLM=5.046 PDIBLC1=0 PDIBLC2=1E-5 PDIBLCB=0
+DROUT=0.2522 PSCBE1=2.8E9 PSCBE2=2.98E-8 PVAG=0 DELTA=0.01 PRT=0
+UTE=-1.5 KT1=0 KT1L=0 KT2=0 UA1=4.3E-9 UB1=-7.6E-18
+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1
+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0
+XPART=0 +CGD0=2.4E-10 CGS0=2.4E-10 CGB0=5.75E-10 CJ=7.27E-4
+PB=0.97 MJ=0.496 CJSW=3.115 PBSW=0.99 MJSW=0.2654
+PVTH0=0.00942 PRDSW=-231.3 PK2=1.397 WKETA=1.863 LKETA=5.729)
```

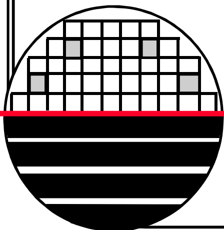


SMFL CMOS PROCESS "HOT & COLD" SPICE MODELS

All parameters the same except those listed are changed to give more transistor current for the hot models:

.model **hot** nmos (LEVEL = 11 VERSION = 3.1
TOX = 2.70E-8 **VTH0**= 0.926 **U0** = 750 **RDSW** = 330)
.model **hot** pmos (LEVEL = 11 VERSION = 3.1
TOX = 2.70E-8 **VTH0**= -1.066 **U0** = 250 **RDSW** = 1.00E3)

.model **cold** nmos (LEVEL = 11 VERSION = 3.1
TOX = 3.50E-8 **VTH0**= 1.126 **U0** = 620 **RDSW** = 410)
.model **cold** pmos (LEVEL = 11 VERSION = 3.1
TOX = 3.50E-8 **VTH0**= -1.266 **U0** = 200 **RDSW** = 1.45E3)



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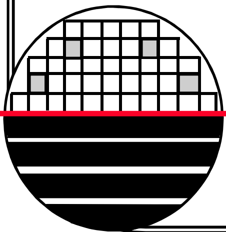
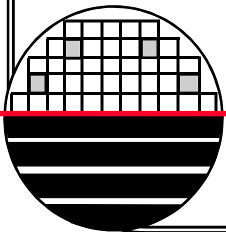


HOMEWORK – SPICE MOSFET MODELS

1. Write an abstract that summarizes the main ideas presented in this document.



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