

PMOS Digital Testing at Rochester Institute of Technology

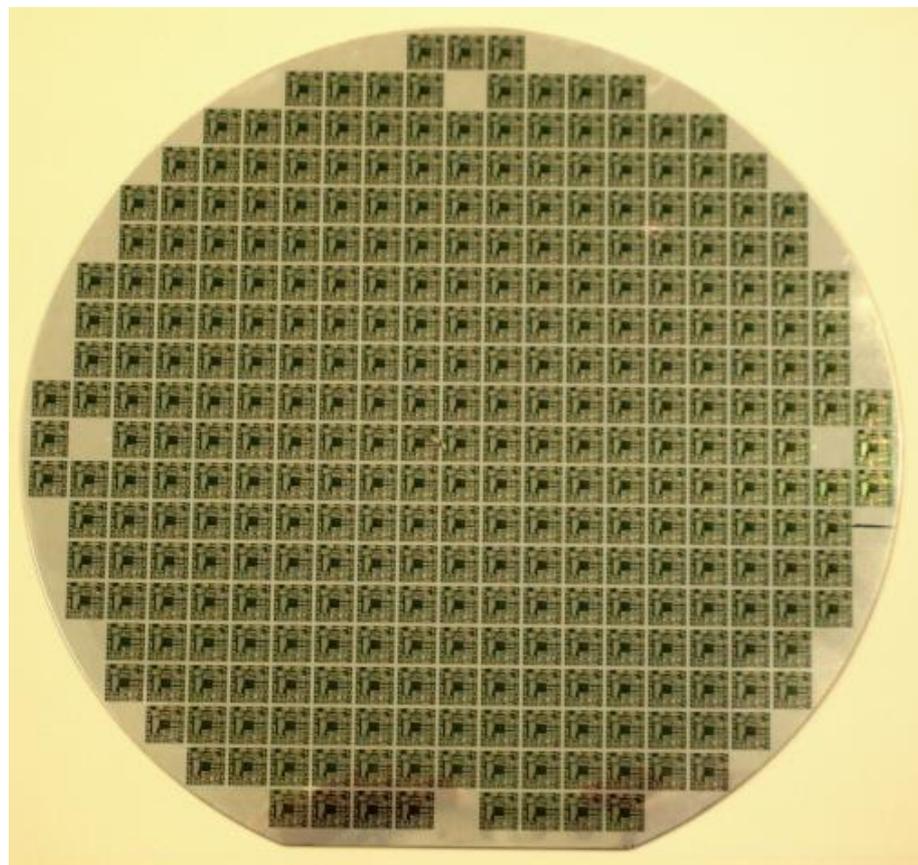
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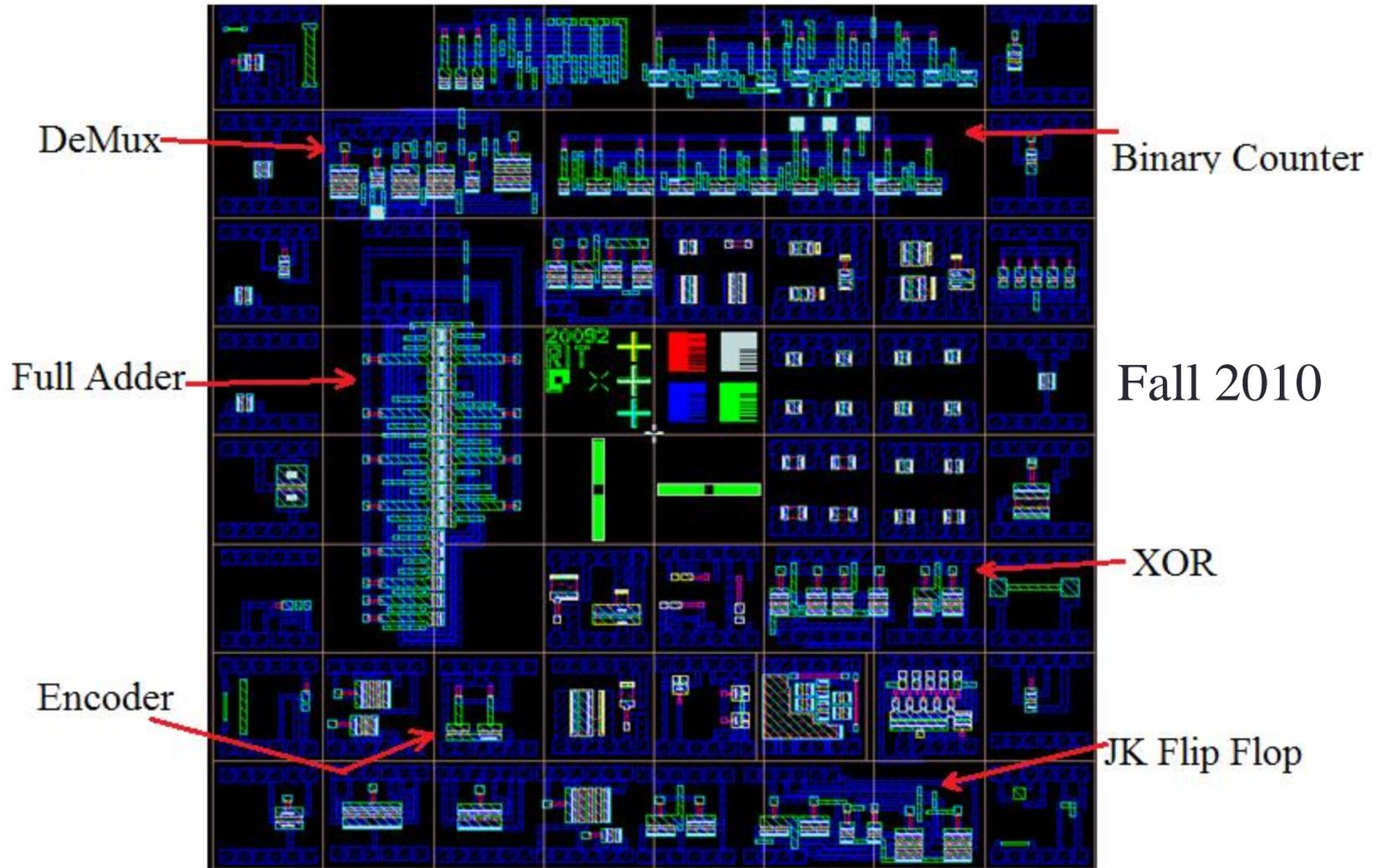
Revised 7-11-2014 PMOS_Digital_Test.ppt

OUTLINE

- PMOS Test Chip
- Analog Discovery Module
- Test Equipment
- Camera, Probes, etc.
- Connecting to Module
- Set up Logic Analyzer
- 3.3 to -5 V Level Shifter
- Set Up Inputs
- Output Data
- NOR and Full Adder



PMOS TEST CHIP

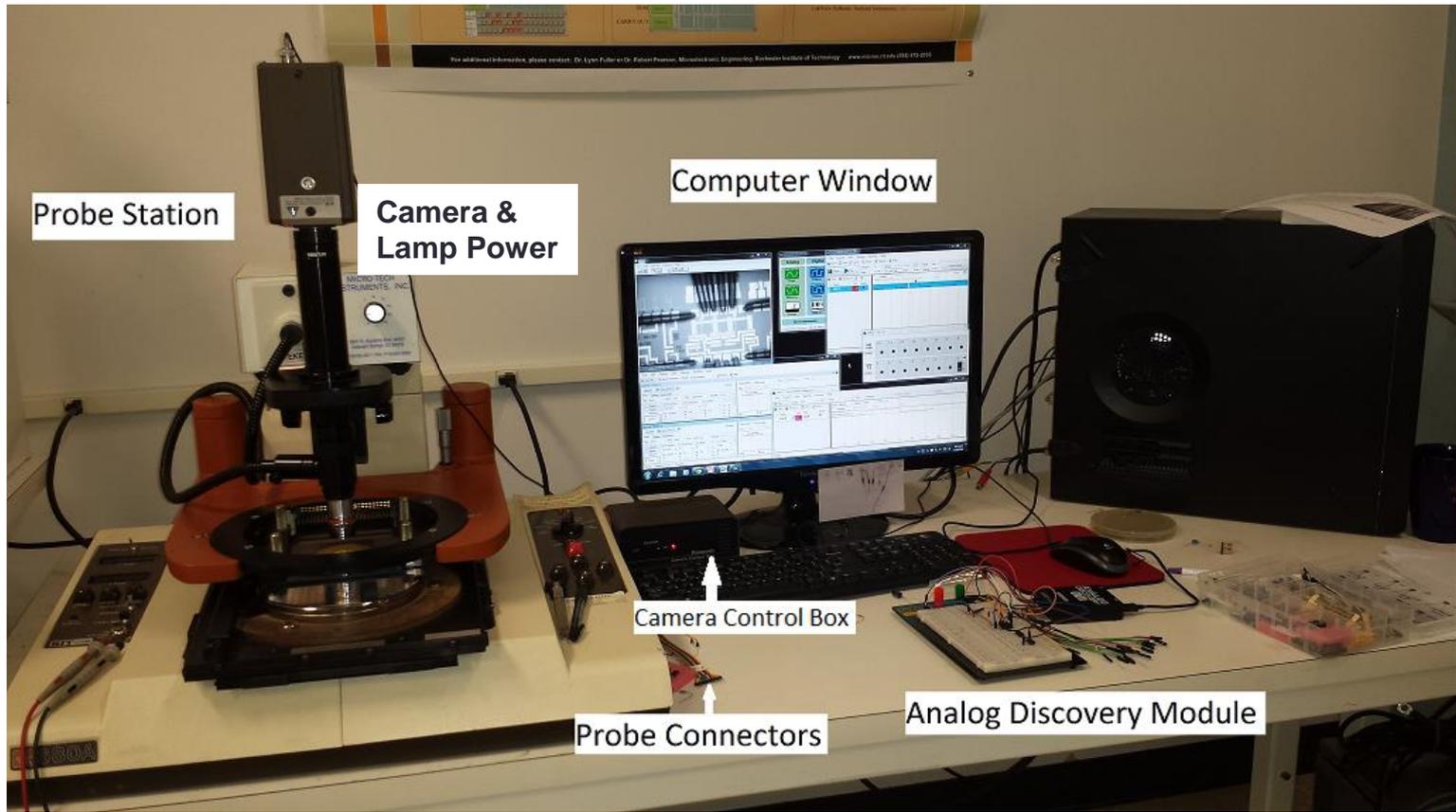


PMOS Factory – Digital Testing

Analog Discovery Module has the following capabilities

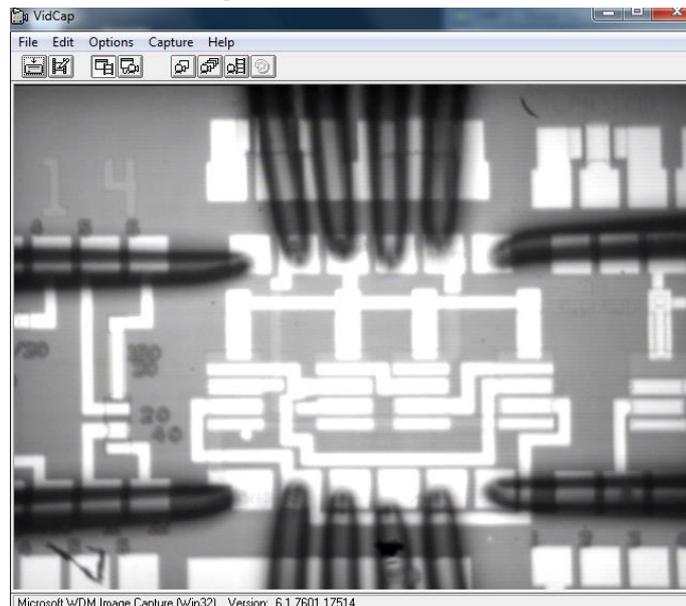
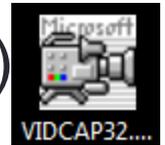
- Two channel oscilloscope
- Two channel arbitrary function generator ($\pm 5V$)
- 16-channel digital logic analyzer (+3.3V CMOS)
- 16-channel pattern generator (+3.3V CMOS)
- 16-channel virtual digital I/O including buttons, switches and LEDs
- Two input/output digital trigger signals (3.3V CMOS);
- Two power supplies (+5V at 50mA, -5V at 50mA).
- Single channel voltmeter (AC, DC, $\pm 25V$);
- Network analyzer – Bode, Nyquist, Nichols transfer diagrams Range: 1Hz to 10MHz;
- Spectrum Analyzer

Digital Testing Hardware Station

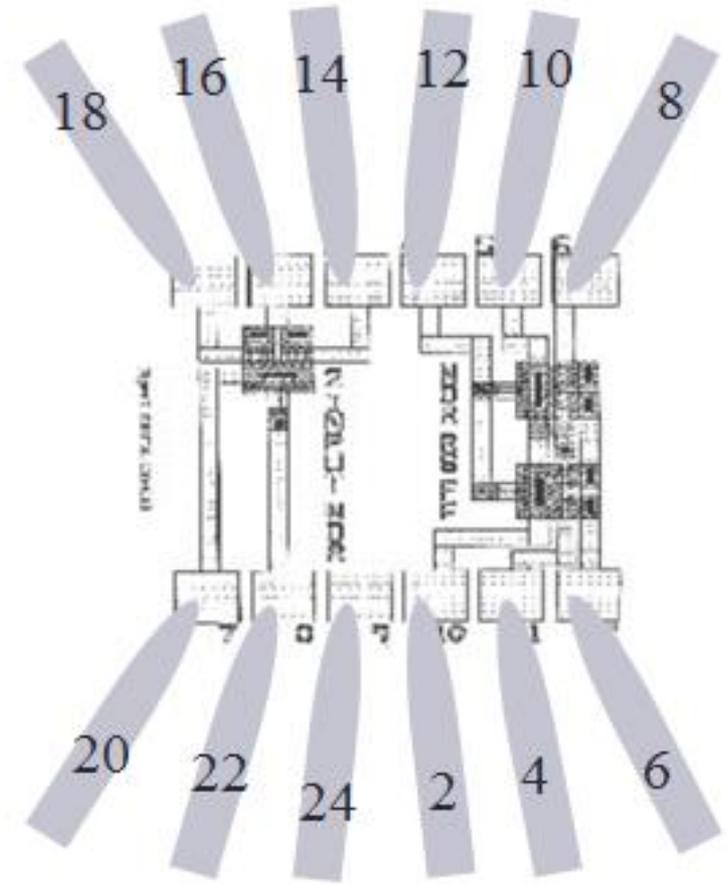
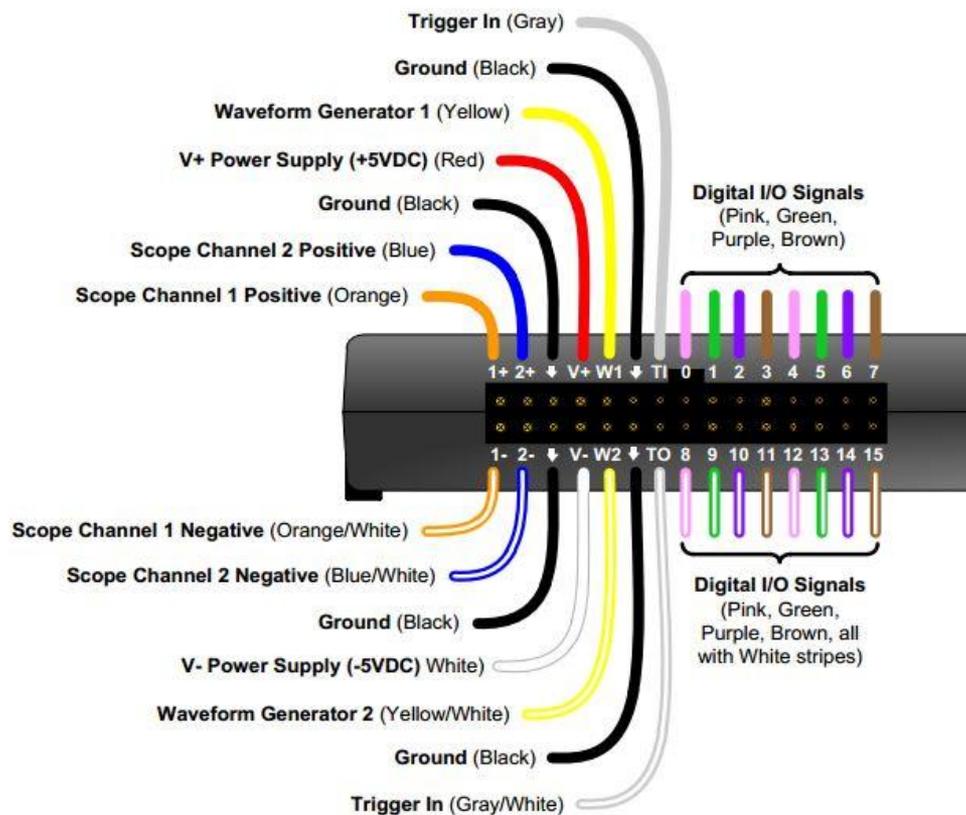


Wafer Loading

- Turn on the camera control box and lamp power, shown in the previous slide.
- Open the camera capture program (VIDCAP32.EXE) from the desktop of the computer
- Align the wafer with the probes, then lower to make contact.



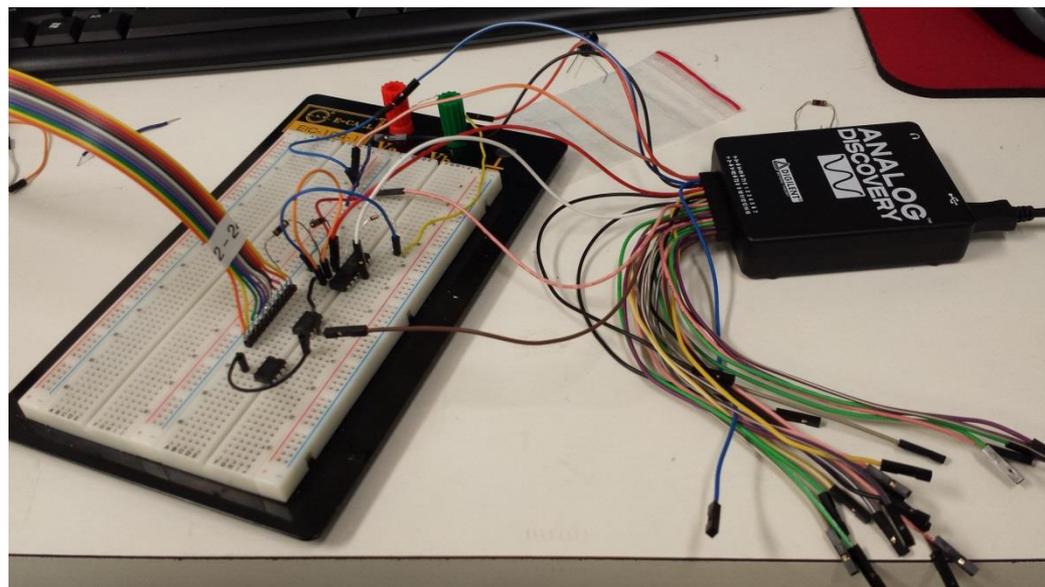
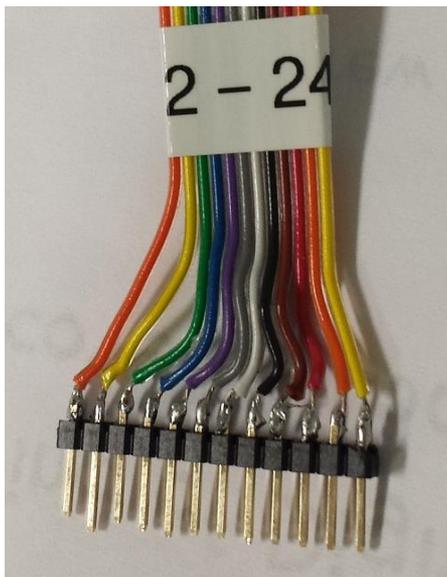
Analog Discovery Pin layout – Probe card connections



Probe Card Pin Numbers

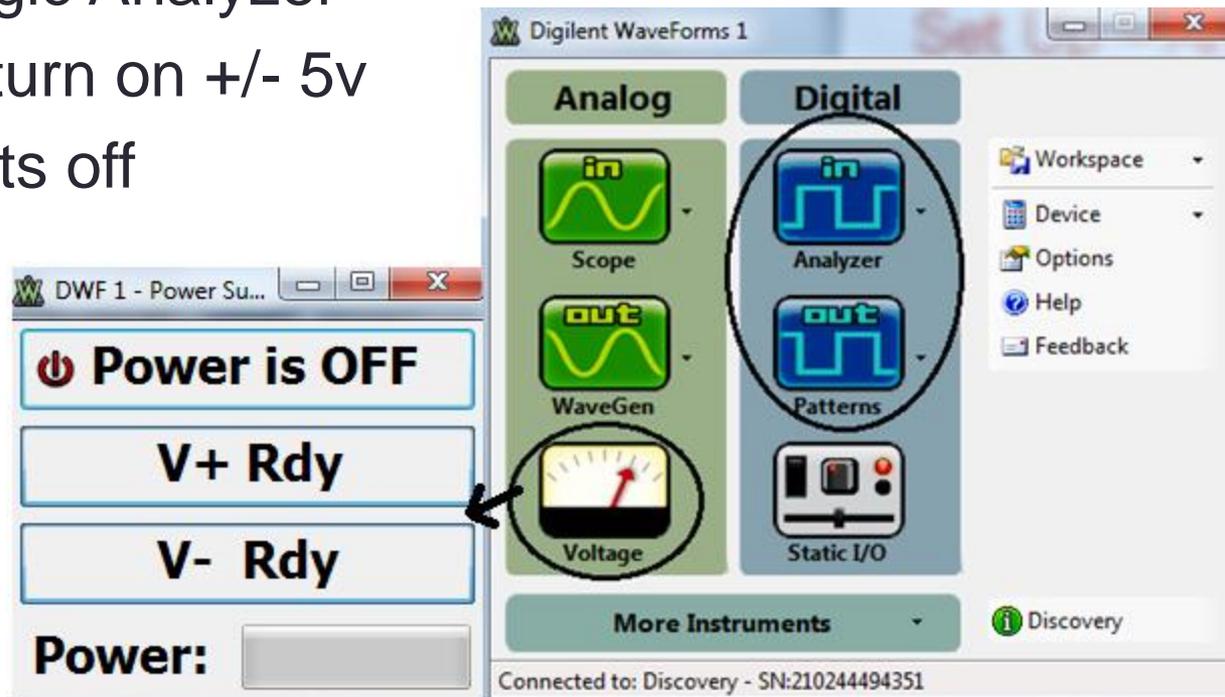
Digital Testing Station - Breadboard

- Pins 2 – 24 on the probe card are connected via ribbon cable (Pin 2 left, Pin 24 Right). Even numbers only 2,4,6,8,10,12,14,16,18,20,22,24



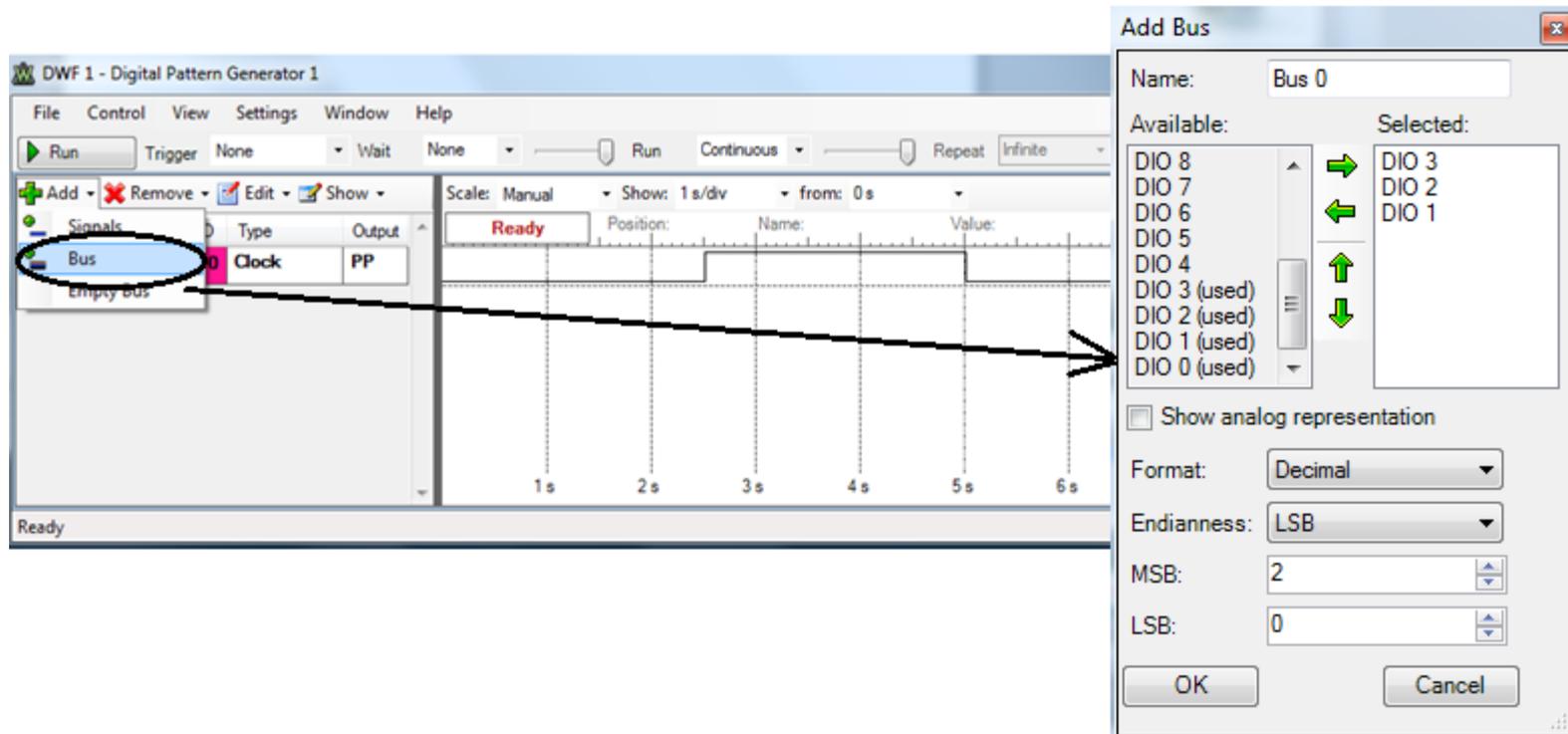
Set Up – Analog Discovery

- Open the WaveForms program by double clicking this icon on the desktop
- Then open the Digital Pattern Generator and Logic Analyzer
- Open Voltage to turn on +/- 5v Power supply (shuts off automatically if too much current is Drawn)



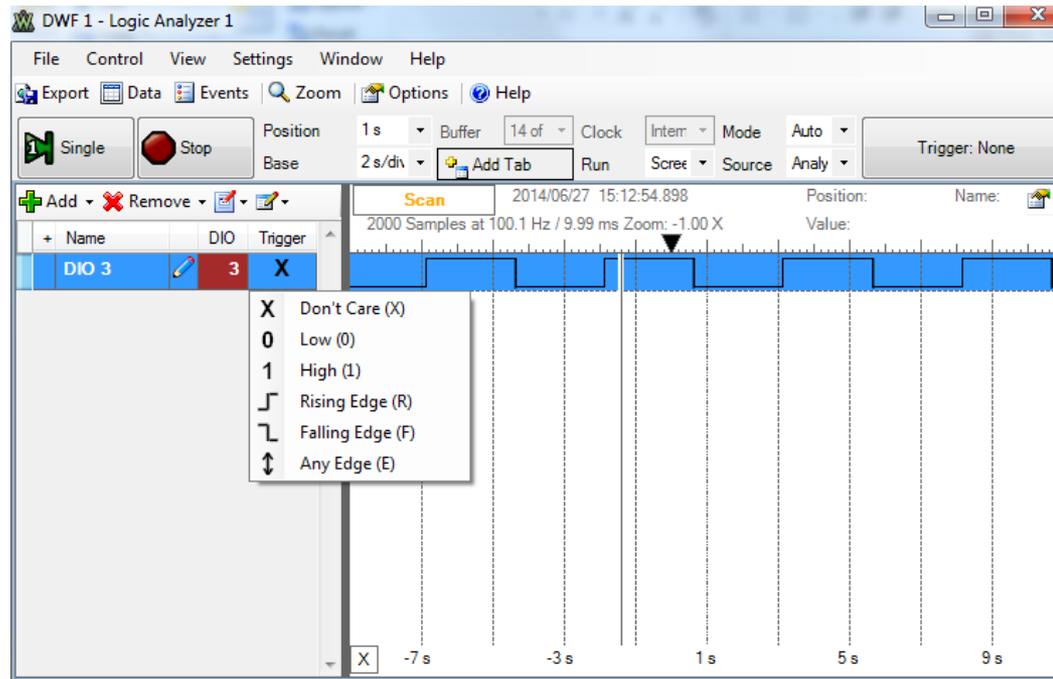
Digital Pattern Generator

- Add Signal – Edit parameters to show 1 s/div
- Outputs are numbered and color coded to the pin layout
- DIO# = Digital Input/Output Pin Number (0-16)



Logic Analyzer Setup

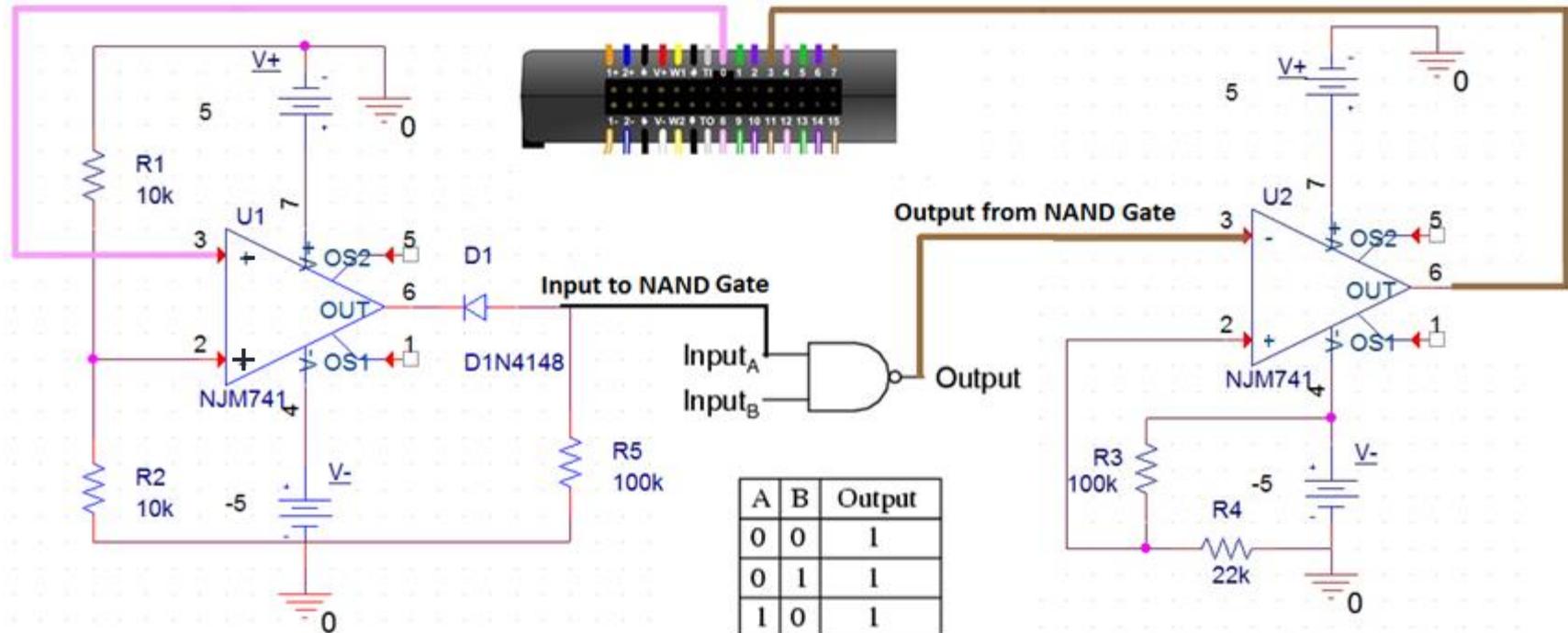
- Adding signals is the same as the Pattern Generator
- Logic Analyzer reads digital signals which can be set to trigger by any edge (E) or don't care (X)



PMOS Digital Testing

- The Logic Analyzer interprets a “high” as +3.3 V, and “low” as 0 V, in PMOS logic “high” is – 5 V and “low” is 0V.
- An operational amplifier (Op Amp) is used to convert the digital pattern generator 0 to +3.3 V signal to 0 to -5V that becomes the input to the PMOS logic circuit.
- A similar Op Amp circuit is used to convert the PMOS logic output to logic levels that can be interpreted by the logic analyzer. The logic analyzer interprets positive voltages (more than +1.65V) as logic high and lower voltages (including negative voltages) as logic low.
- These circuits are shown on the next slide and are used for each individual PMOS logic gate input or output.

PMOS Digital Testing Circuit

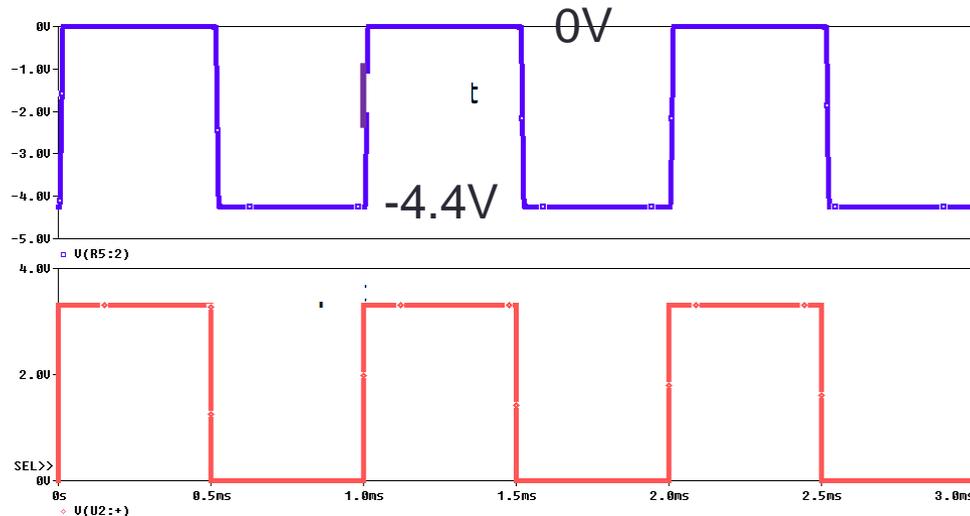


This comparator has +2.5 volt at the non-inverting input. Thus if the signal generator is low (0V) the Op Amp output goes high (+5). The diode is reverse biased and the signal to the PMOS logic low (0V). If the signal generator is high (3.3V) the Op Amp output goes low (-5). The diode is forward biased (0.6V) thus the signal to the PMOS logic gate is high (-4.4V).

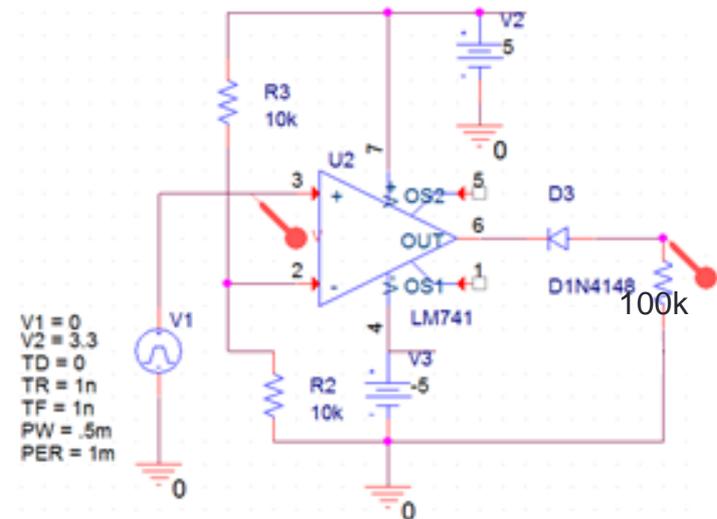
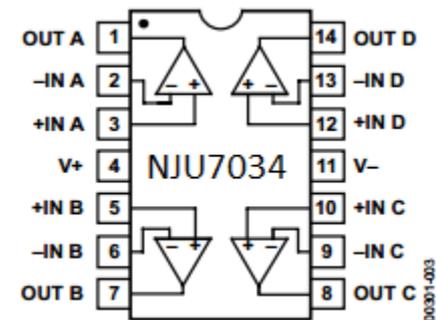
This comparator has -1 volt at the non-inverting input. Thus if the logic out is low (0V) the logic analyzer sees a -5 or low signal. If the logic out is high (-5) the logic analyzer sees a +5 or high signal.

3.3 V to -5 V Digital Shifter

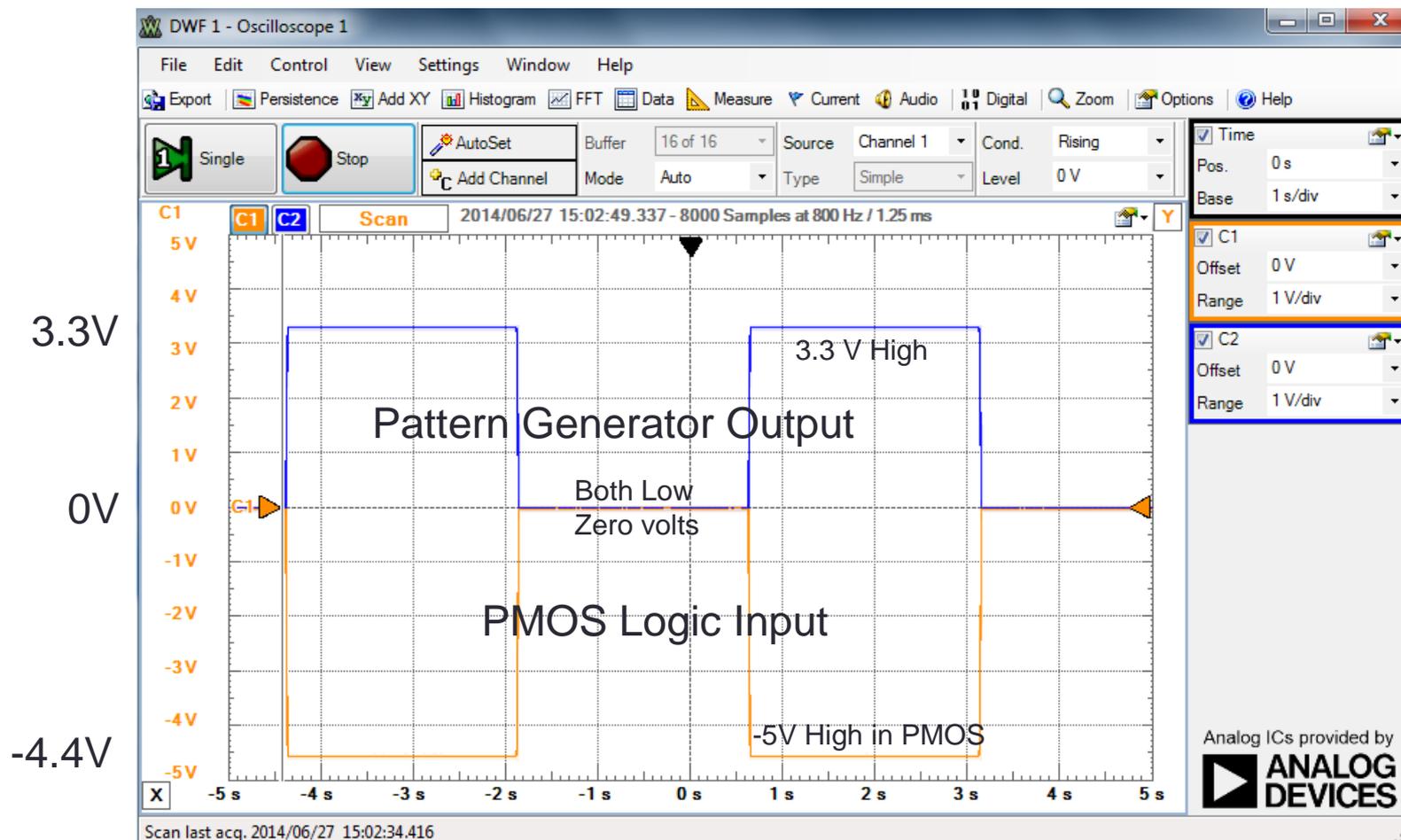
- Required for each individual input using high input impedance, rail-to-rail, Operational Amplifiers such as the NJU7034D



This comparator has +2.5 volt at the non-inverting input. Thus if the signal generator is low (0V) the Op Amp output goes high (+5). The diode is reverse biased and the signal to the PMOS logic low (0V). If the signal generator is high (3.3V) the Op Amp output goes low (-5). The diode is forward biased (0.6V) thus the signal to the PMOS logic gate is high (-4.4V).



3.3 V to -5 V Digital shifter



Data Acquisition

- Select Run on the Logic Analyzer and Pattern Generator
- Data can be exported to Excel from the Logic Analyzer on the top left corner

The image shows two software windows side-by-side. The left window is titled 'DWF 1 - Logic Analyzer 1' and the right is 'DWF 1 - Digital Pattern Generator 1'. Both windows have a menu bar with 'File', 'Control', 'View', 'Settings', 'Window', and 'Help'. In the Logic Analyzer window, the 'Export' button in the 'File' menu and the 'Run' button in the 'Control' section are circled. In the Digital Pattern Generator window, the 'Run' button in the 'Control' section is circled. The Digital Pattern Generator window also features a table of DIO settings and a timing diagram.

Name	DIO	Type	Output
Bus 0		Binary Co...	PP
[3] MSB	4		
[2]	2		
[1]	1		
[0] LSB	0		

The timing diagram on the right shows a signal over 6 seconds. The signal is high for the first 2 seconds, then low for the next 2 seconds, and then high for the last 2 seconds. The scale is 100k. The position is 8.34 s and the value is Ready.

Exporting Data to Excel

- Raw data can be exported to a .csv (comma - separated values) excel spreadsheet file using the export button in the logic analyzer

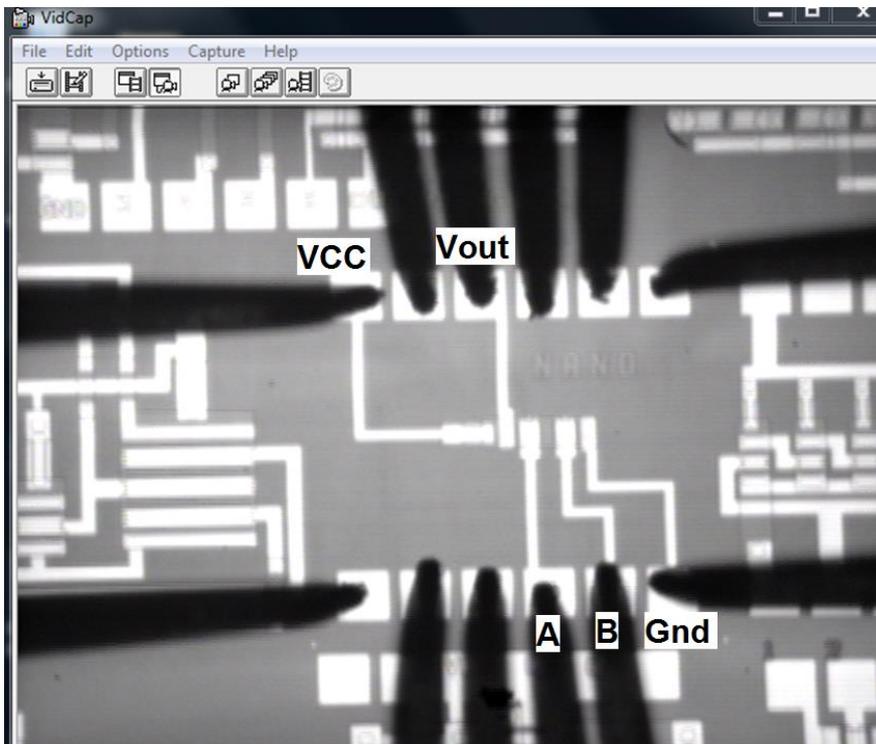
The screenshot illustrates the process of exporting data from the Digilent WaveForms Logic Analyzer to an Excel spreadsheet. The 'Export' button in the top menu is circled, and an arrow points to the 'Analyzer Export' dialog box. The dialog shows the 'Comma Separated Values (*.csv)' type selected, and the 'Save Options' (Comments, Header, Label) are checked. The data table in the dialog shows the following values:

Time (s)	DIO 4	DIO 3
0.000	0	1
0.005	0	1
0.010	0	1
0.015	0	1
0.020	0	1
0.025	0	1
0.030	0	1
0.035	0	1

The resulting Excel spreadsheet is shown on the right, with the same data table. The spreadsheet has the following structure:

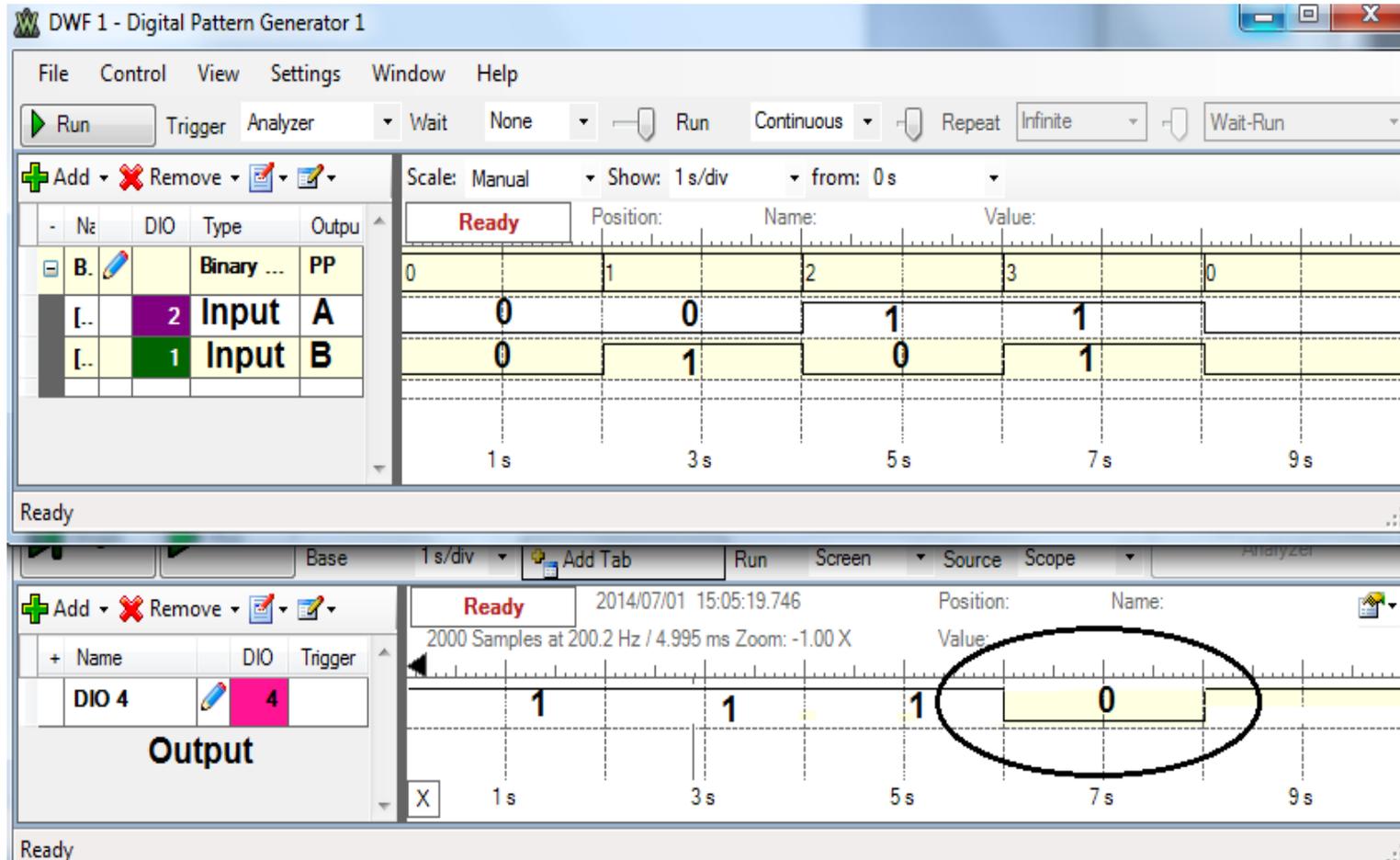
A1	#Title	
#Title	Digilent WaveForms Logic Analyzer Data	
#Device Name	Analog Discovery	
#Serial Number	SN:210244494351	
#Software Version	2.7.5	
Time (s)	DIO 4	DIO 3
0	0	1
0.005	0	1
0.01	0	1
0.015	0	1
0.02	0	1
0.025	0	1

Example: PMOS 2-Input NAND Gate



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

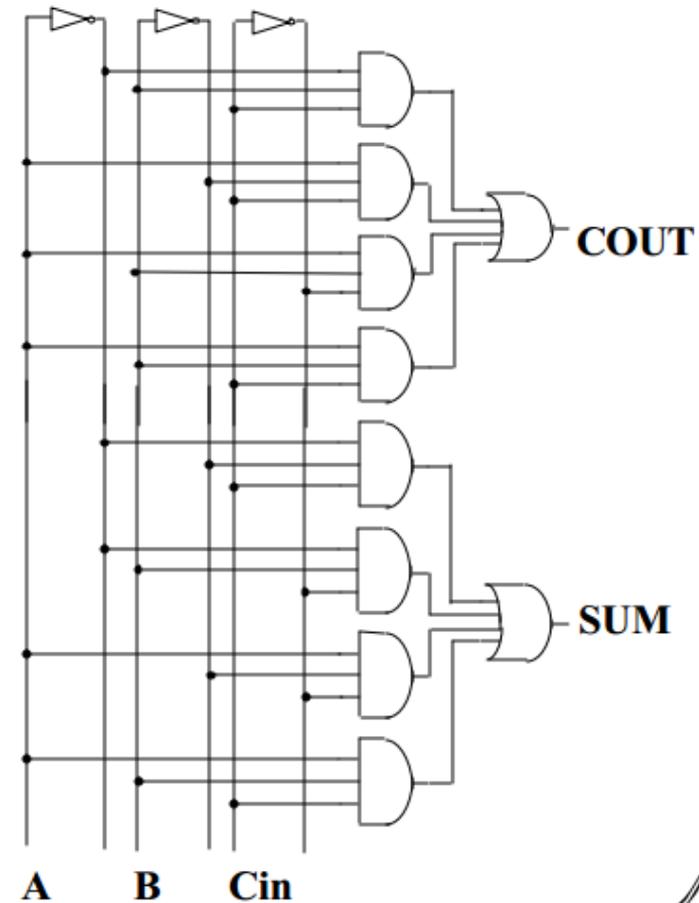
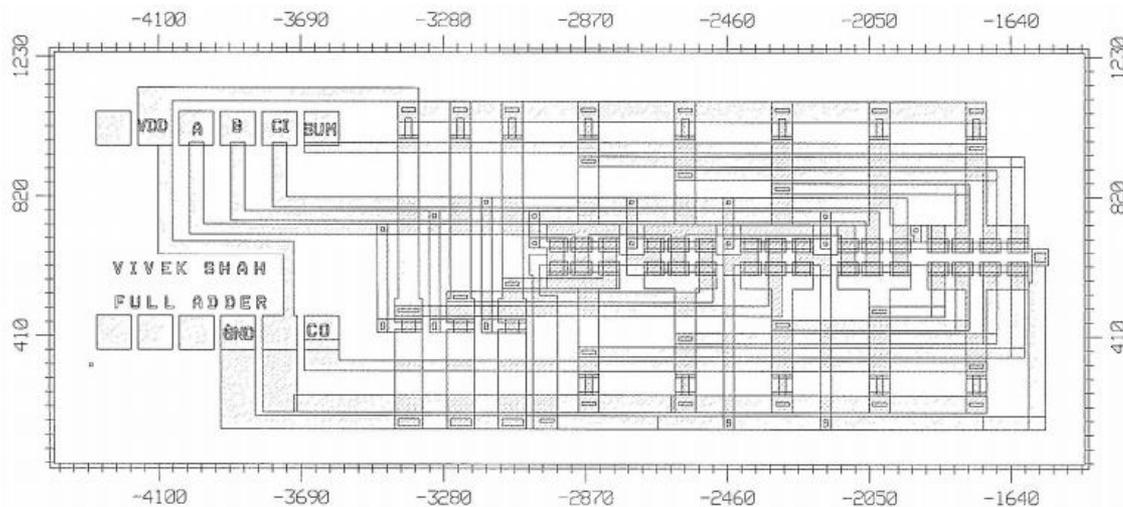
PMOS 2-Input NAND Gate Test Results



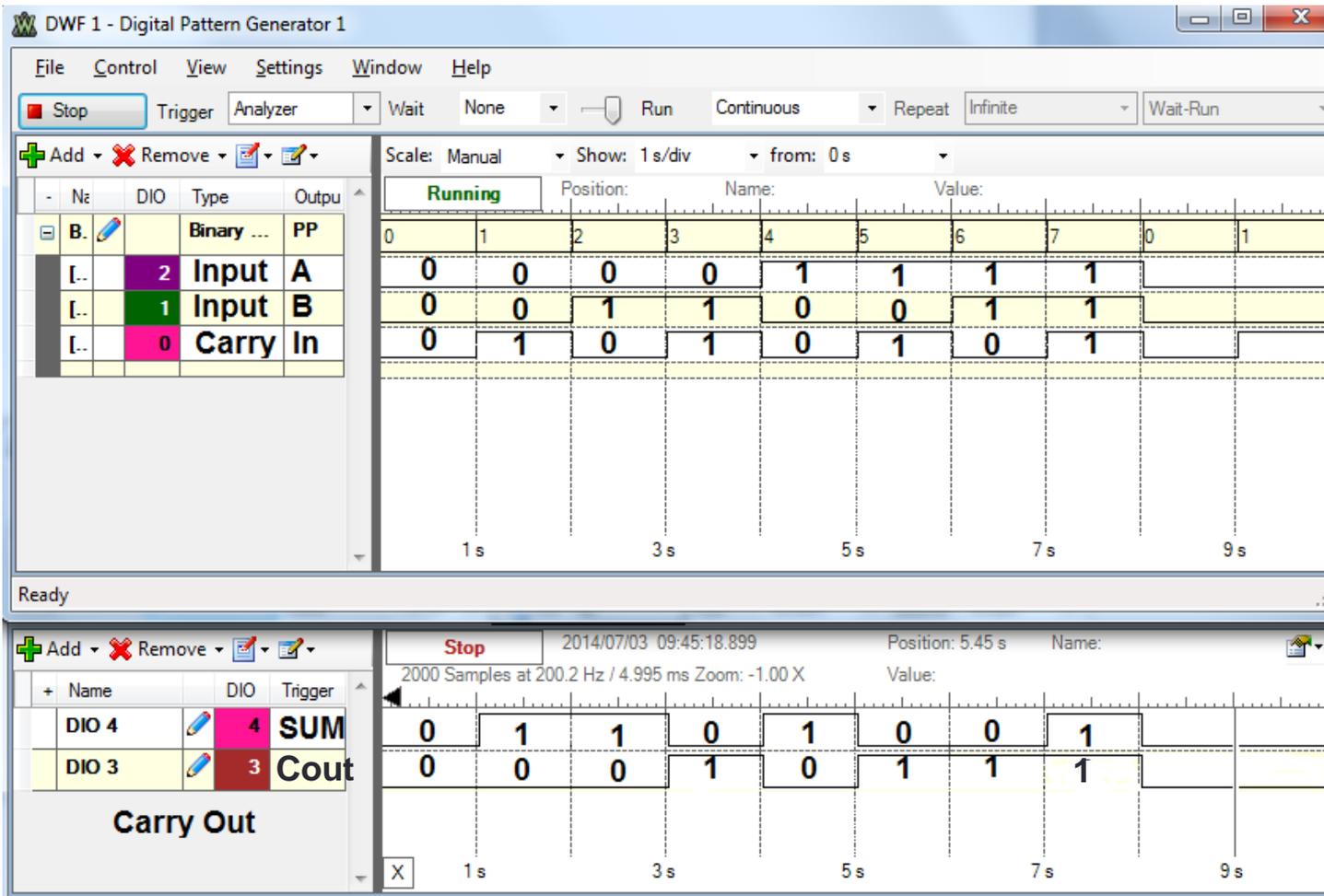
- PMOS logic high is -5 V and logic low is 0V

Example: PMOS Full Adder

A	B	CIN	SUM	COU
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



PMOS Full Adder Test Result



- PMOS logic high is -5 V and logic low is 0V

References

- Analog Discovery Website
 - <http://www.digilentinc.com/Products/Detail.cfm?Prod=ANALOG-DISCOVERY>
- Analog Discovery Manual
 - http://www.digilentinc.com/Data/Products/ANALOG-DISCOVERY/Discovery_TRM_RevB_1.pdf