RIT Metal Gate PMOS Process ROCHESTER INSTITUTE OF TECHNOLOGY MICROELECTRONIC ENGINEERING

PMOS 150mm PROCESS DETAILS

Dr. Lynn Fuller, Dr. Ivan Puchades

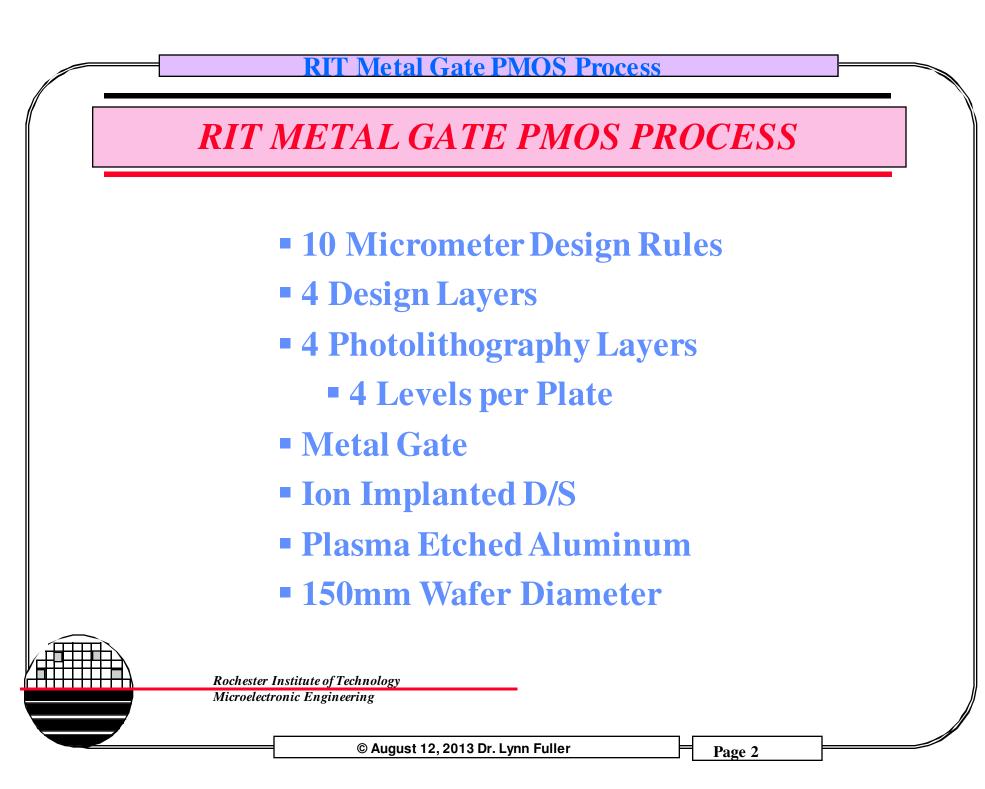
Webpage: http://people.rit.edu/lffeee Microelectronic Engineering Rochester Institute of Technology 82 Lomb Memorial Drive Rochester, NY 14623-5604 Tel (585) 475-2035 Fax (585) 475-5041 Email: Lynn.Fuller@rit.edu MicroE Webpage: http://www.rit.edu/kgcoe/ue/

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8-12-2013 pmos150.ppt



METAL GATE PMOS PROCESS

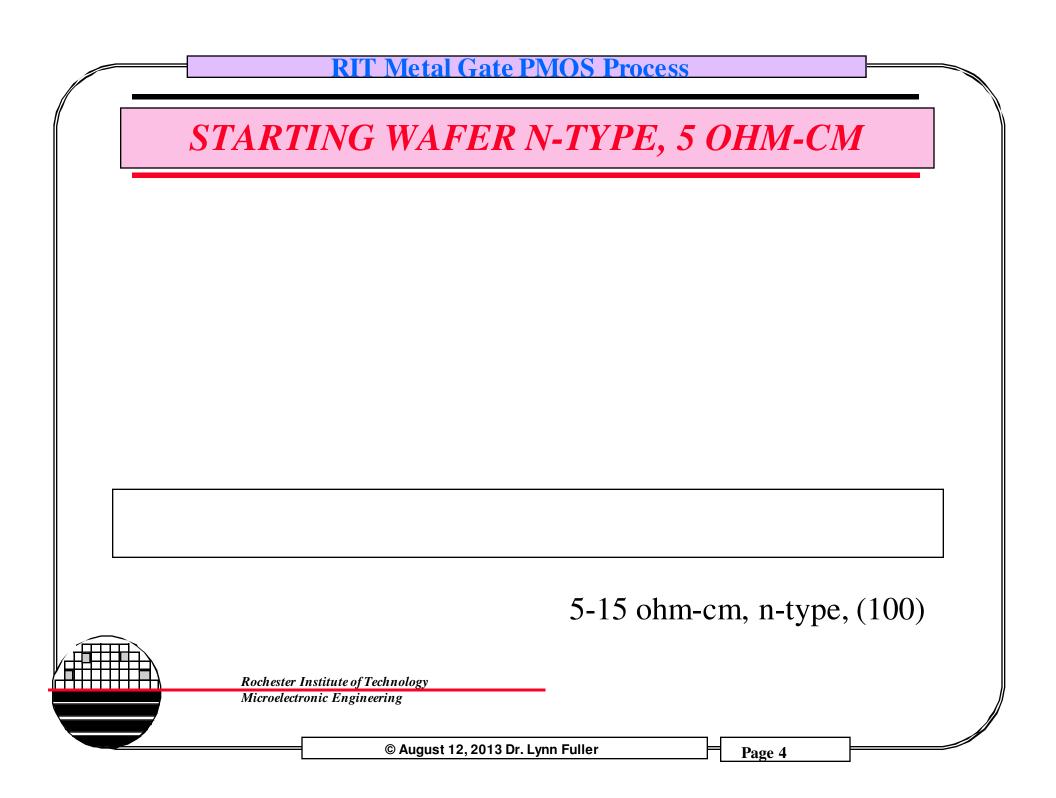
PMOS Versions 150

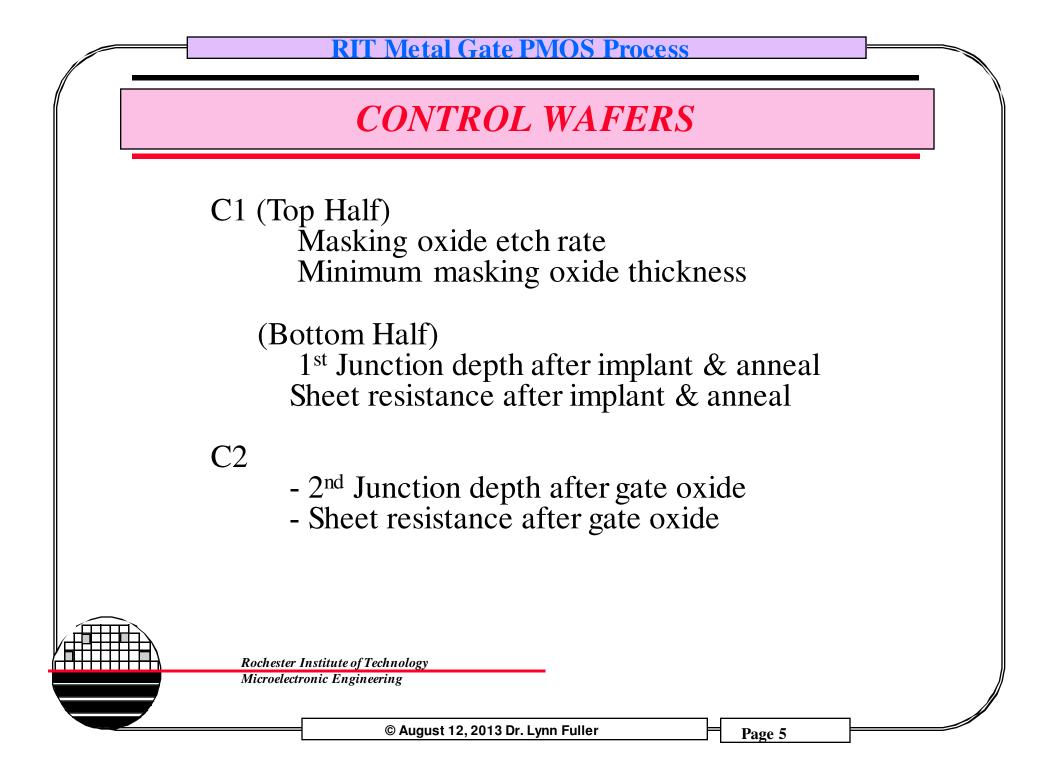
- 1. ID01 Scribe Wafers C1, C2, D1...DX
- 2. DE01 4 Point Probe C1, 5-15 ohm-cm
- 3. CL01 C1, C2, and All Device Wafers
- 4. OX06 6500Å, Tube 1, Recipe 406
- 5. PH03 PMOS Level 1, Diffusion
- 6. ET06 Step Etch C1, Etch C2 Bare
- 7. ET06 Etch All Device Wafers
- 8. ET07 Ash Device Wafers
- 9. CL01 RCA Clean All Wafers
- 10.IM01- B11, 75 KeV, All Wafers
- 11.OX06 4000Å Tube 1, Recipe 341
- 12.PH03 PMOS Level 2, Oxide
- 13.ET06 C1, C2 and All Device Wafers
- 14.DE01 4 Point Probe C1

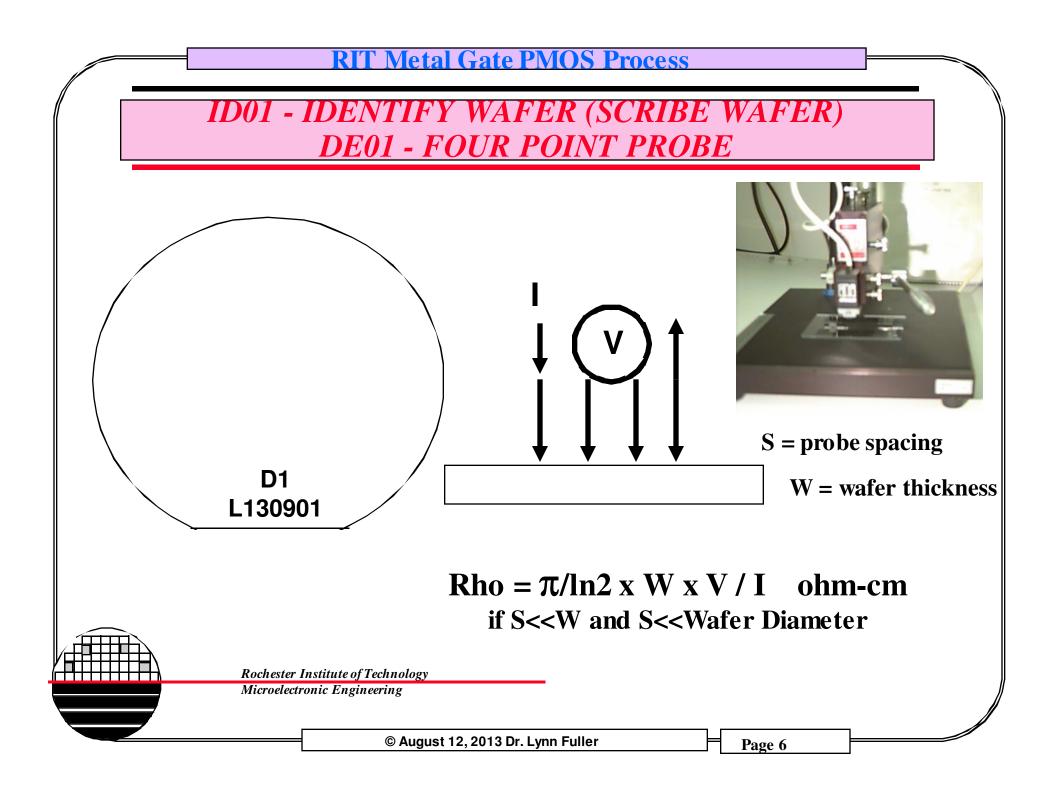
15.GRV1 Grove and Stain C1

16.ET07 Ash Device Wafers 17.CL01 C2 and All Device Wafers, 2 HF dips 18.OX05 Gate Ox, Tube 4, 700Å, Recipe 270 19.PH03 - PMOS Level 3, CC 20.ET06 C2 and All Device Wafers 21.ET07 Ash Device Wafers 22.DE01 4 pt probe C2 23.GRV1 Grove and Stain C2 24. CL01 All Device Wafers, Two HF dips 25.ME01 Sputter Metal All Device Wafers 10KÅ 26.PH03 - PMOS – Level 4, Metal 27.ET15 Etch Aluminum All Device Wafers 28.ET07 Ash Device Wafers 29.SI01 Sinter Device Wafers Tube 2, Recipe 101 30. TE01 Test Wafers

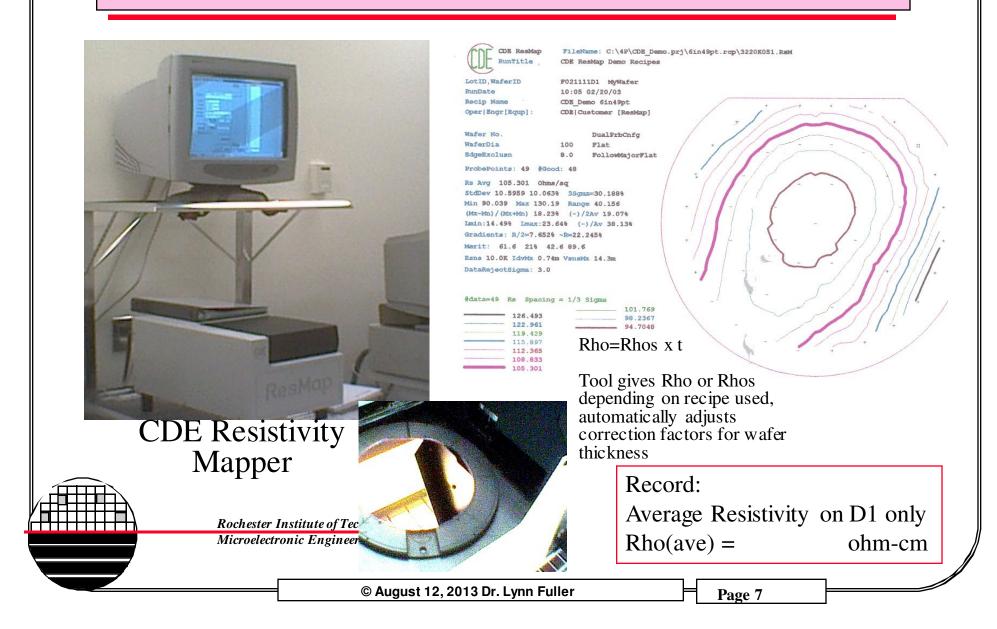
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DE01 - MEASURE WAFER RESISTIVITY



Metal Gate PMOS Process **RI**'

TENCORE SURF SCAN

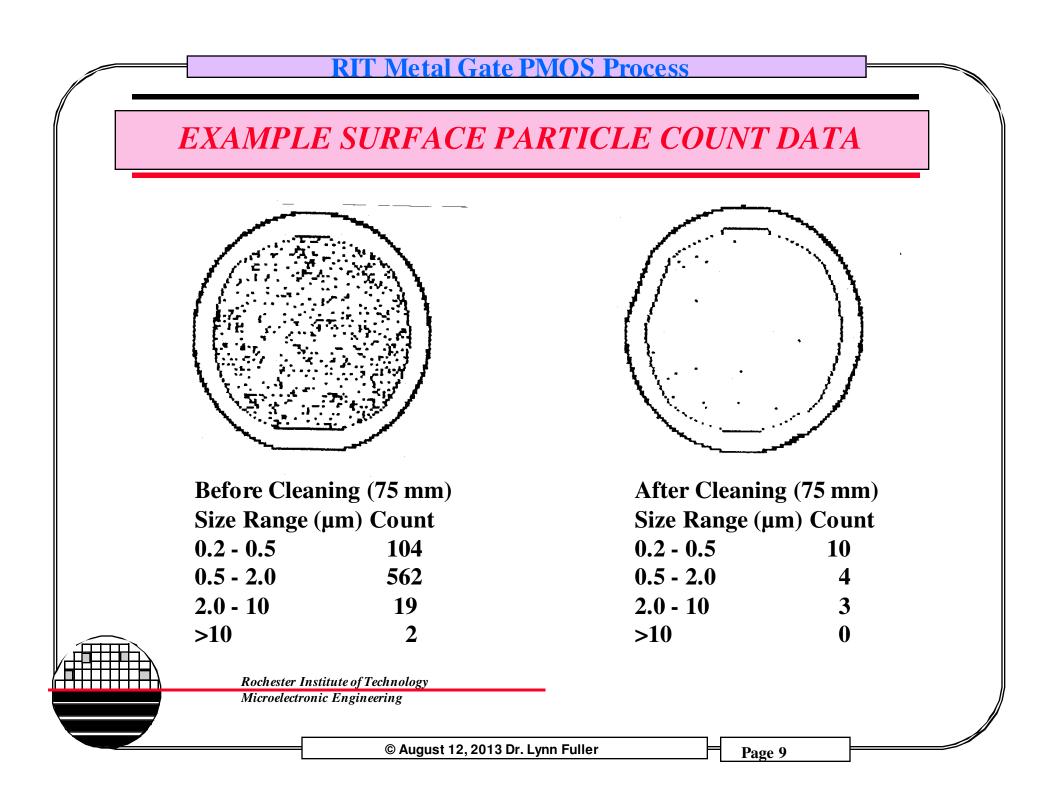
Gives total surface particle count and count in 4 bins <0.5, 0.5 to 2.0, 2.0-10, >10. Bin boundary can be selected. Edge exclusion eliminated count from near the edge of the wafer.

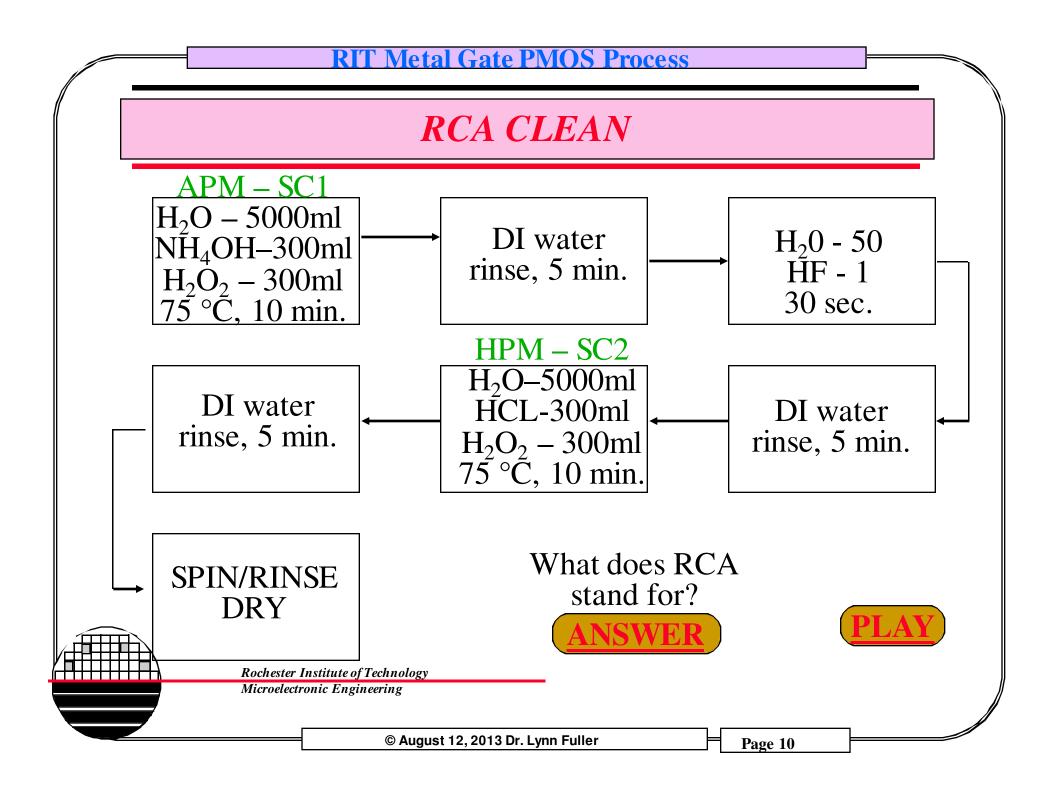




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RCA CLEAN TOOLS

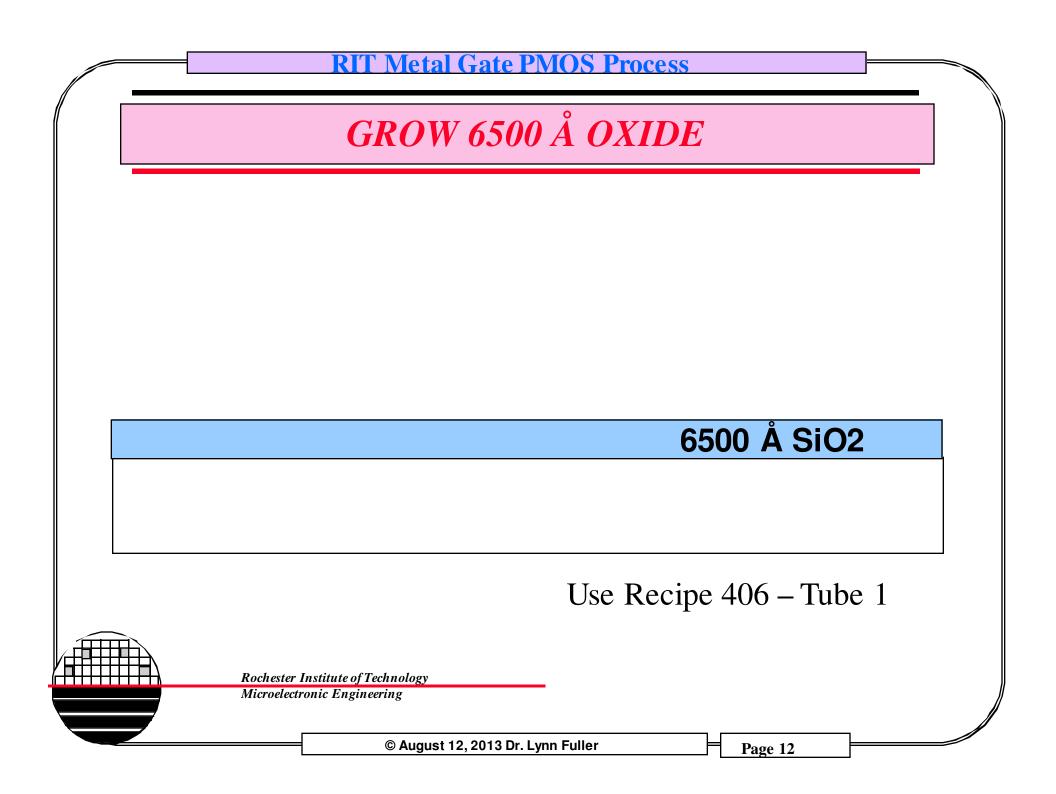
RCA Bench Spin/Rinse/Dry Tool

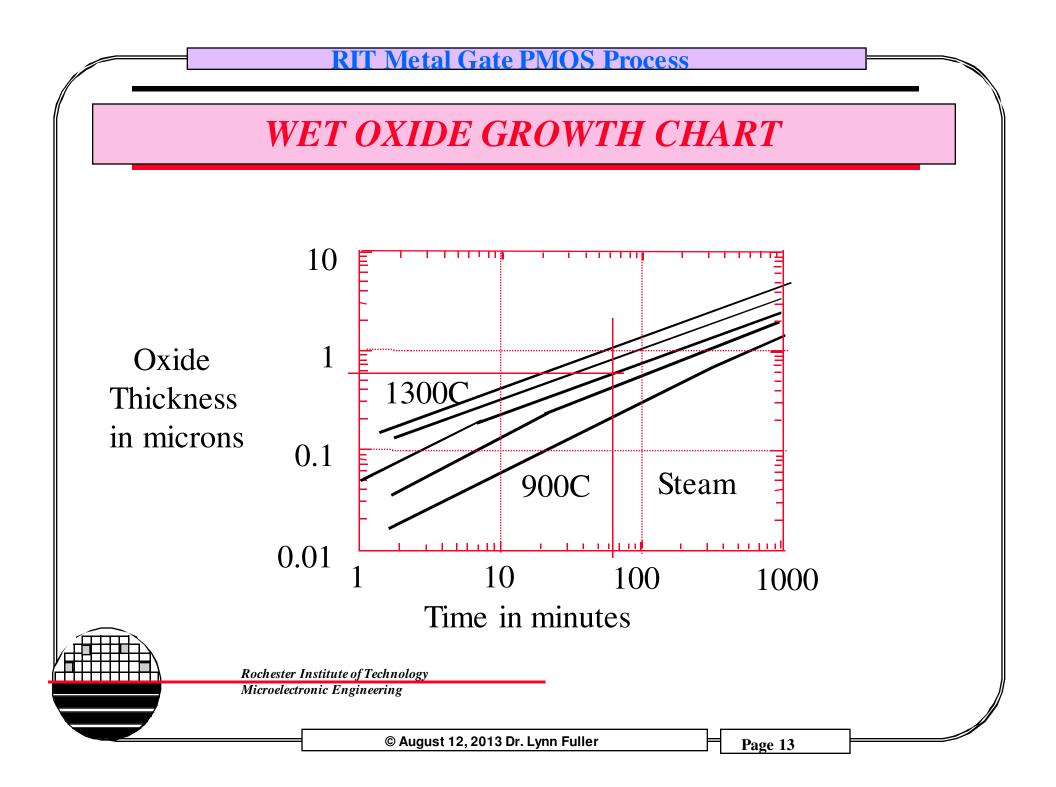


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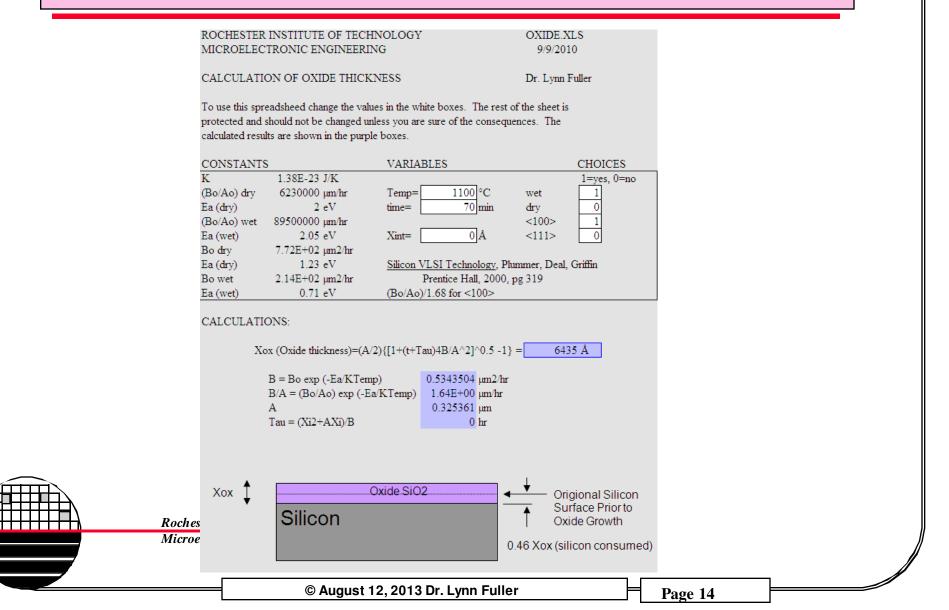
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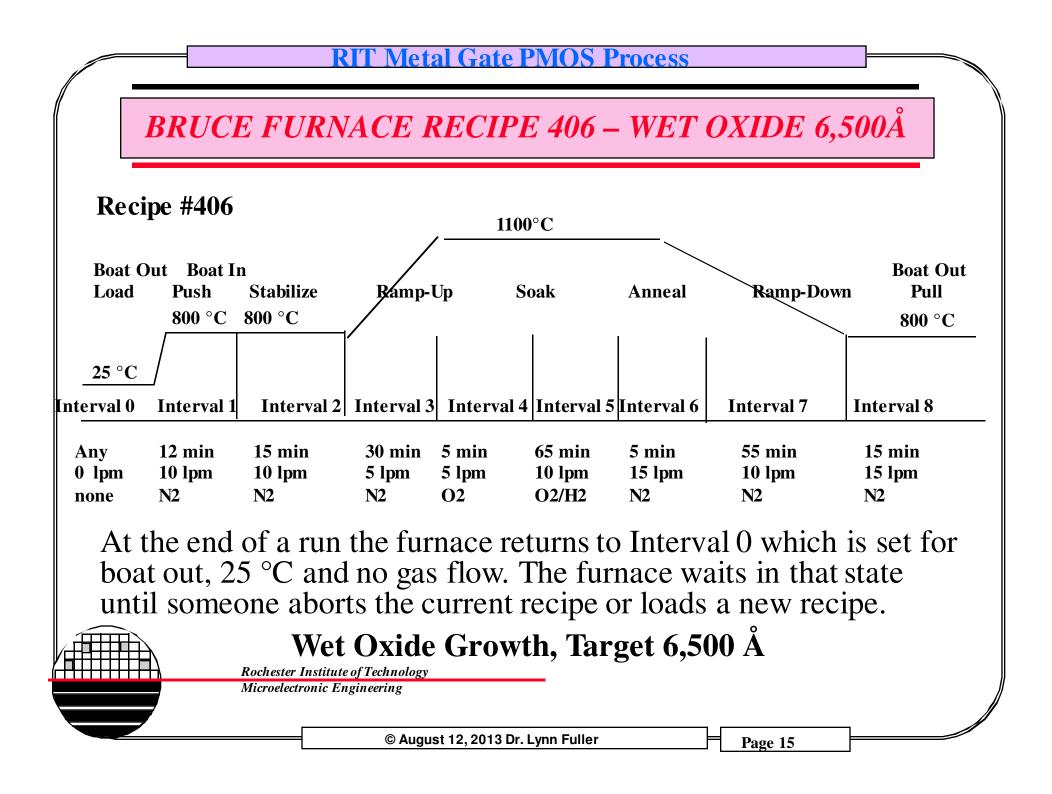
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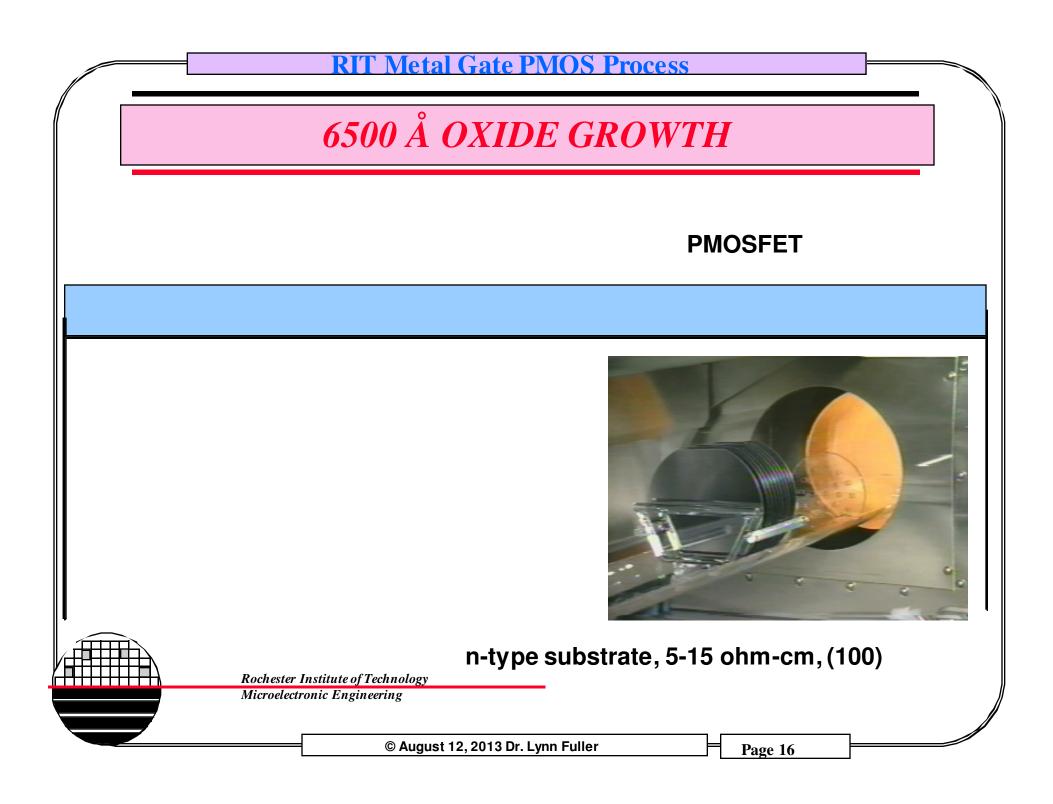




OXIDE THICKNESS CALCULATOR



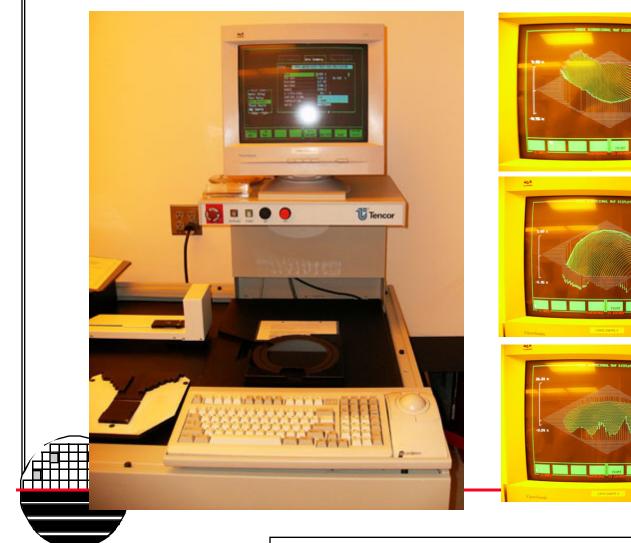




OXIDE COLOR VERSUS THICKNESS TABLE

Thickness	Cobr	_	Thickness	Cobr
500	Tan	thur i	4900	Blue
700	Brown	ula pa igle	5000	Blue Green
1000	Dark Violet - Red Violet	cal cal	5200	Green
1200	Royal Blue	pti	5400	Yellow Green
1500	Light Blue - Metallic Blue	e o e o ith	5600	GreenYellow
1700	Metallic - very light Yellow Green	observed perpendicular light or the optical path change with the angle.	5700	Yellow -"Yellowish" (at times appears to be Lt gray or matellic)
2000	Light Gold or Yellow - Slightly Metallic	or or	5800	Light Orange or Yellow - Pink
2200	Gold with slight Yellow Orange	observed light or t change	6000	Carnation Pink
2500	Orange - Melon		6300	Violet Red
2700	Red Violet	ths) will	6800	"Bluish" (appears violet red, Blue Green, boks grayish)
3000	Blue - Violet Blue	vafer must be c wavelengths) the color will	7200	Blue Green - Green
3100	Blue	col col	7700	"Yelbwish"
3200	Blue - Blue Green	wafer I wav e the e	8000	Orange
3400	Light Green	il v s	8200	Salmon
3500	Green - Yellow Green	the the e (al	8500	Dull, LIght Red Violet
3600	Yellow Green	, p. i.	8600	Violet
3700	Yellow	erve a valid color, the w surface under white (all will be different, hence	8700	Blue Violet
3900	Light Orange	d c fer	8900	Blue
4100	Carnation Pink	valid unde diffe	9200	Blue Green
4200	Violet Red	be a	9500	Dull Yellow Green
4400	Red Violet	rfa ill	9700	Yellow - "Yellowish"
4600	Violet	To observe a valid color, the w to the surface under white (all length will be different, hence	9900	Orange
4700	Blue Violet	To obs to the s length	10000	Carnation Pink
	Yes!	To I len	SiO₂	No! SiO ₂
	Microelectronic I Silicon			Silicon
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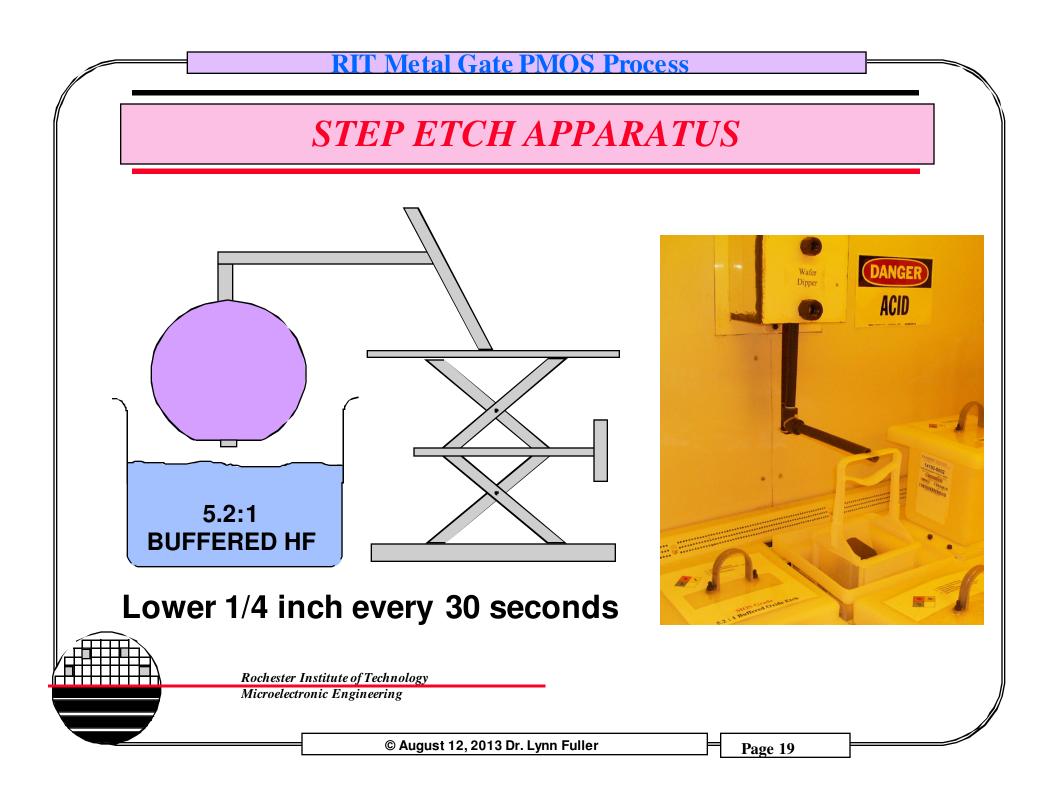
TENCORE SPECROMAP

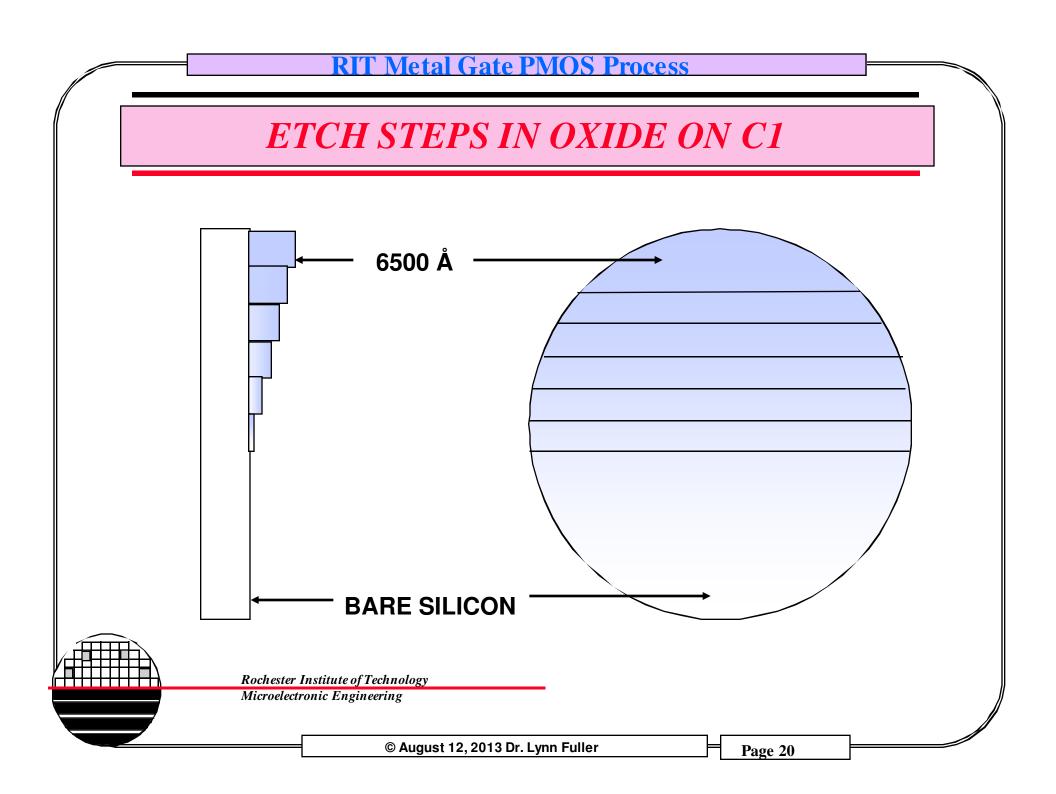


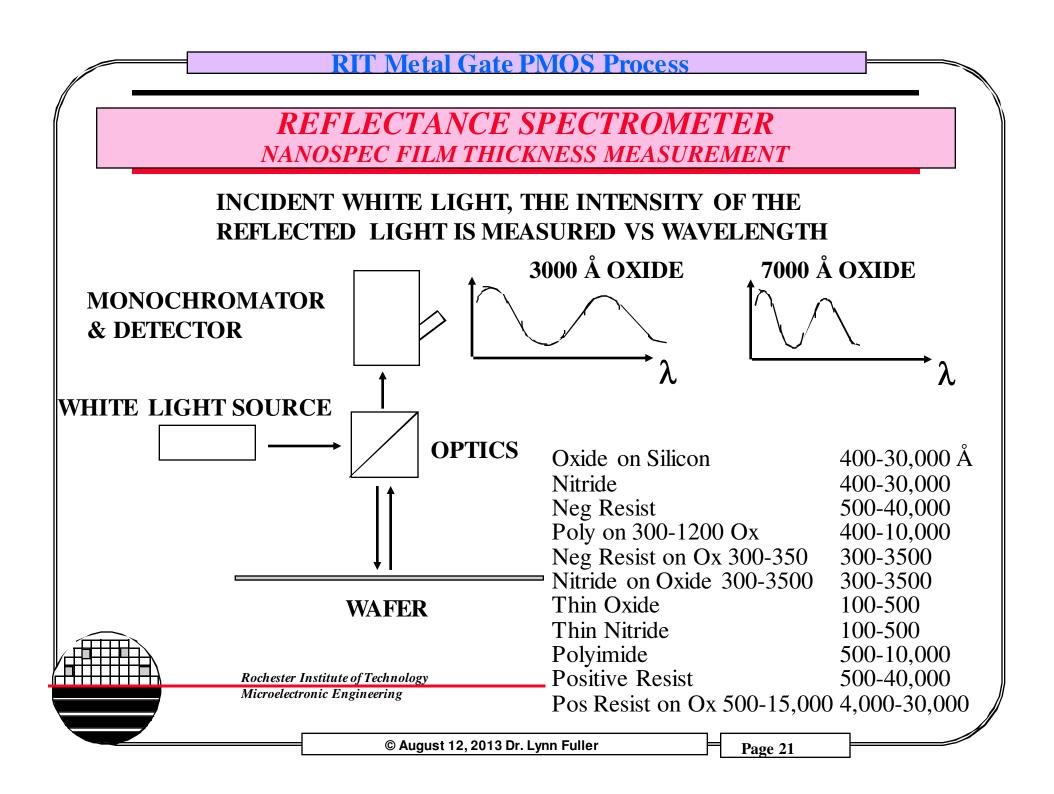


Std Deviation No of Points

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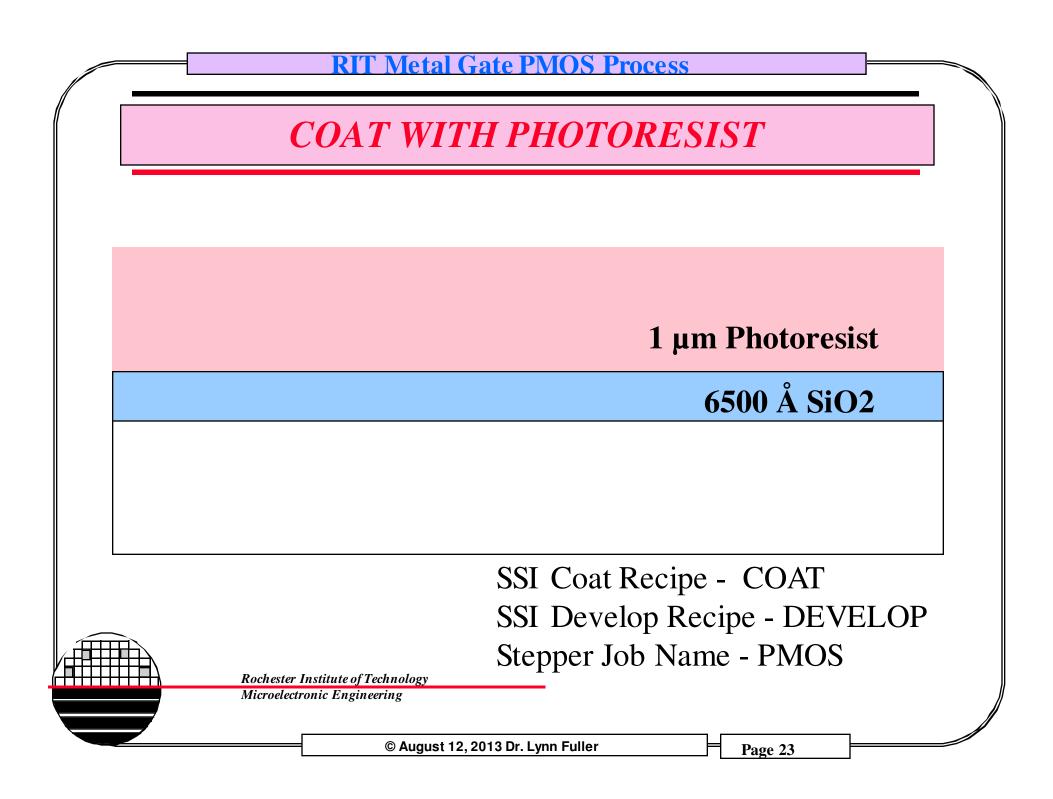
MEASURE OXIDE THICKNESS



Record:	
Color =	
Color Chart Thickness =	Å
Nanospec Thickness =	Å

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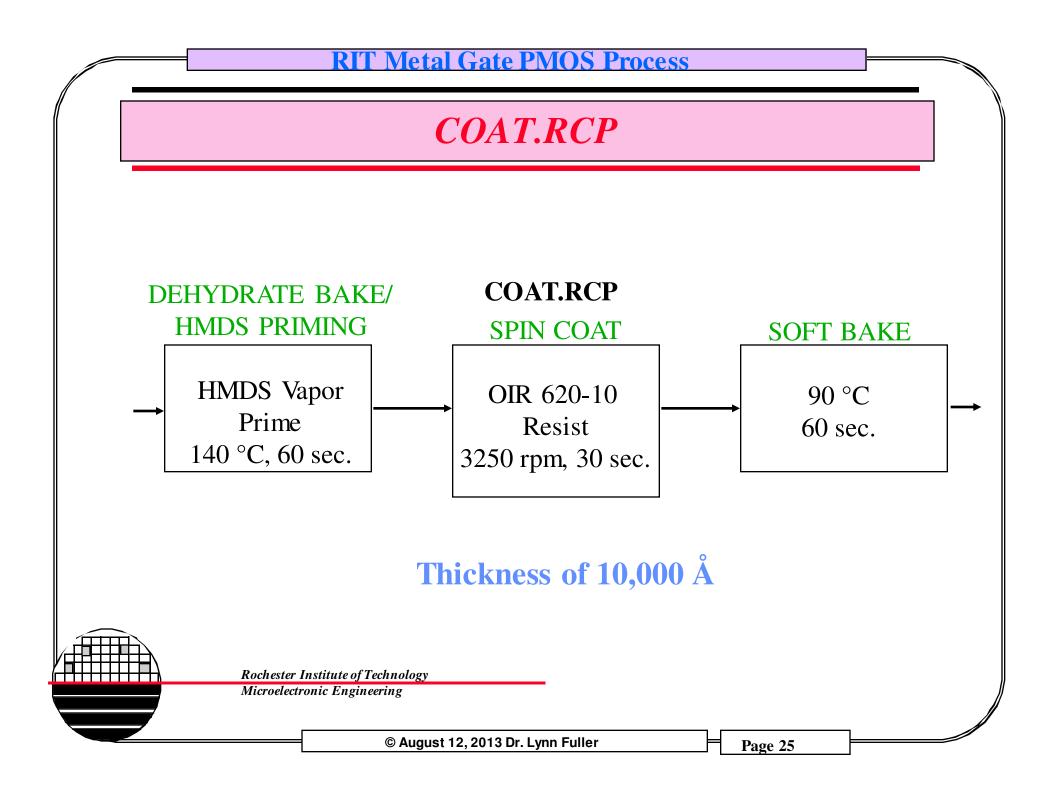


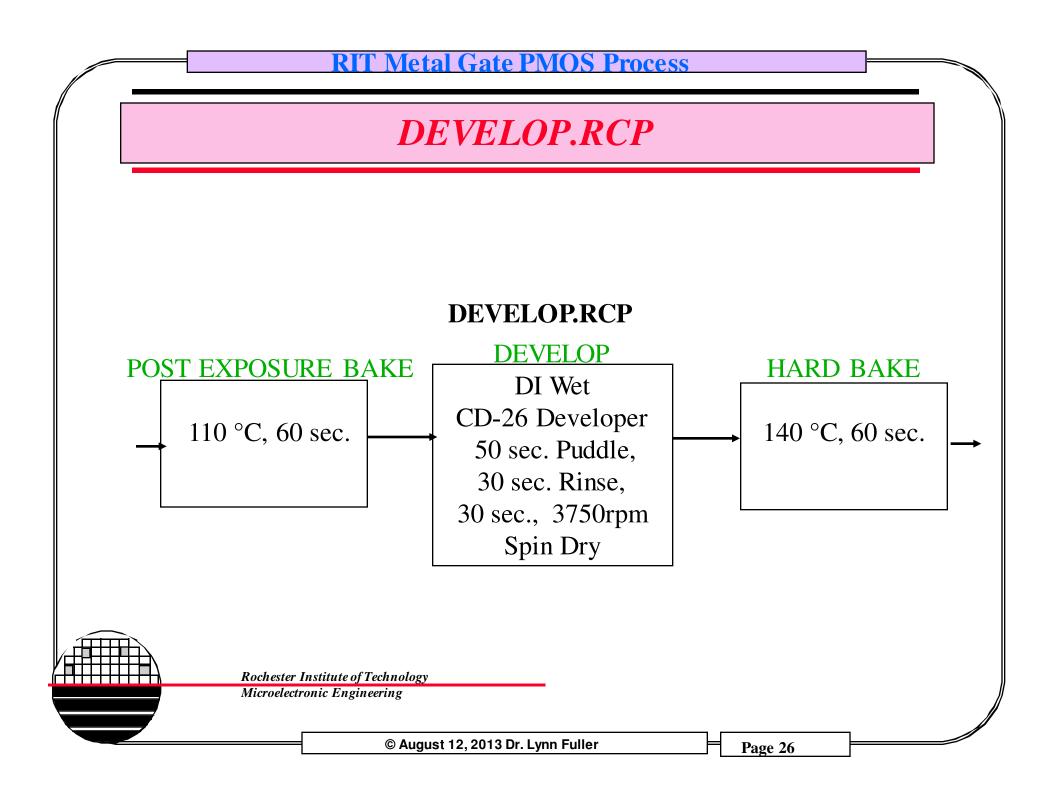
Metal Gate PMOS Process **RT** LITHOGRAPHY FOR PMOS 150 PROCESS Spin Xpr Coat Dev Dev Hard Bake Lv Level Dose Recipe mj/cm² | # **RPM** Name Recipe Time μm 50s 140C/1min Diff develop 1 3250 1.0 250 coat 2 ThinOx 250 140C/2min 1.3 68s 2000 devmtl coatmt 3 140C/1min CC 1.3 250 coatmt 2000 devCC 180s 4 Metal 2000 1.3 250 devmtl 68s 140C/2min coatmtl

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SSI COAT AND DEVELOP TRACK FOR 6" WAFERS

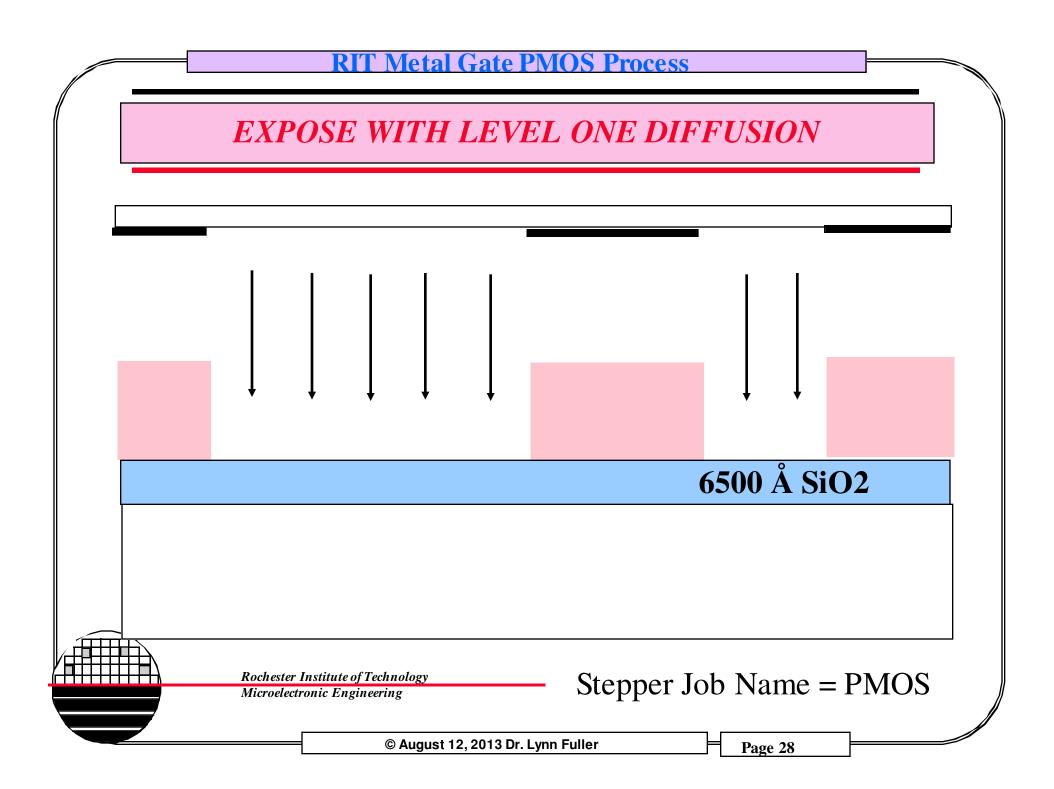


Use Recipe: Coat.rcp and Develop.rcp

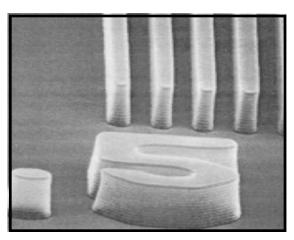
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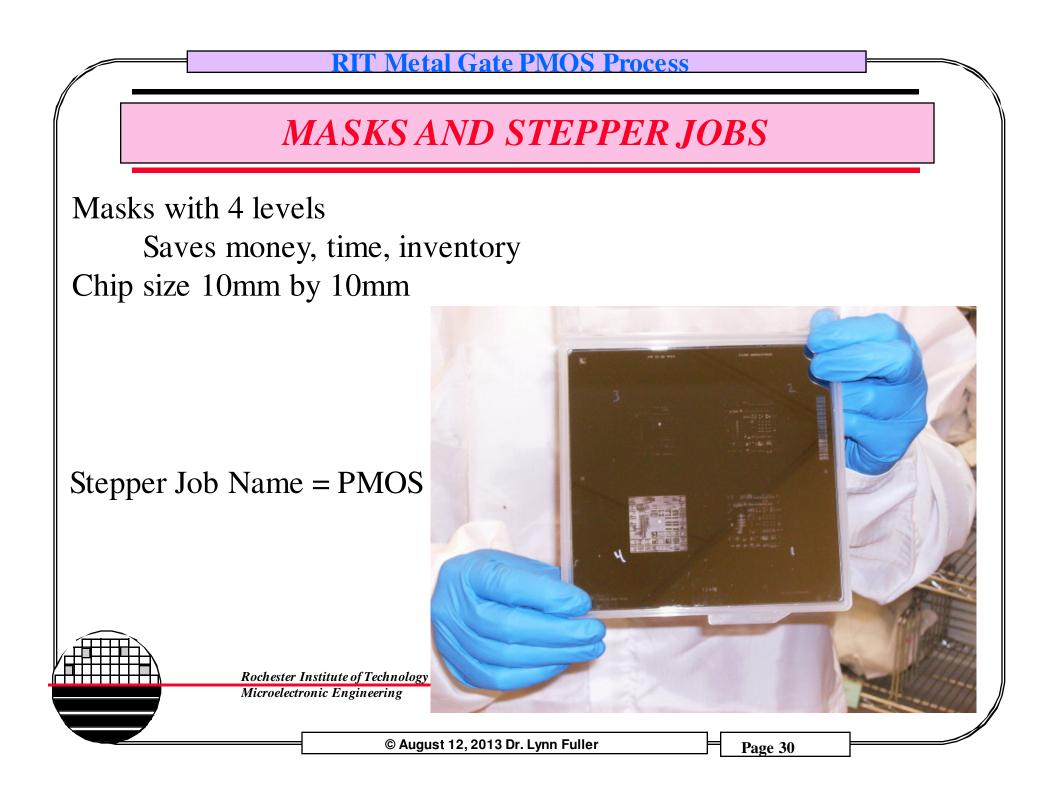
ASML 5500/200 STEPPER

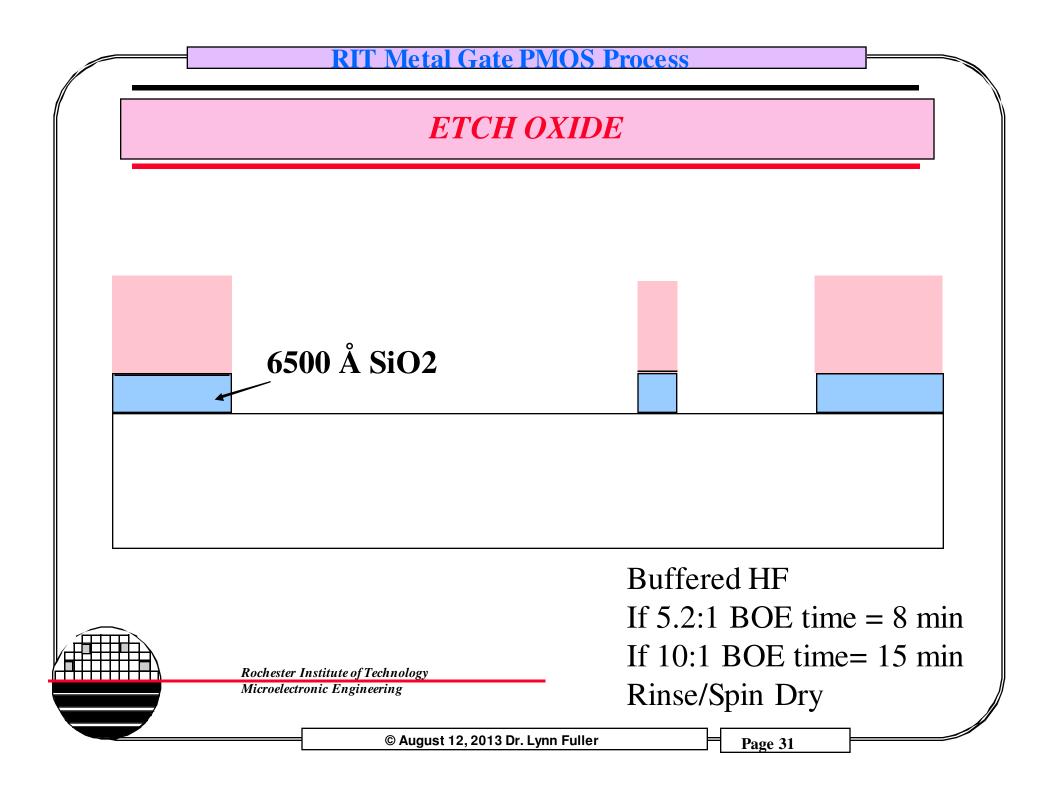


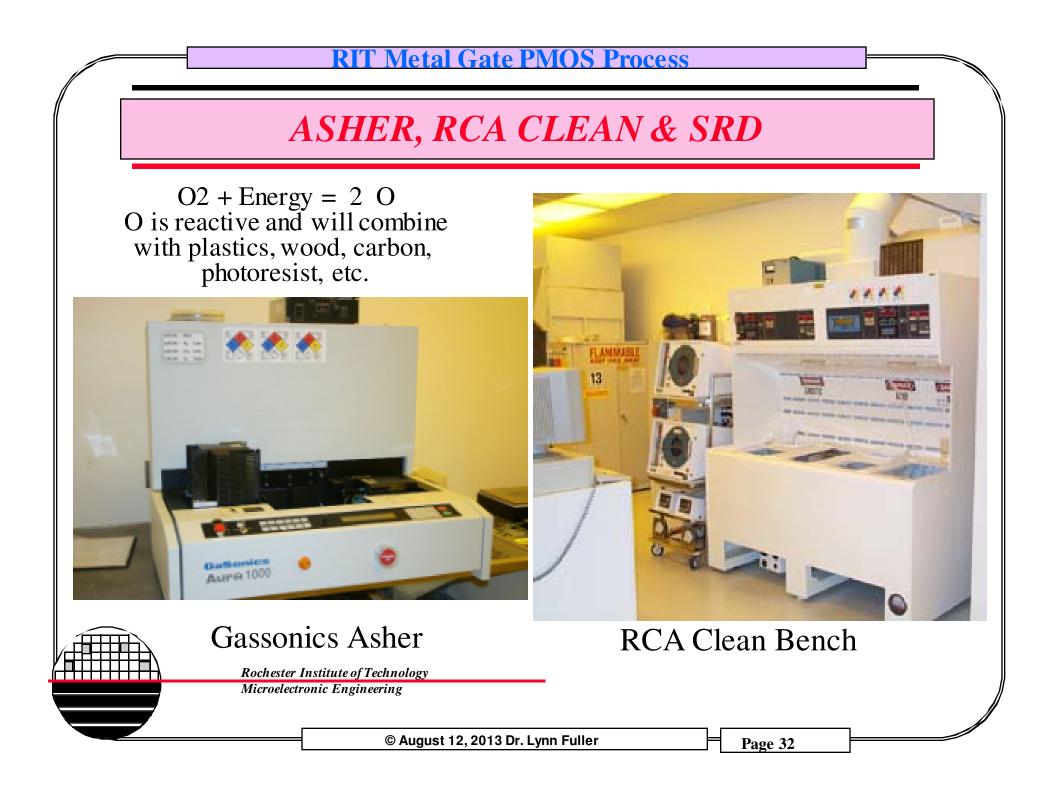
NA = 0.48 to 0.60 variable σ = 0.35 to 0.85 variable With Variable Kohler, or Variable Annular illumination Resolution = K1 λ /NA = ~ 0.35 μ m for NA=0.6, σ =0.85 Depth of Focus = k₂ λ /(NA)² = > 1.0 μ m for NA = 0.6

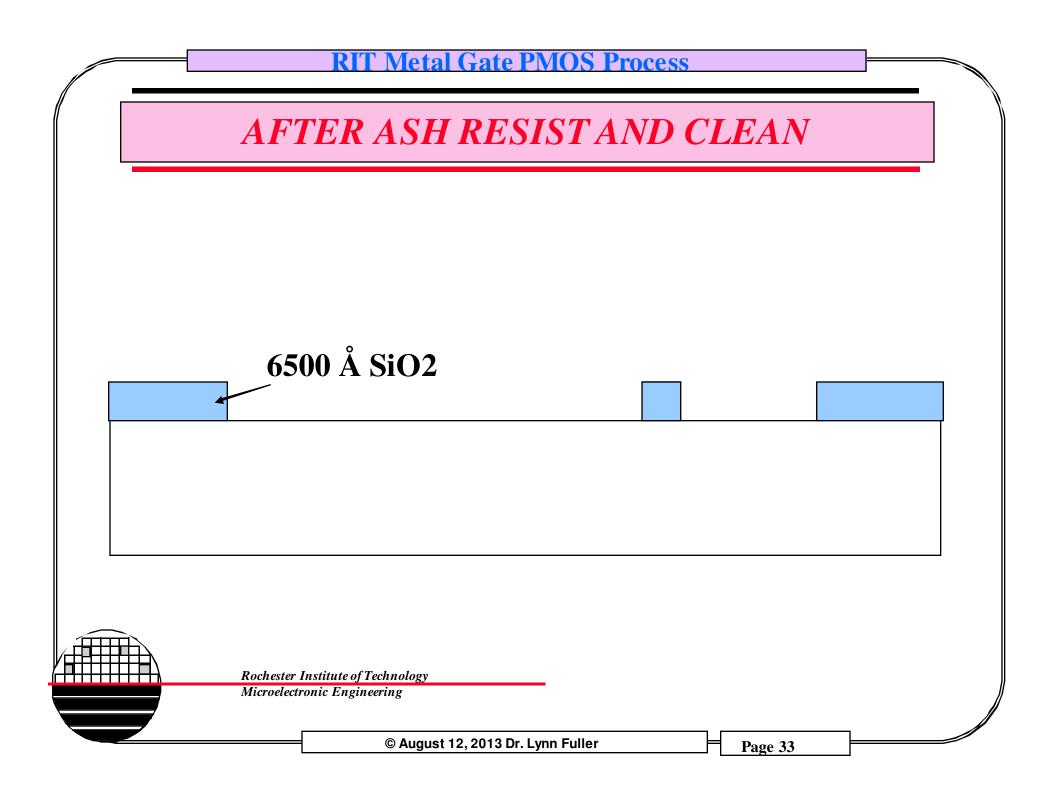
i-Line Stepper $\lambda = 365$ nm 22 x 27 mm Field Size

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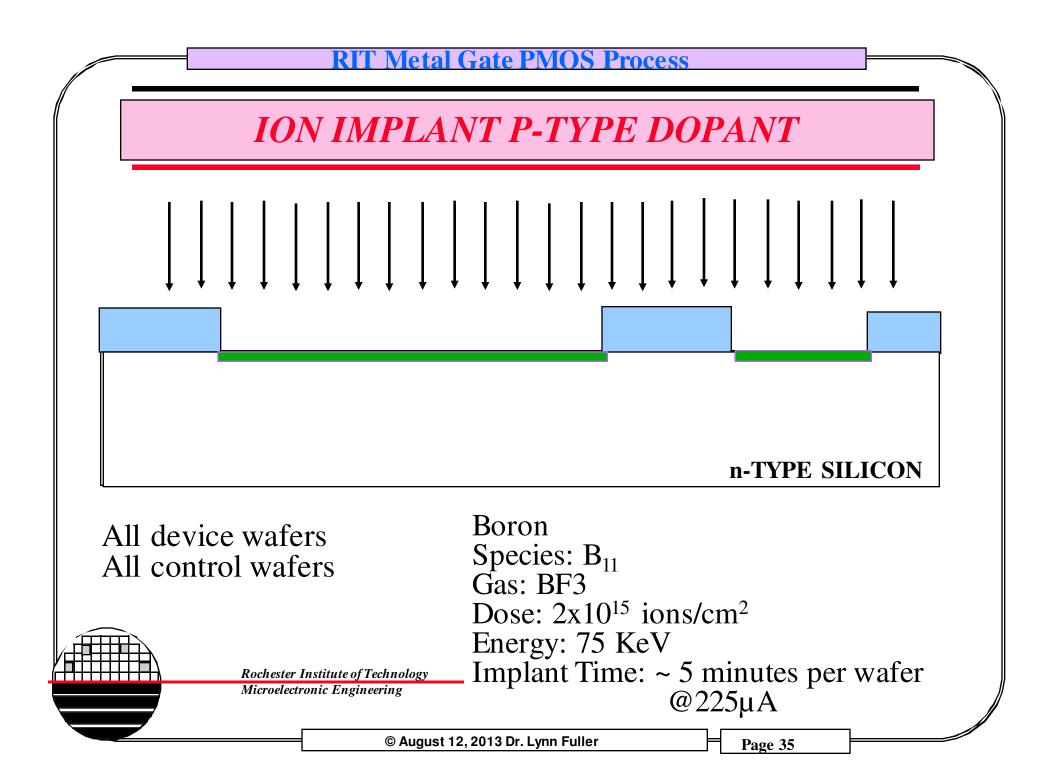


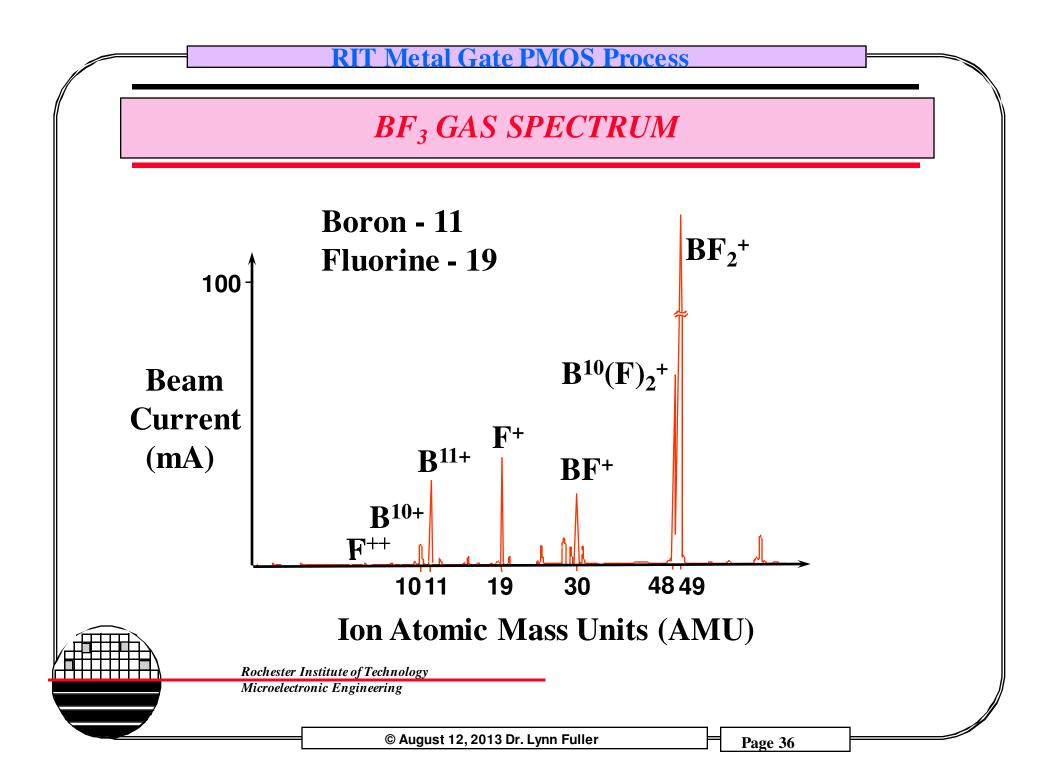


VARIAN 350 D ION IMPLANTER (4" AND 6" WAFERS)

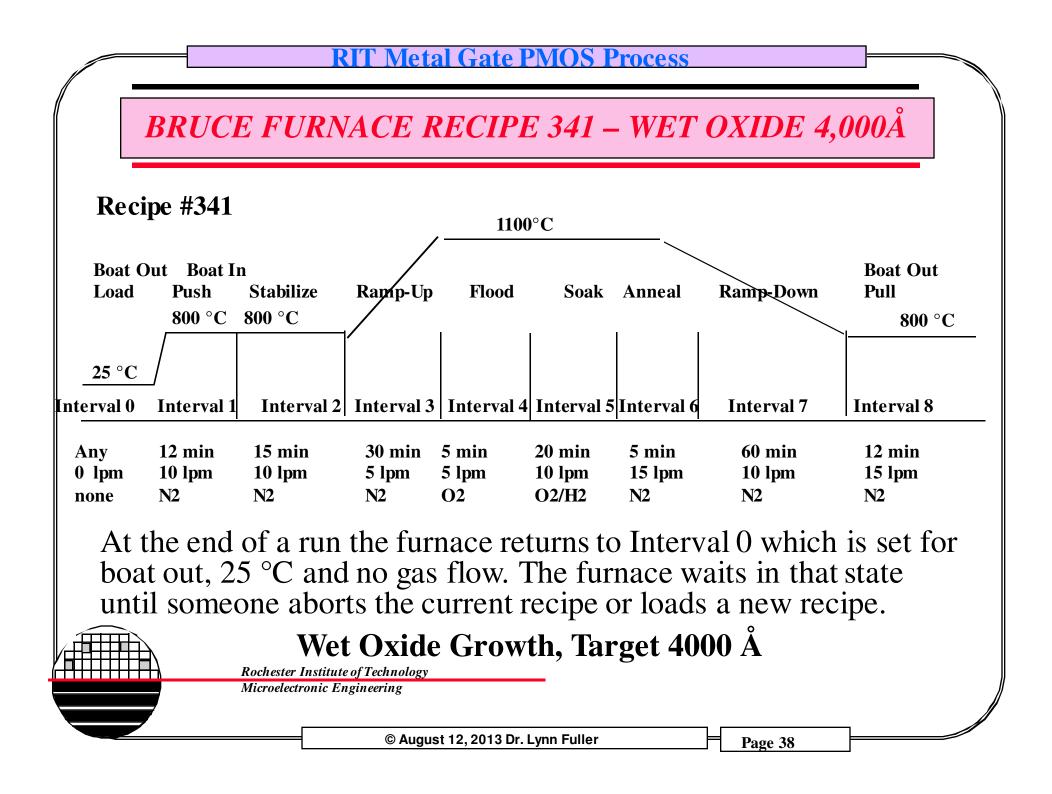


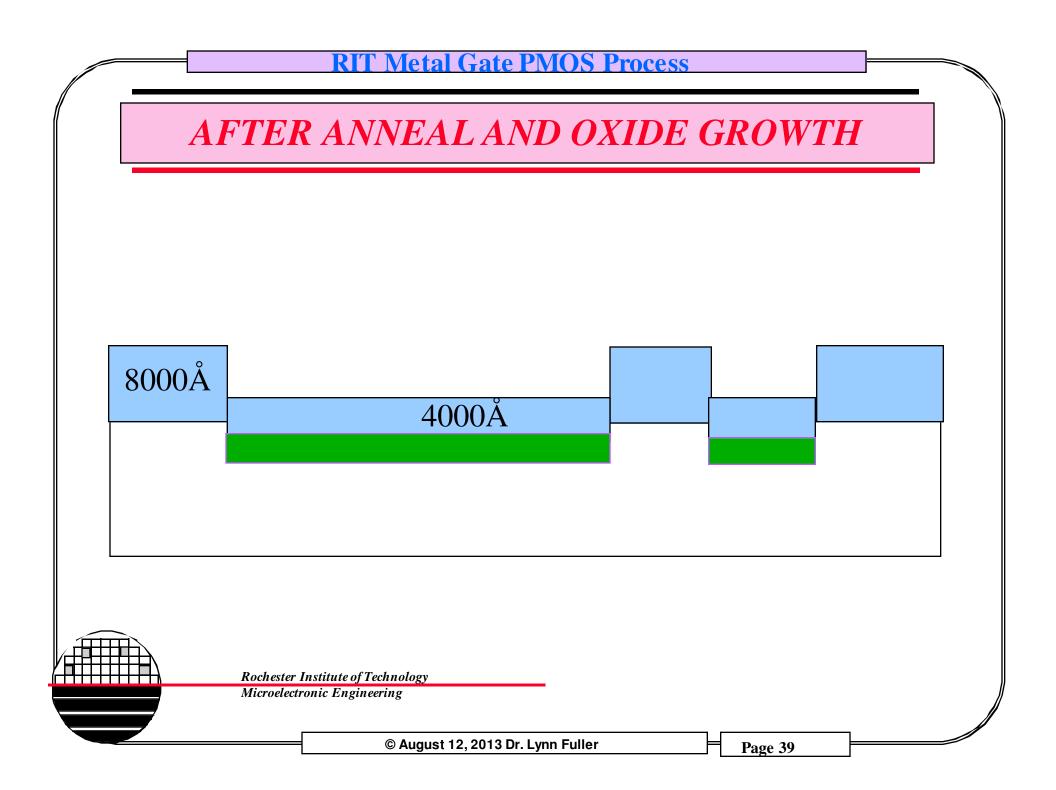
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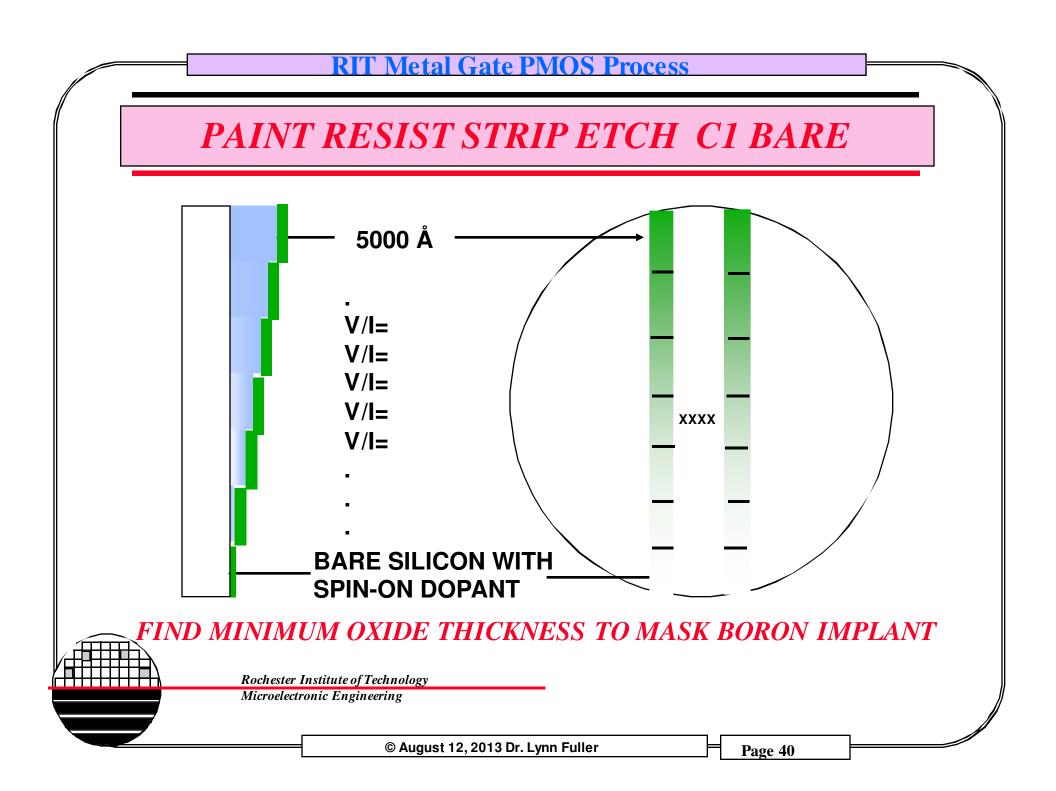


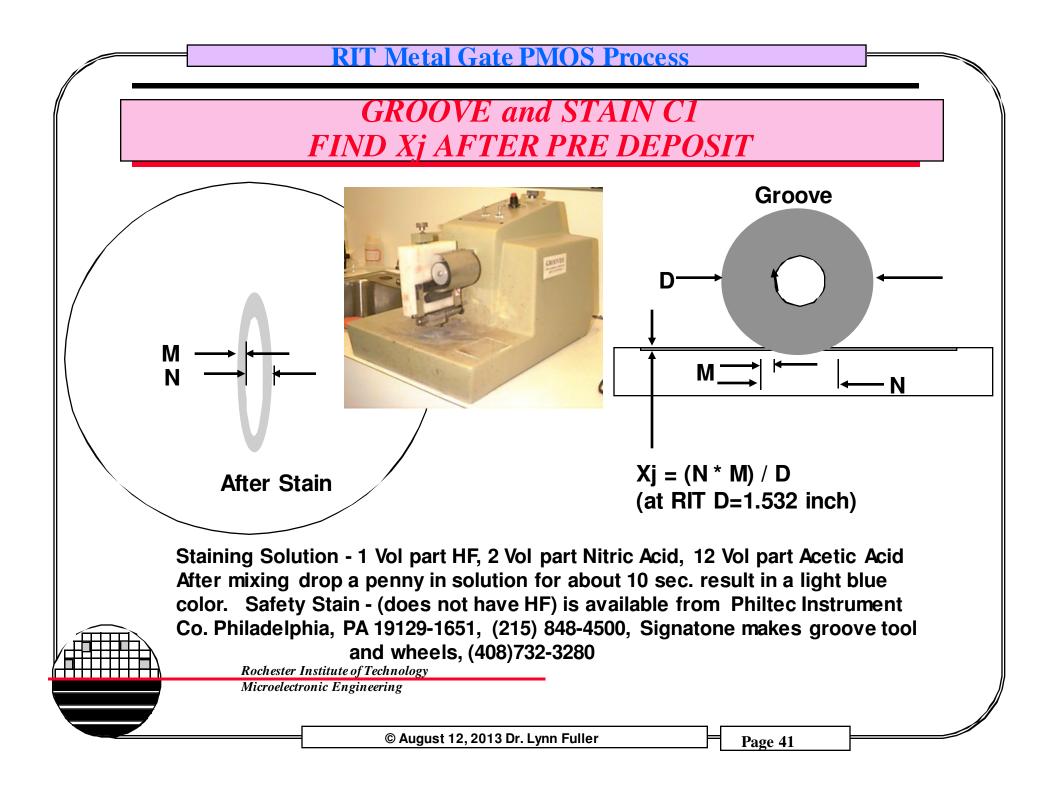


<u>F Metal Gate PMOS Process</u> RTI **IMPLANT MASKING THICKNESS CALCULATOR** Lance Barron Rochester Institute of Technology Microelectronic Engineering Dr. Lynn Fuller 11/20/2004 **IMPLANT MASK CALCULATOR** Enter 1 - Yes 0 - No in white boxes **DOPANT SPECIES MASK TYPE ENERGY** KeV **B11** Resist 75 0 1 BF2 0 Poly 0 **P31** 0 Oxide 1 Nitride 0 Thickness to Mask >1E15/cm3 Surface Concentration 3971.104 Angstroms Rochester Institute of Technology Microelectronic Engineering © August 12, 2013 Dr. Lynn Fuller Page 37









TRAVELING STAGE MICROSCOPE



Example: If M=.003 inches and N=0.025 inches, find xj.

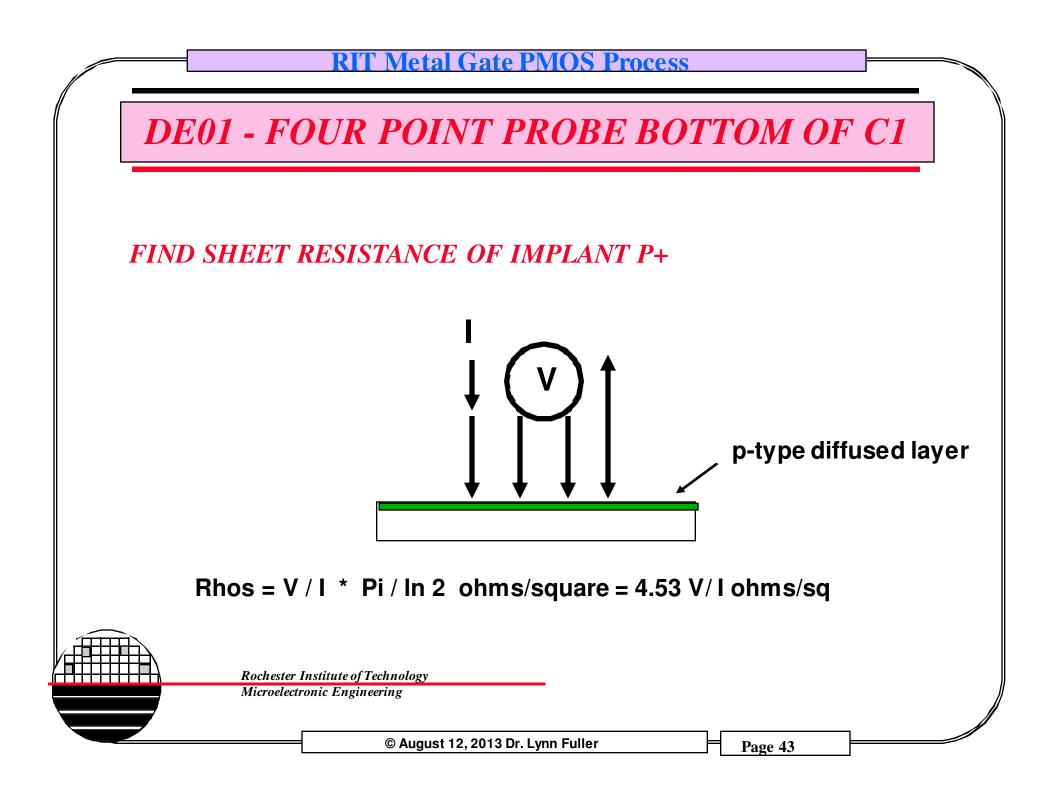
Xj = (N * M) / D

- = (0.025 * 0.003)/1.588 inch)
- = 0.0000472 inch
- = 1.20 μm

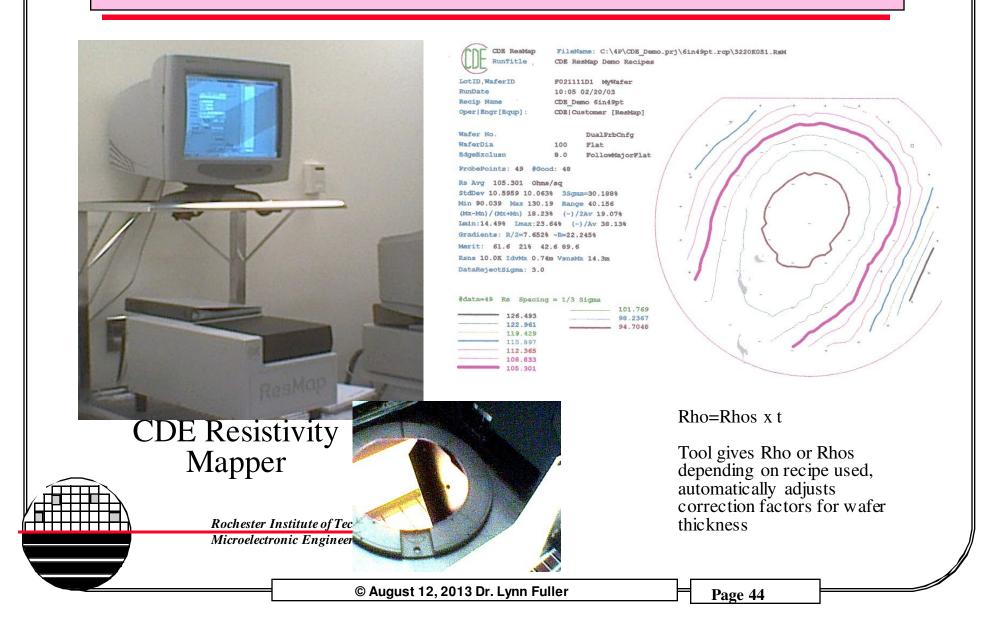
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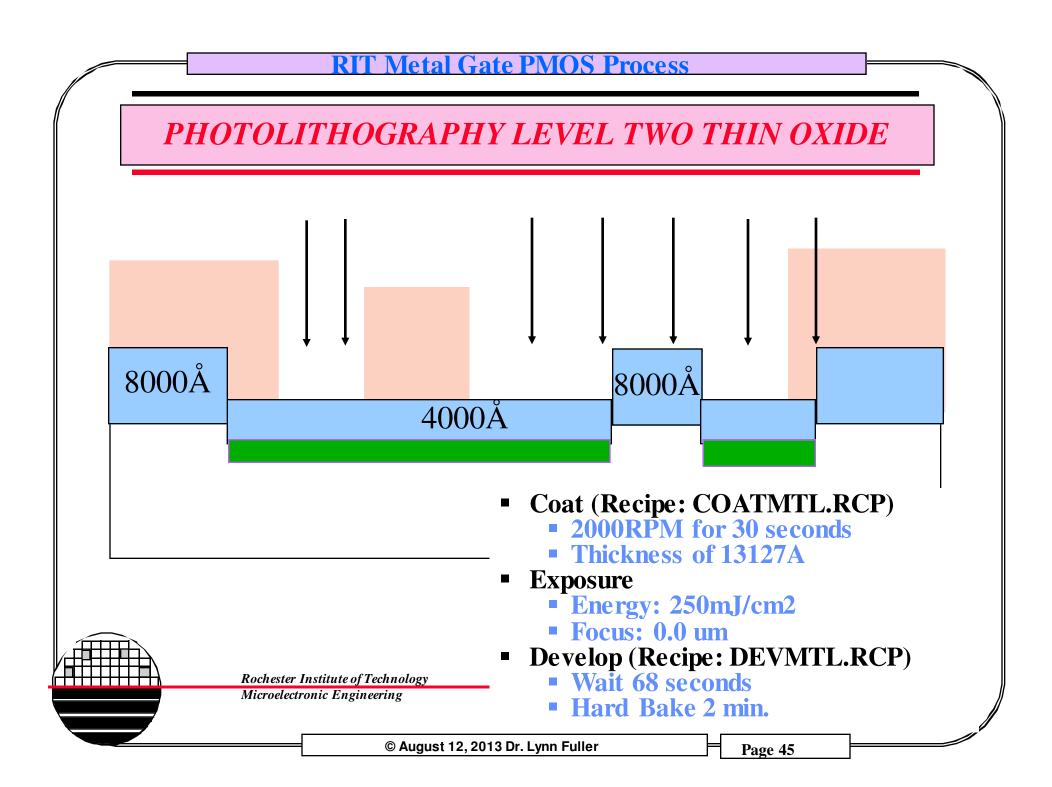
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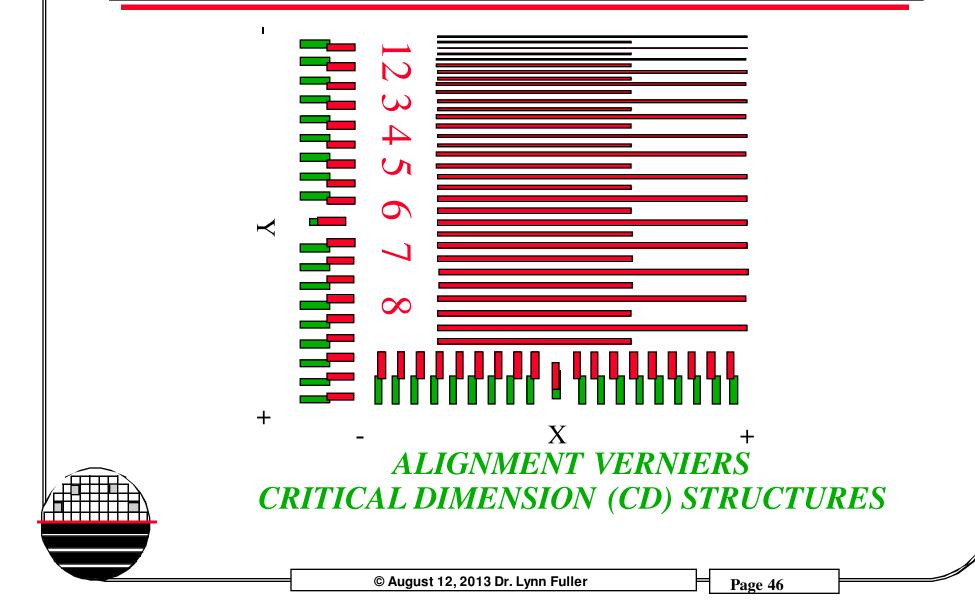


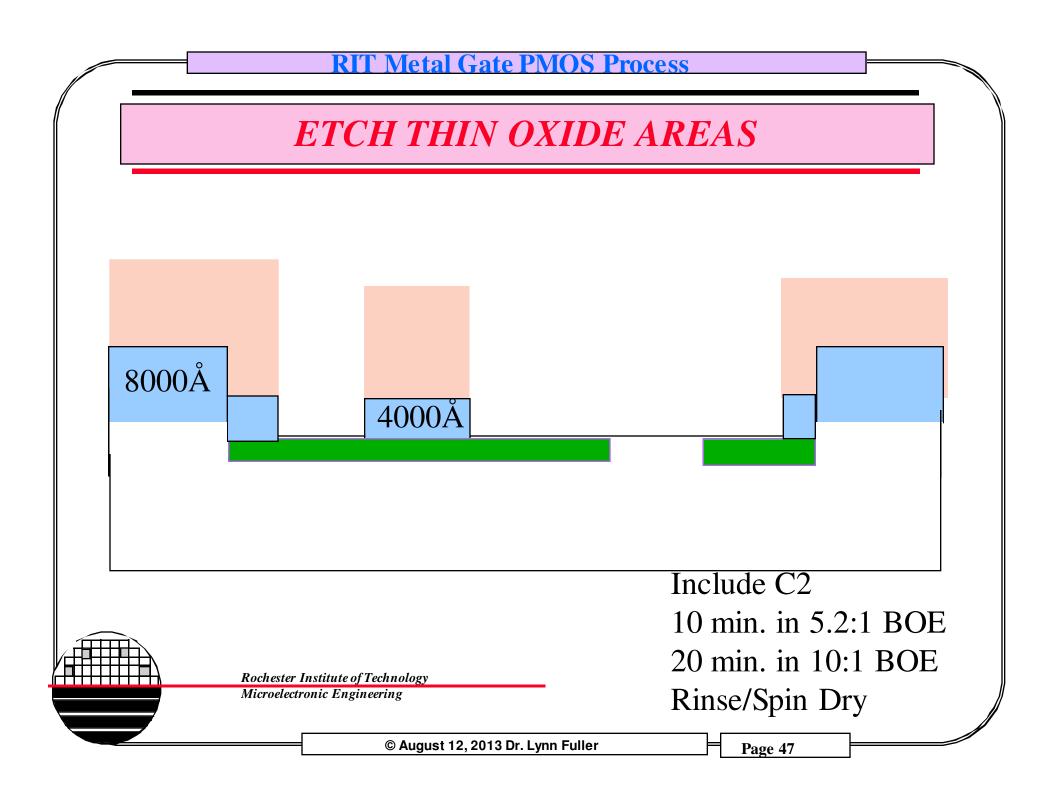
MEASURE SHEET RESISTANCE

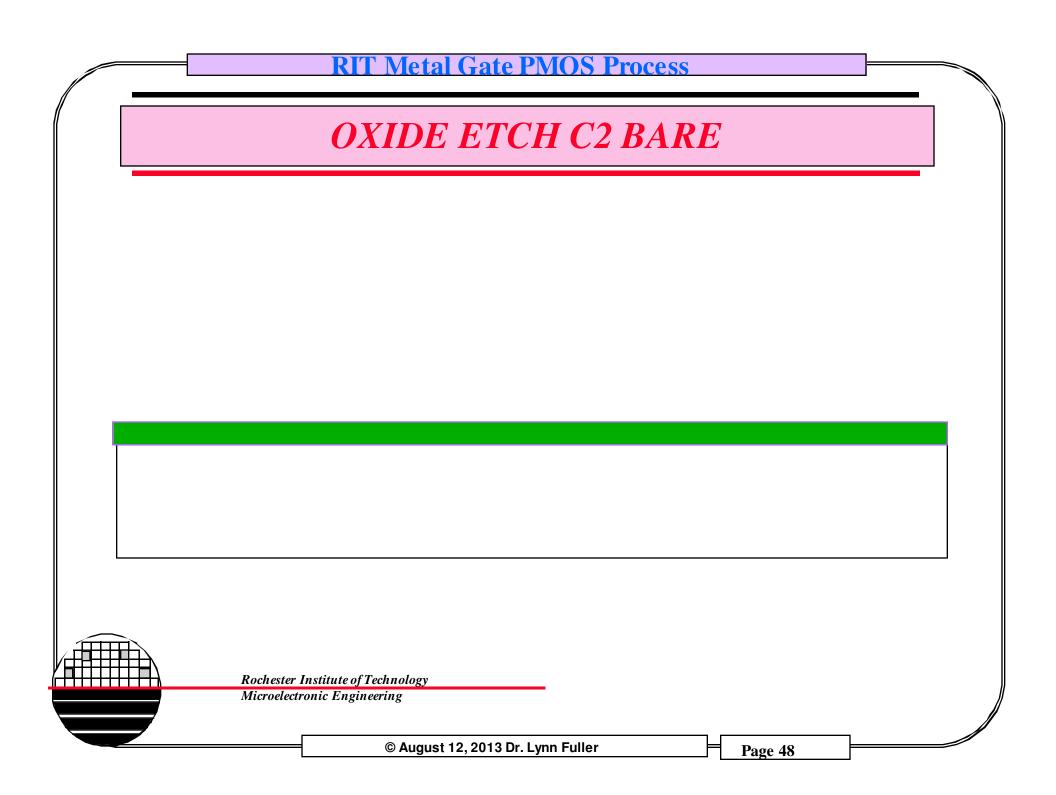


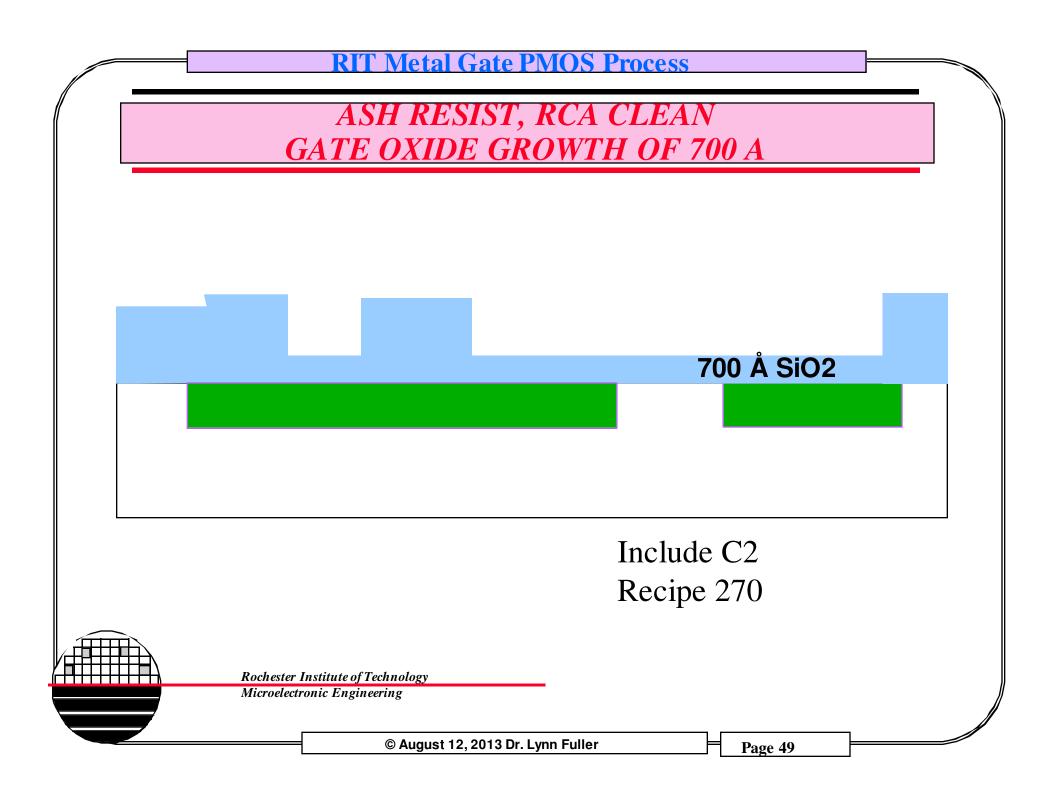


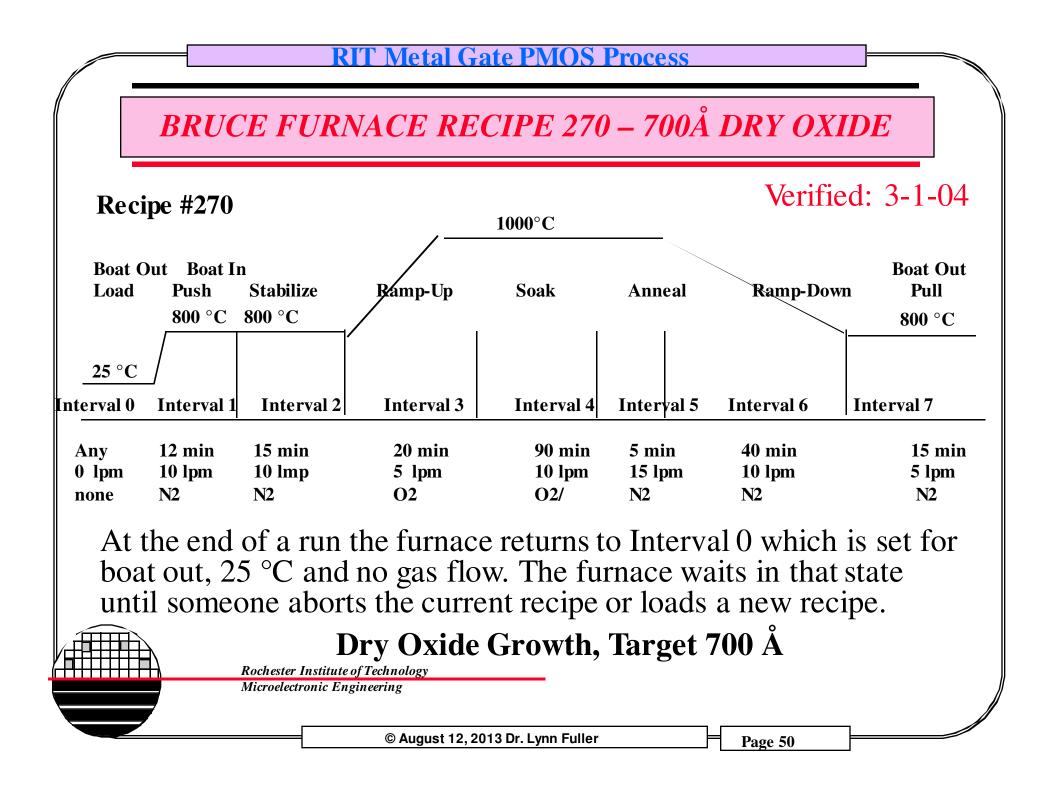
2ND PHOTOLITHOGRAPHY

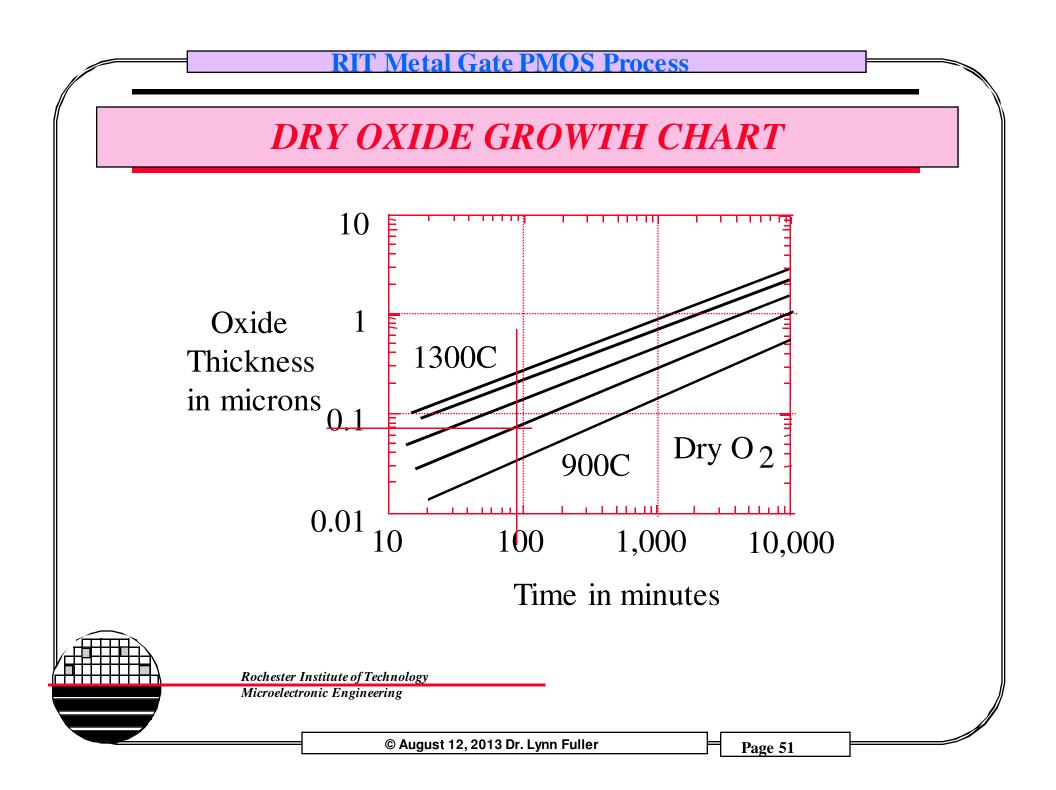




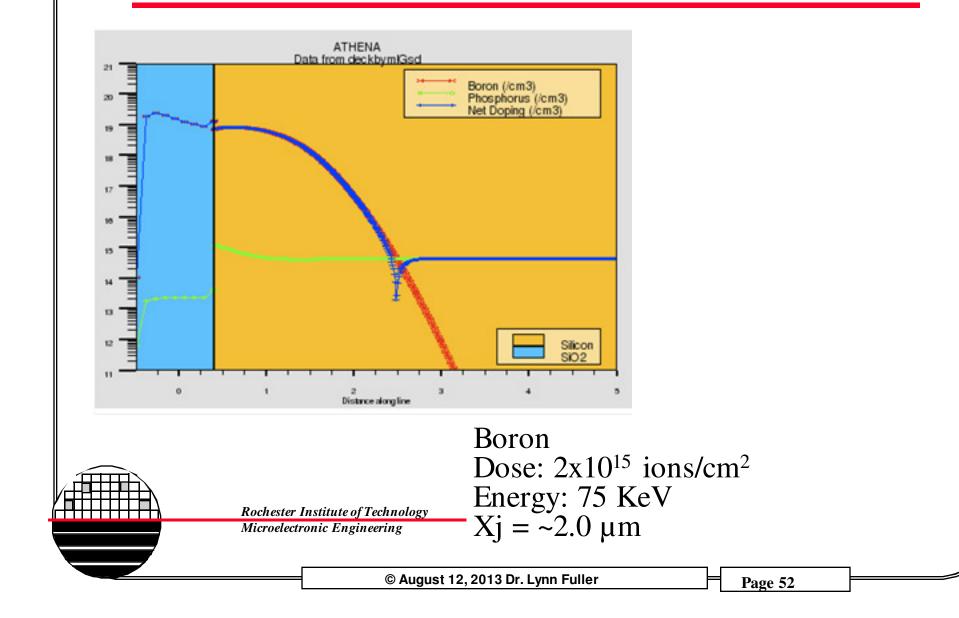


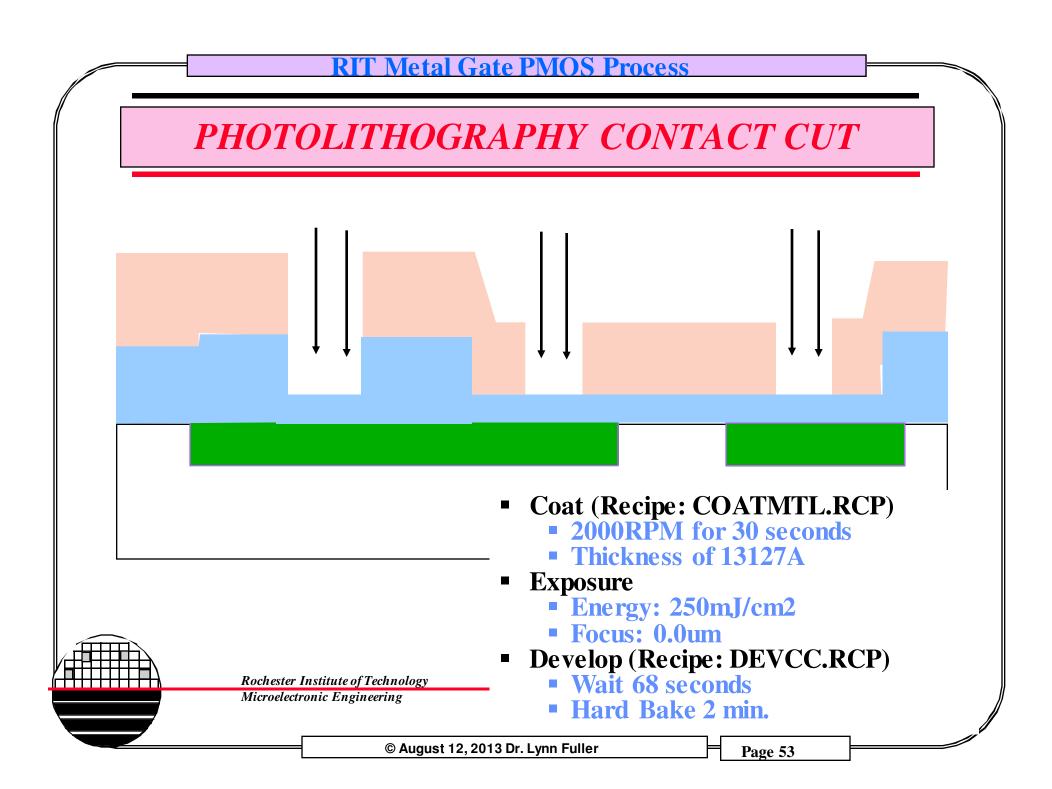


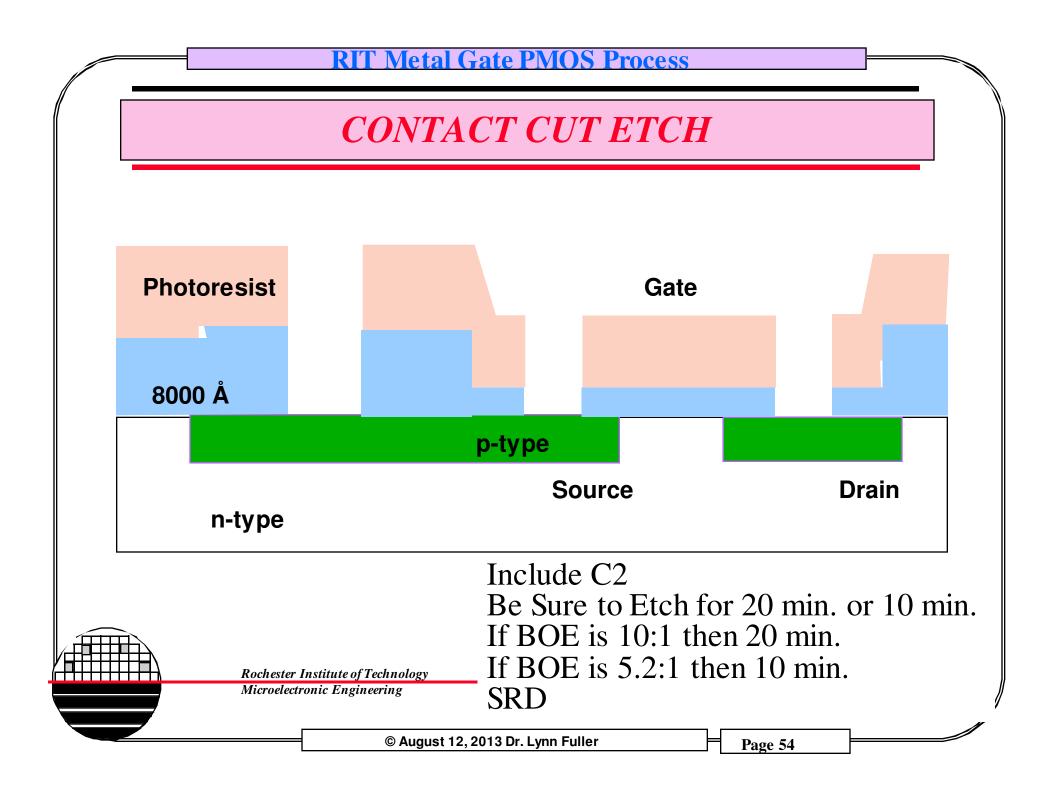


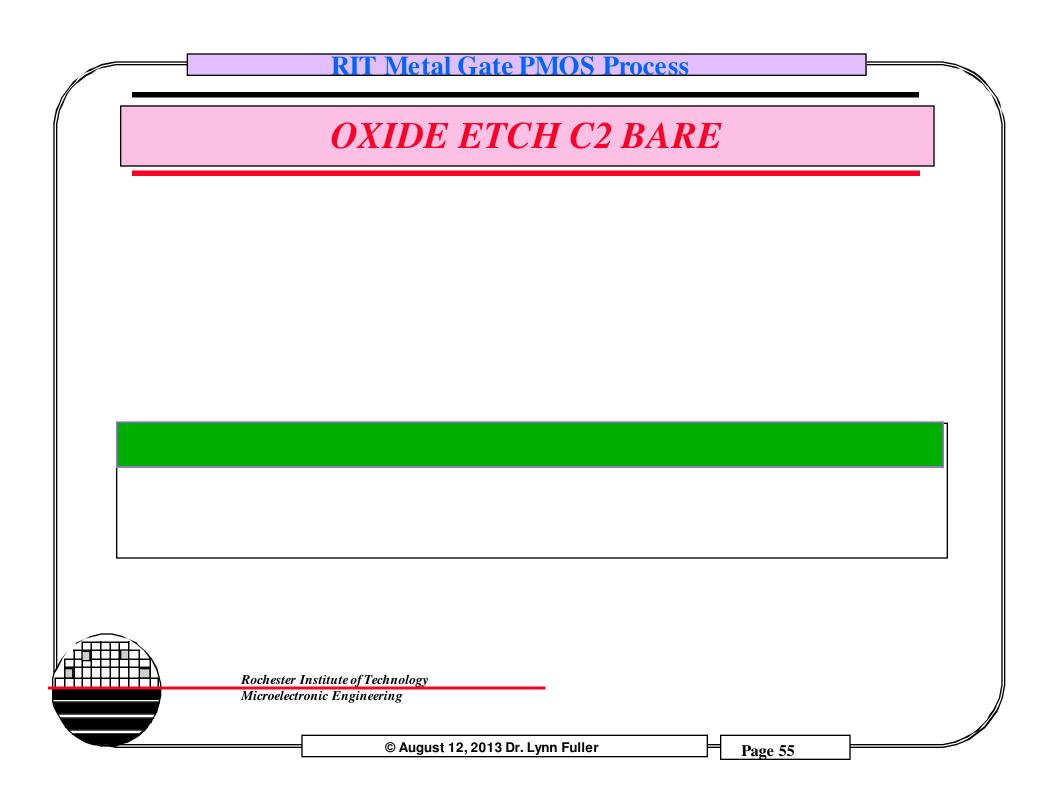


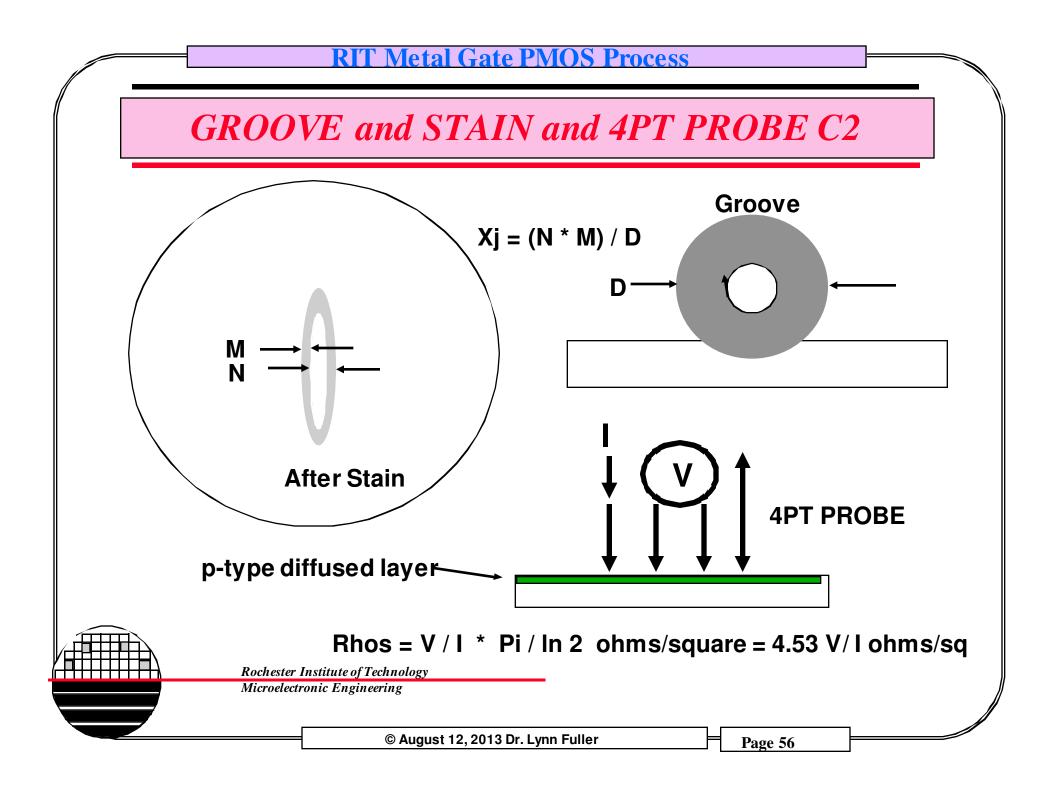
SIMULATION AFTER ALL HIGH TEMP STEPS

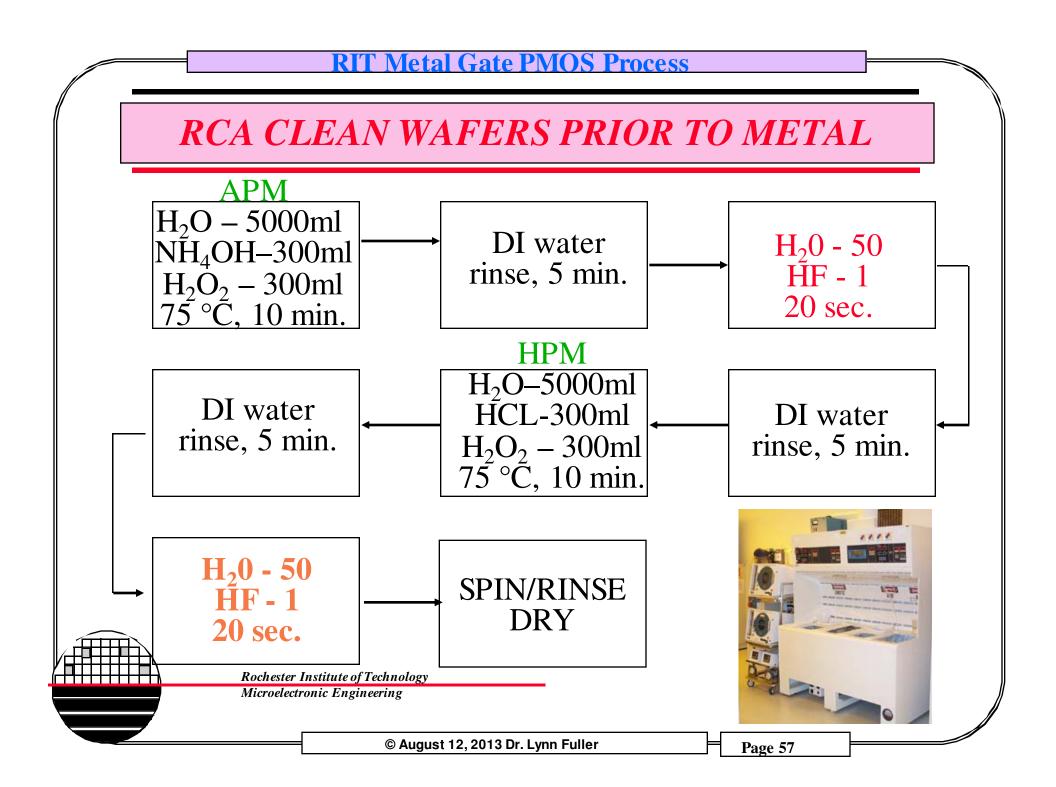


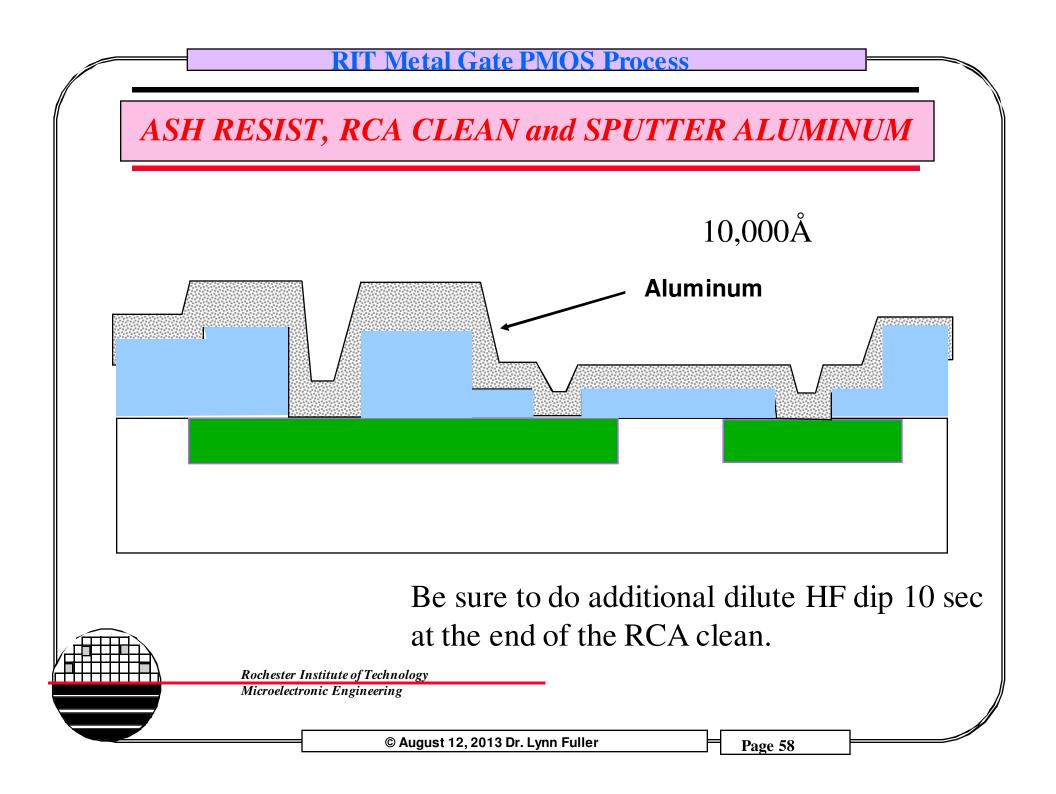












METAL DEPOSITION



CVC 601 Thickness 10,000Å Dep Rate \sim 300 A/min Pressure 5 mT Ar Flow 28 sccm Time \sim 20 min \sim 2000 sec Power 2000 watts Pre Sputter 300 sec

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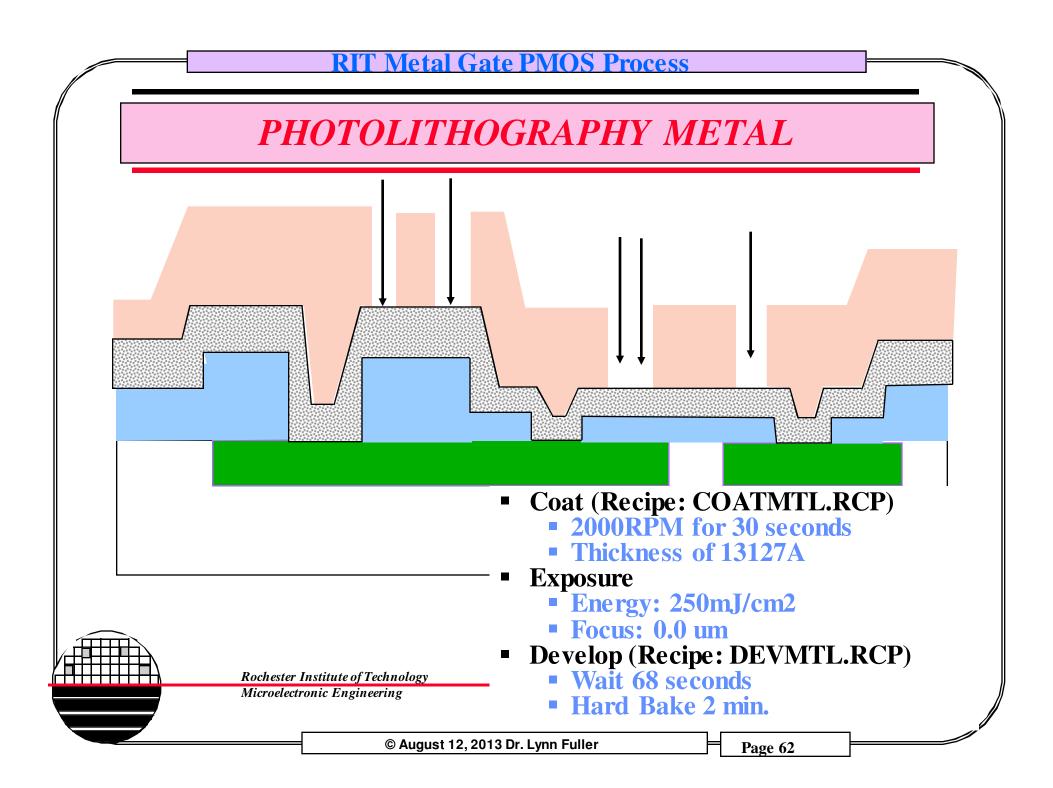
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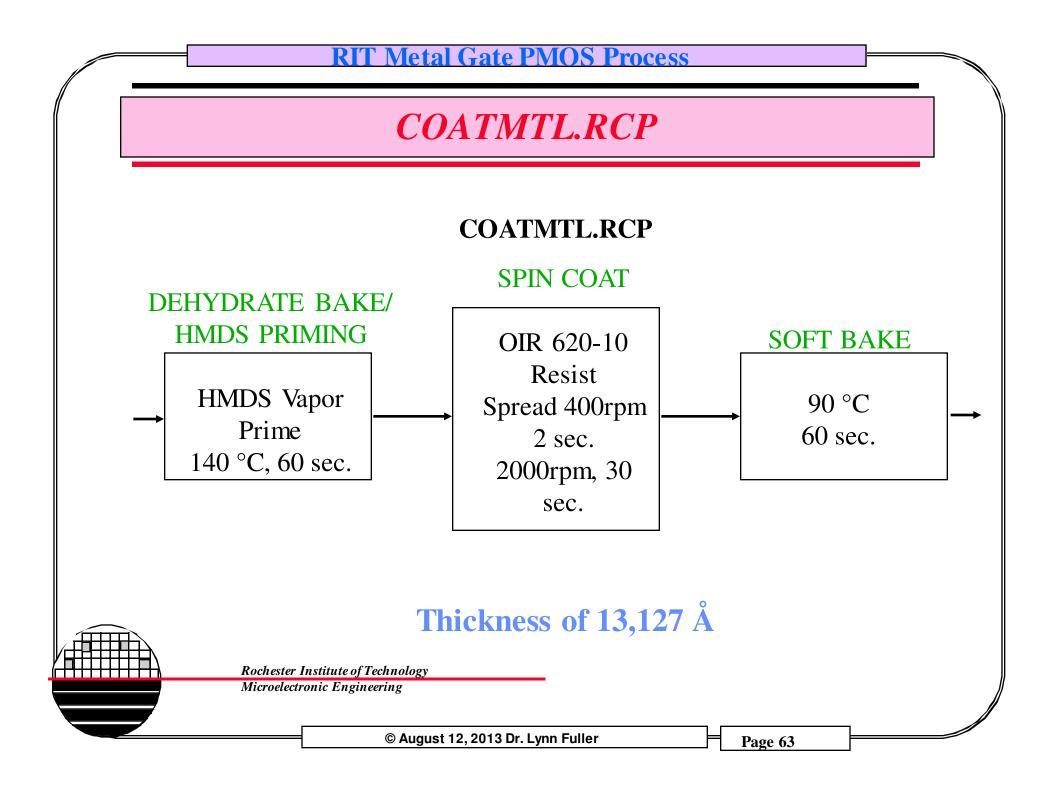
PE4400 SPUTTER / SPUTTER ETCH TOOL

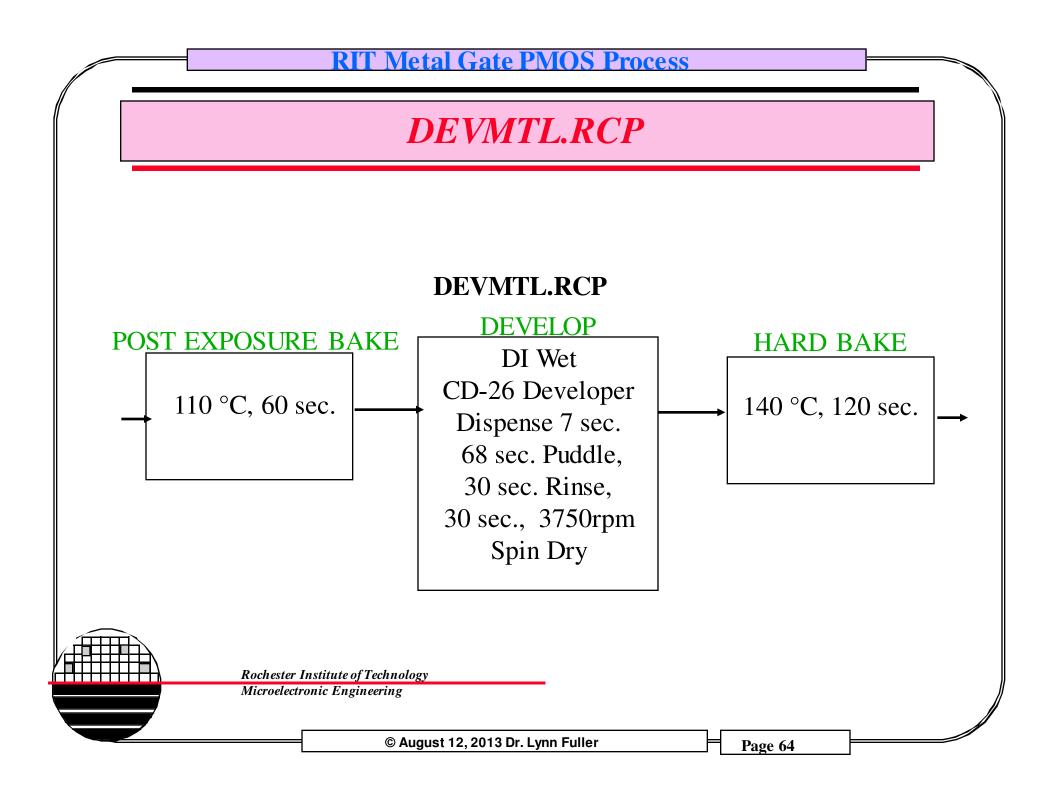


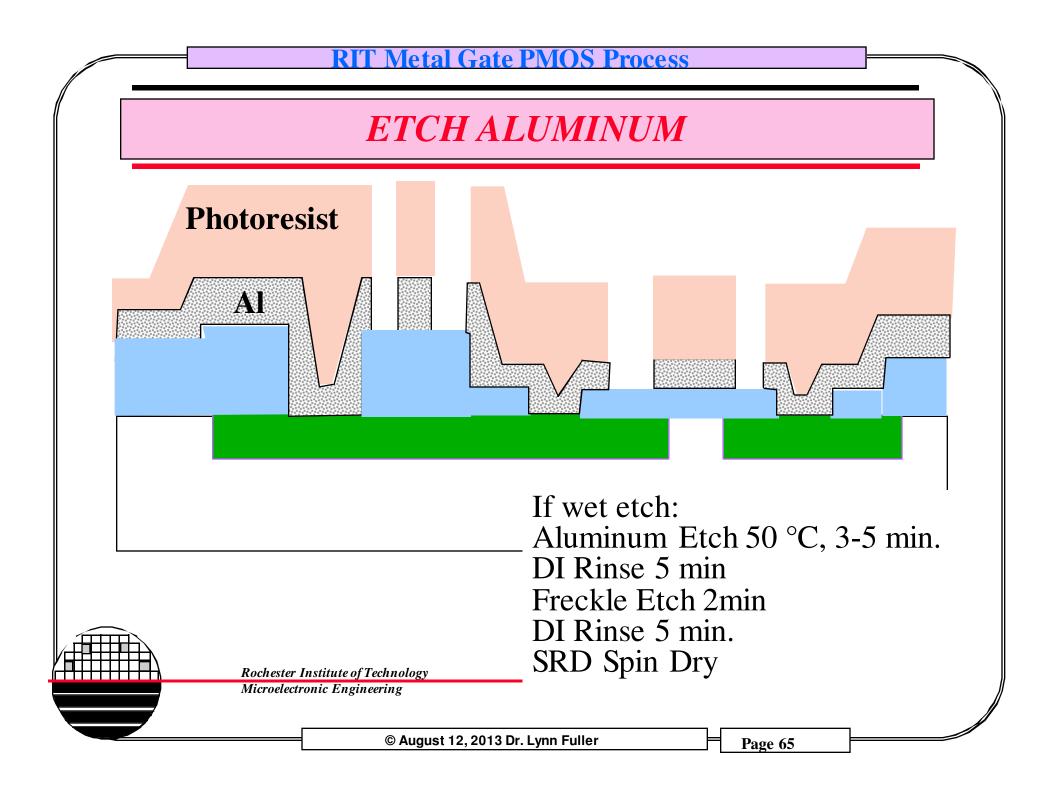
Metal Gate PMOS Process **R I** ' **PE4400 – ALUMINUM DEPOSITION** Results **Tool Parameters** Wafer ID: 10/4 Power = 400 watts Ave thickness = Pressure 5 mTorr 8665 Å From P2 Chiller 20 °C Min =Max =Argon flow 40 sccm Non Uniformity = % Dep Rate ~64Å/min? Time = 135 min (2hr 15min) Surface Roughness 10nm great **Blank Wafers** Table rotation speed 200 = -6rpm Name: Magnet array @1° angle Date: Table space as close as possible **Rochester Institute of Technology** Microelectronic Engineering

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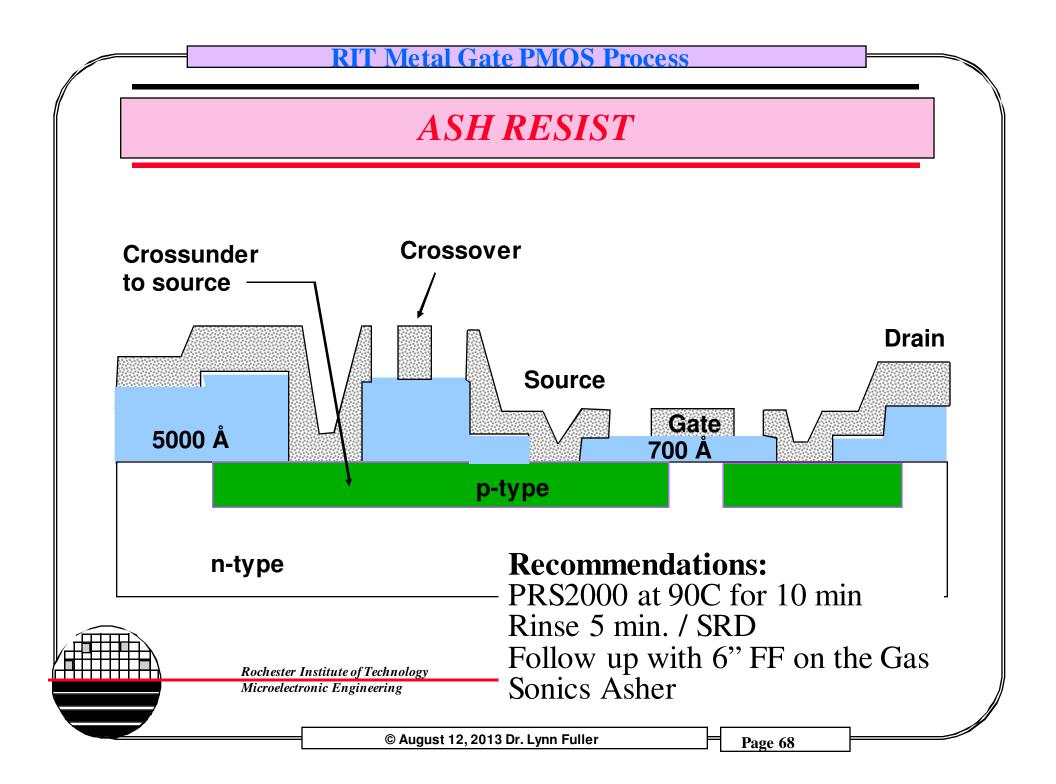
ALUMINUM ETCH USING LAM4600

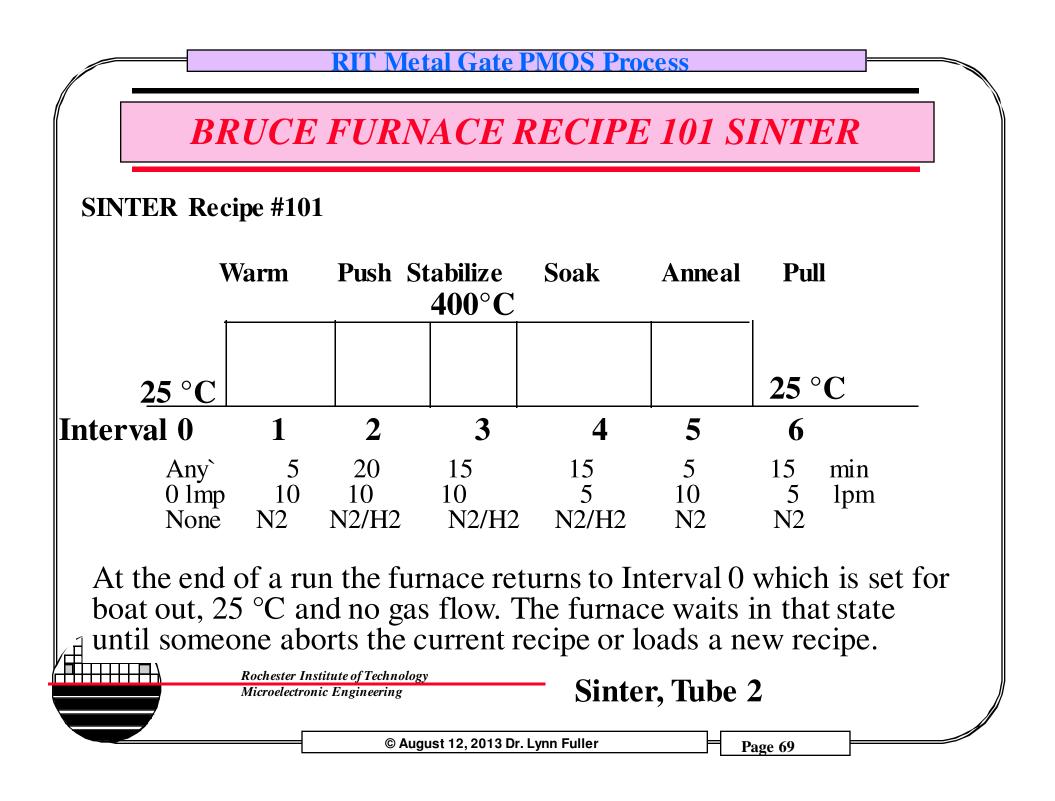


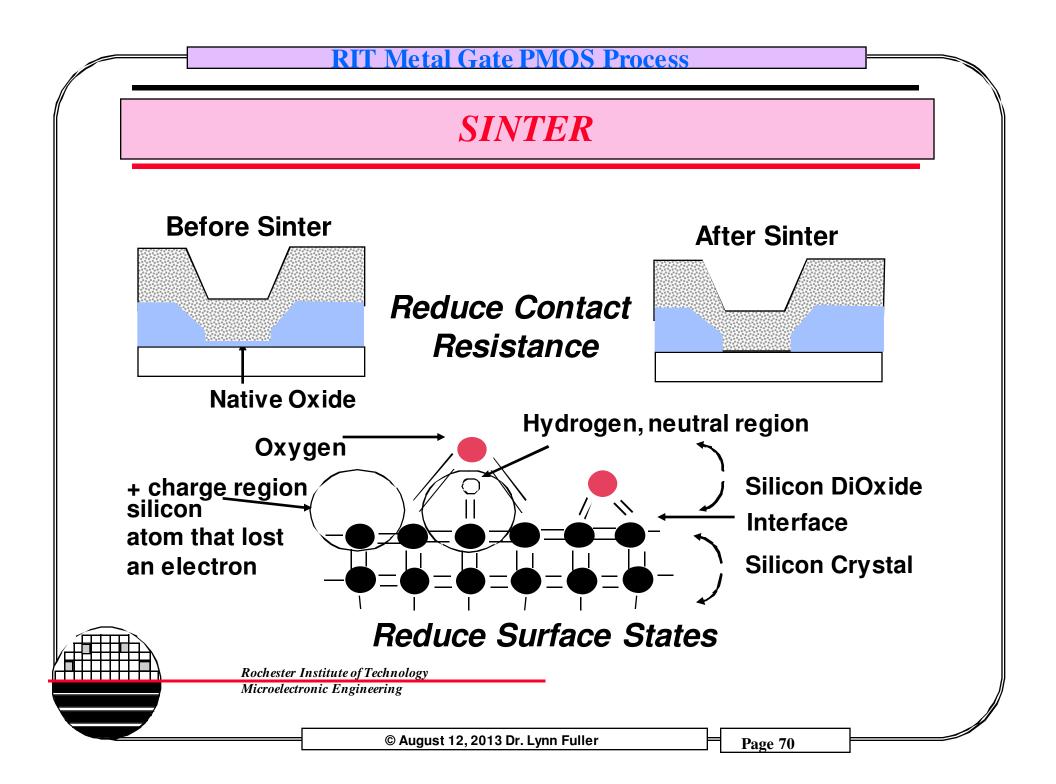
LAM4600 ANISOTROPIC ALUMINUM ETCH

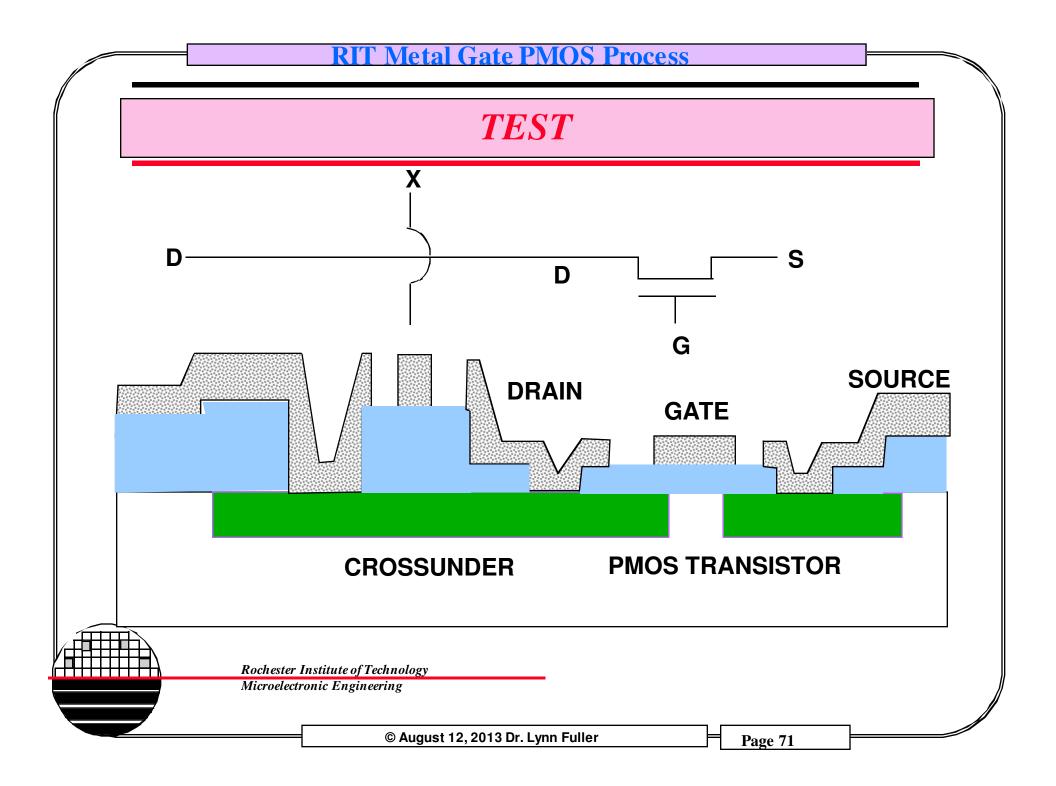
Step	1	2	3	4	5		
Pressure	100	100	100	100	0		
RF Top (W)	0	0	0	0	0		
RF Bottom	0	250	125	125	0		
Gap (cm)	3	3	3	3	5.3		
O2 111	0	0	0	0	0		
N2 222	13	13	20	25	25		
BCI 333	50	50	25	25	0		
CI2 444	10	10	30	23	0		
Ar 555	0	0	0	0	0		-
CFORM 666	8	8	8	8	8	Channel	В
Complete	Stabl	Time	Time	Oetch	Time	Delay	130
Time (s)	15	8	230	10%	15	Normalize	10 s
Fuller, May 2010						Norm Val	5670
Rochester Institute of Technology Microelectronic Engineering						Trigger	105%
						Slope	+
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TEST RESULTS

