

May 2001

**MICROELECTRONIC ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY**

Firsts for Microelectronic Engineering

Dr. Lynn Fuller

Motorola Professor and
Founder of Microelectronic Engineering
Rochester Institute of Technology

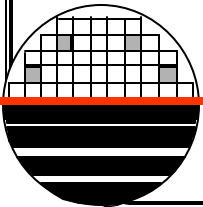
82 Lomb Memorial Drive
Rochester, NY 14623-5604

Tel (716) 475-2035

Fax (716) 475-5041

LFFEEE@rit.edu

<http://www.microe.rit.edu>

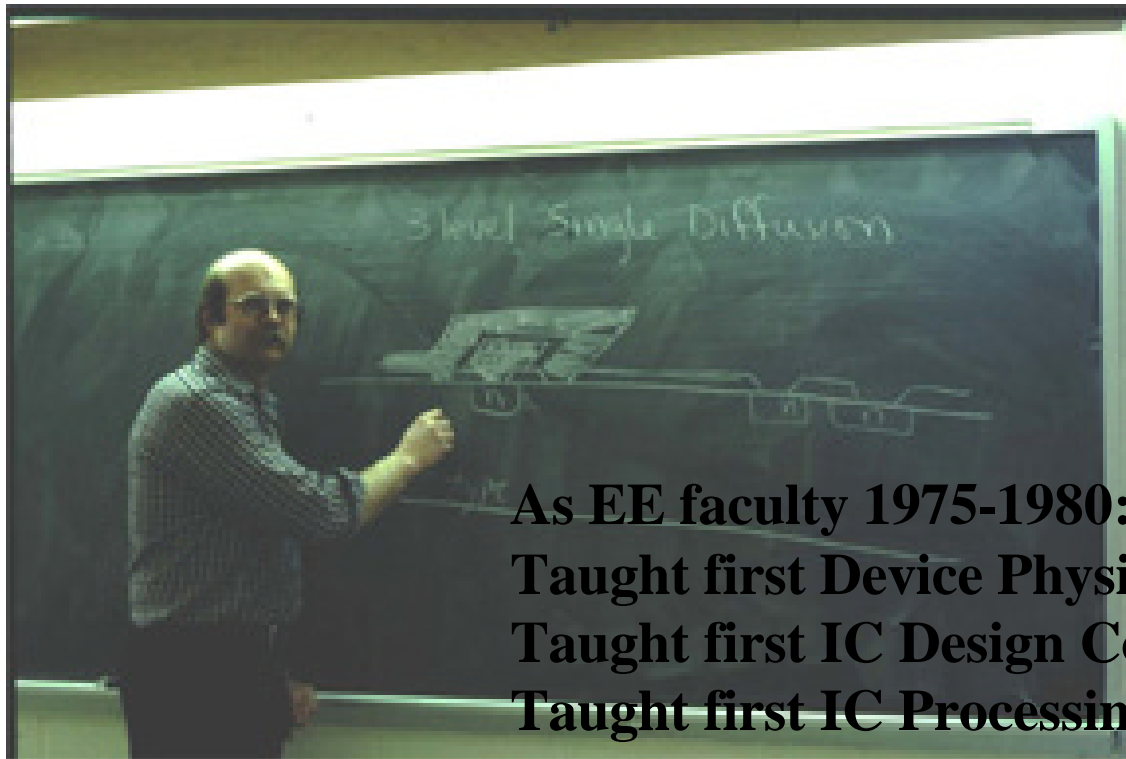


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5-14-2001

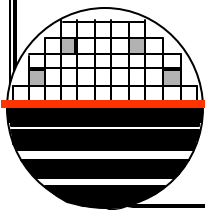
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DR. LYNN FULLER, FACULTY IN EE



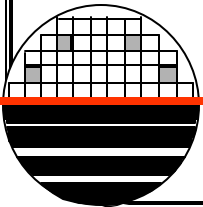
**As EE faculty 1975-1980:
Taught first Device Physics Courses
Taught first IC Design Courses
Taught first IC Processing Labs
Introduced SPICE to RIT
Made RIT's first transistors**

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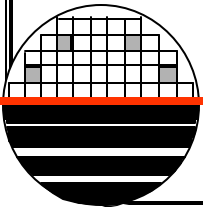
HISTORY

- 1982 Start of BS Program in Microelectronic Engineering - Dr. Lynn Fuller, Director; 55 Freshman, 10-2nd and 5-3rd Year Students; Hire Department COO Sara Widlund; Professor Pearson and Facilities Manager Scott Blondell**
- 1983 Hire Professor Turkman**
- 1984 Start plans for new building**
- 1985 Graduate first 5 students, Hire Professor Jackson**
- 1986 Honorary PhD to Jack Kilby, Move into new building, Hire Professor Lane and Technician One**
- 1987 ABET Accreditation of BS program, Graduate first 5 year RIT Students, SRC Program for Micro Manufacturing Engineering Masters Degree, Hire Professor Kurinec**
- 1988 Start student run factory, Graduate first Masters students, Hire Professor Smith and Technician Two**



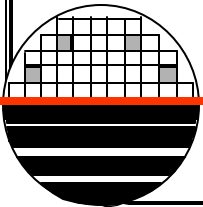
HISTORY

- 1989 Dedicate Perkin Elmer Laboratory for Electron Beam Lithography**
- 1990 Imaging Science Ph.D. Program IBM CIM in Higher Education**
- 1991 Dedicate Excimer Laser Laboratory, Ranked 1st in SRC Survey**
- 1992 10 Annual Conference, ABET Visit No. 2**
- 1993 B.S. Program Curriculum Changes, Hire Professor Hirschman**
- 1994 Dr. Lynn Fuller named Motorola Professor**
- 1995 MSMME Program approved and started, First SEMATECH Research Contract**
- 1996 Process first 6 inch wafers, Intel becomes affiliate member**



HISTORY

- 1997 NEC, Nikon, Canon, & Micron Become affiliate members**
- 1998 Hire Professor Philip Rack, Start Distance Offering of Masters Program, ABET visit No. 3**
- 1999 ABET Certification No 3**
- 2000 ASM Lithography, Air Products and Photonics become Affiliates, Hire Professor William Grande, Dale Ewbank, Suraj Bhaskaran. Dr. Bruce Smith becomes the Intel Professor**
- 2001 Dr. Santosh Kurinec becomes Department Head**
- 2002 20th Year Celebration, Hire Professor Sean Rommel**
- 2003 Start of Ph.D. Program in Microsystems Engineering**
- 2004 Bruce Smith starts Amphibian Systems Inc.**
- 2005 First Ph.D. Graduates in Microsystems Engineering**
- 2006 Dr. Hirschman named Micron Professor**
- 2007 25th Year**

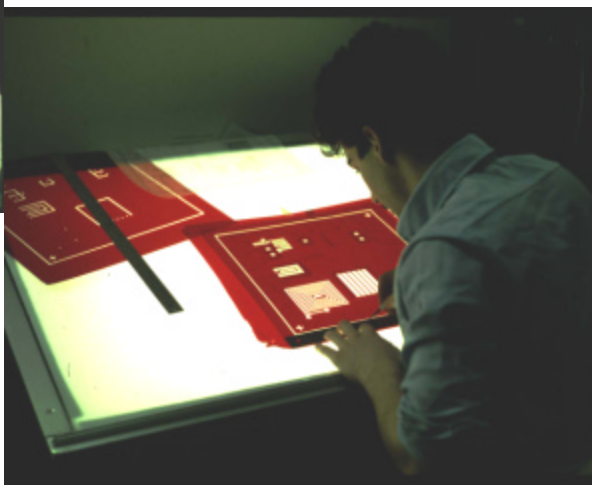


EARLY IC LAYOUT AT RIT

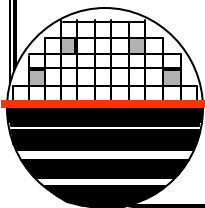


Drawing of Layout

Rubylith for each Layer



Design Rule Check



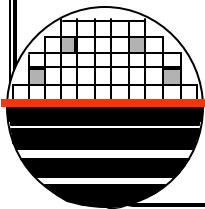
EARLY LITHOGRAPHY AT RIT



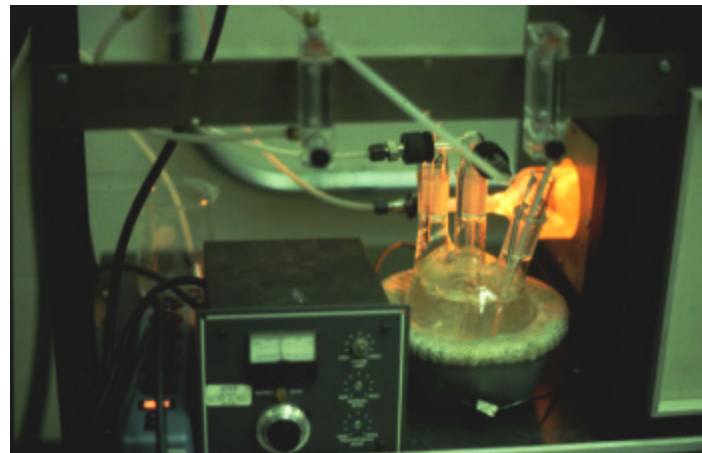
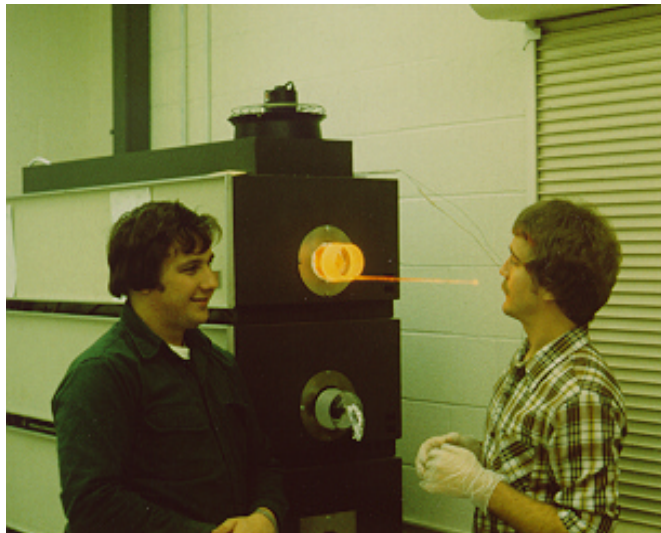
Kasper contact aligner on 2x4 blocks.
Notice homemade reduction camera.



Hamilton Beech Blender
Modified for spin
coating resist on wafers.
Purée gives coating
thickness of $\sim 1 \mu\text{m}$

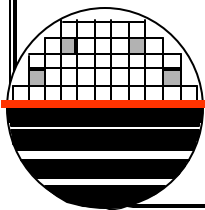


OXIDE GROWTH AND DIFFUSION AT RIT

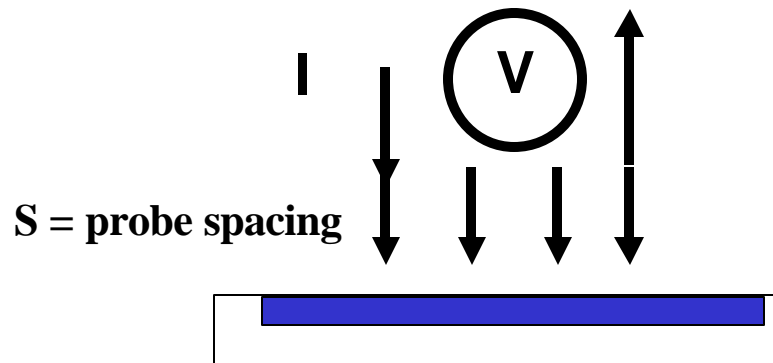
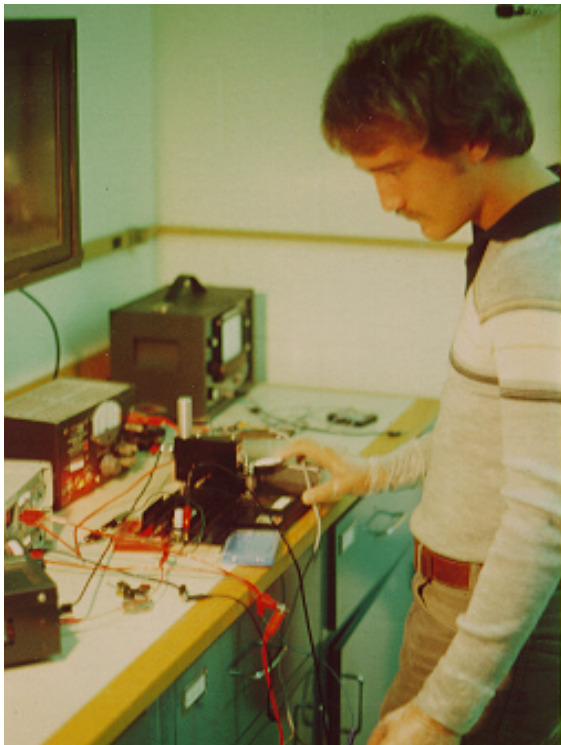


Gas flow and bubbler system

Students Jim Razzak and Rob Pearson do oxide growth on 2" wafers.



FOUR POINT PROBE AT RIT

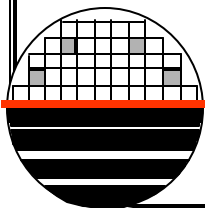


x_j = Diffusion Layer Thickness

$$\text{Rhos} = \frac{\rho}{\ln 2} \times V / I = 4.532 V/I \text{ ohms/sq}$$

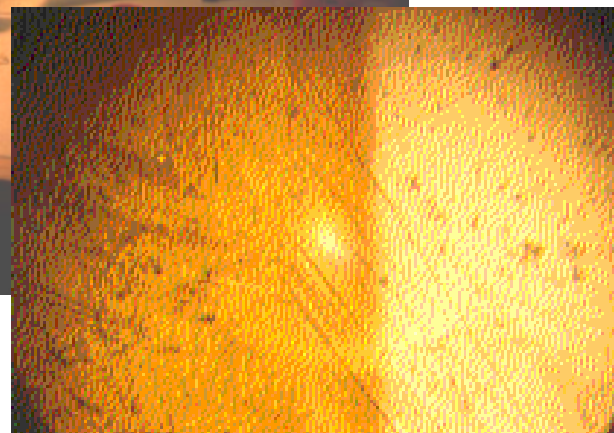
,if $S > x_j$

Use FORTRAN program on VAX
RUN USER:[MICROLIB.TOOLS]FOURPT



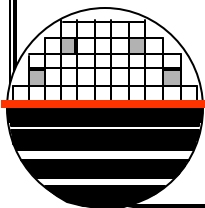
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RIT'S FIRST ANGLE LAP AND STAIN XJ MEASUREMENT



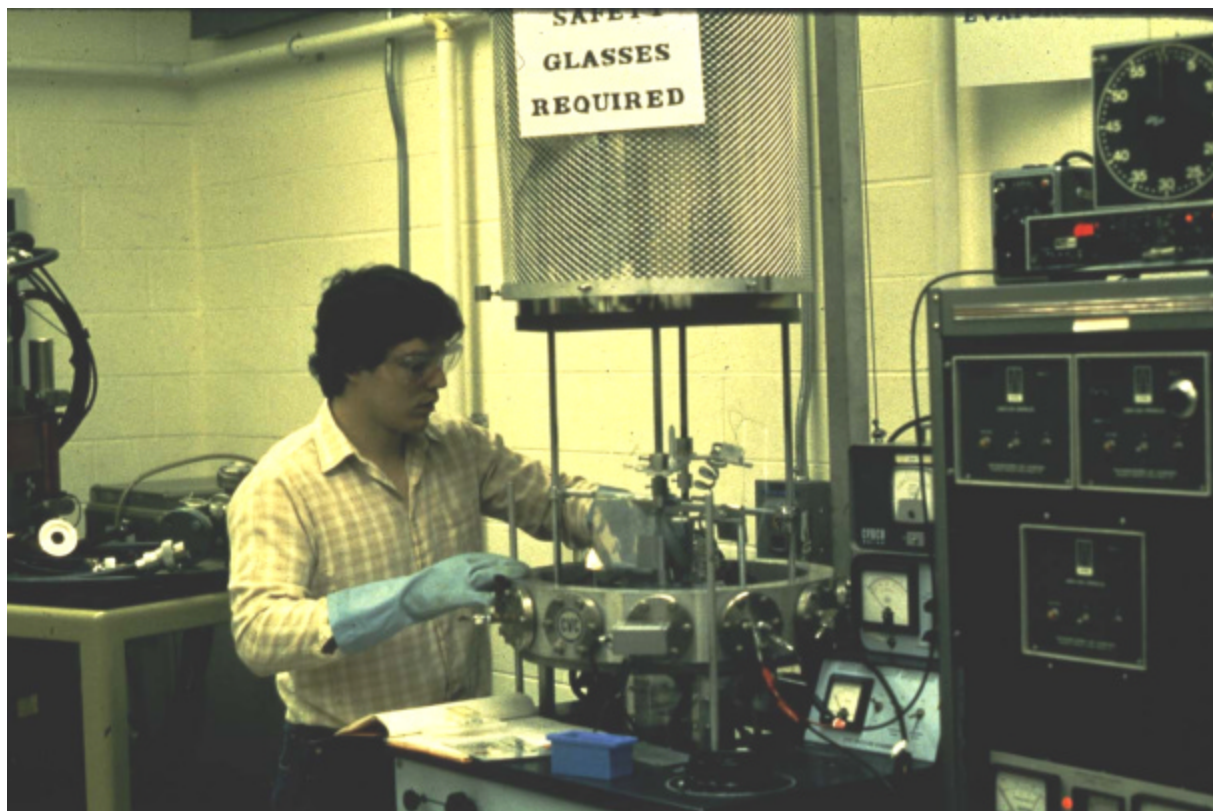
Chris Knaus

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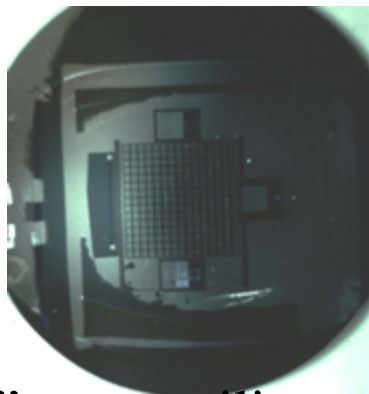
RIT'S FIRST METALLIZATION SYSTEM



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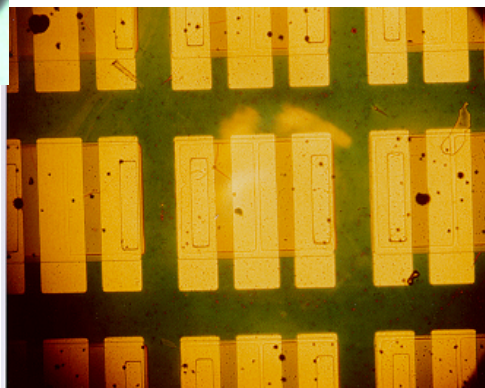
Summer 1979

FIRST RIT PMOS TRANSISTOR



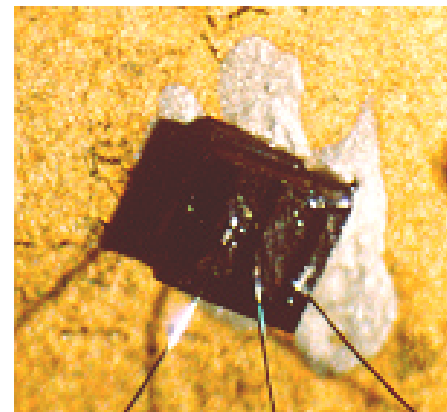
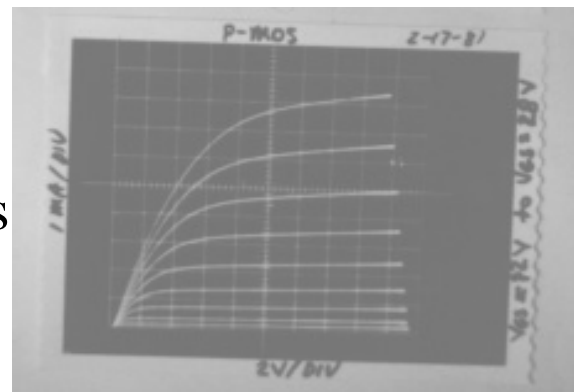
2" n-type silicon wafer

2-17-81

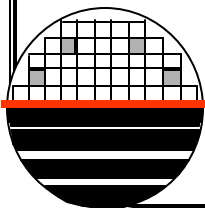


PMOS Transistors

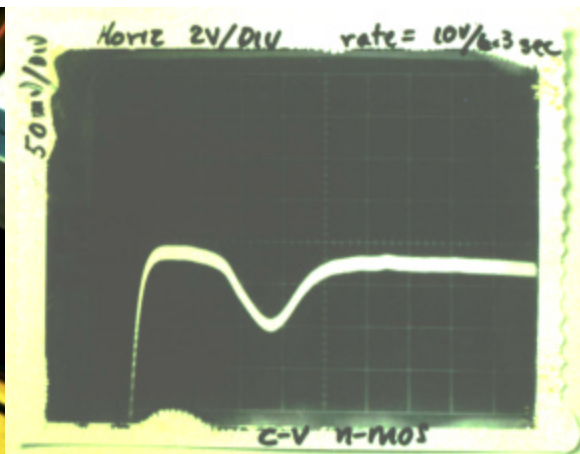
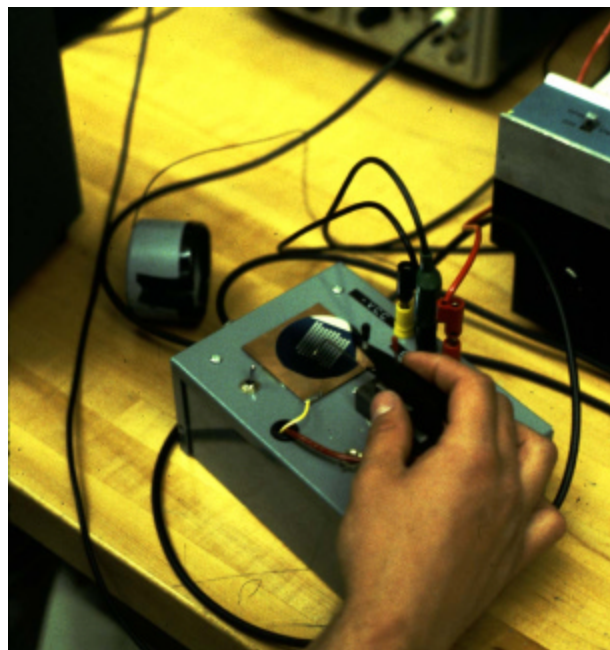
$V_t = 12$ volts



Packaged Device
Aluminum wire bonds

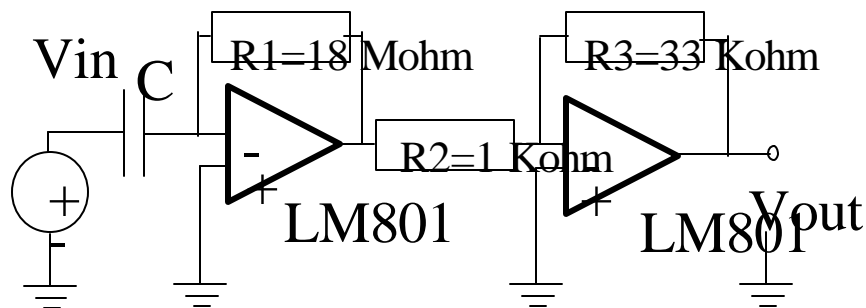


LOW FREQUENCY CV MEASUREMENTS

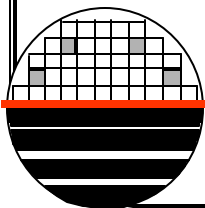


Homemade C-V Measurement System

1 V/sec
Ramp

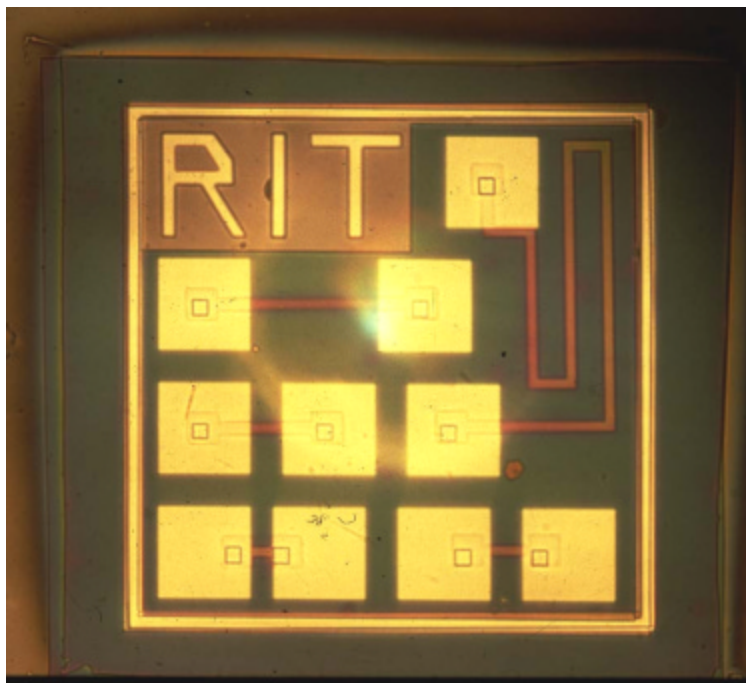


$$V_{out} = (C R_1 R_3 / R_2) (dV_{in}/dt)$$



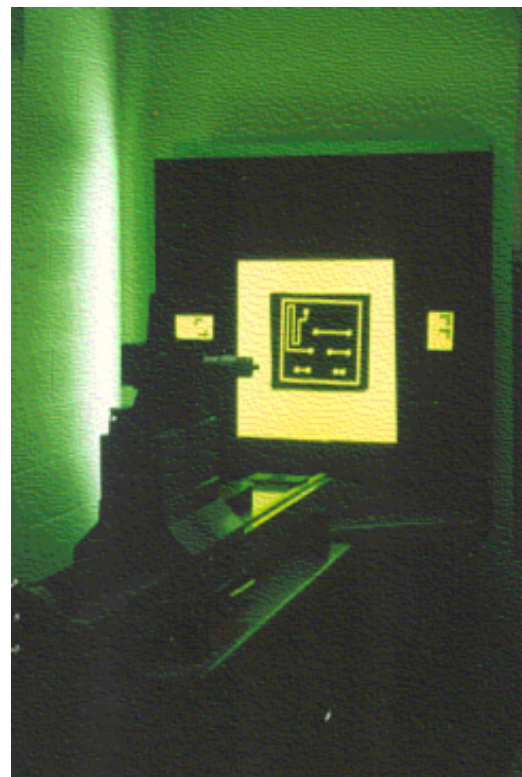
RIT'S FIRST DIFFUSED RESISTORS

P-type diffused resistors in an n-type wafer.

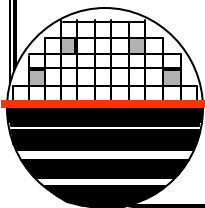


Completed chip.

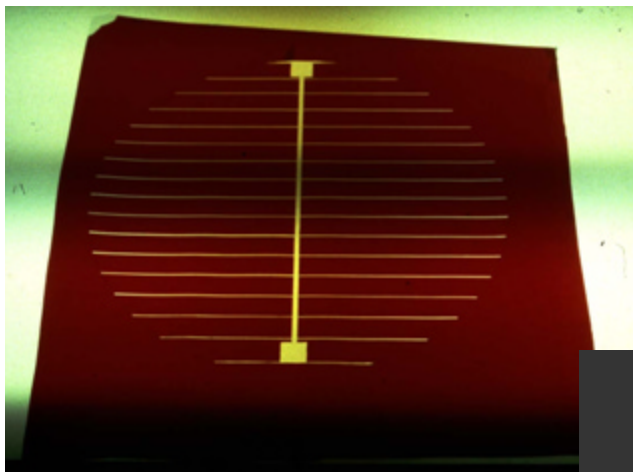
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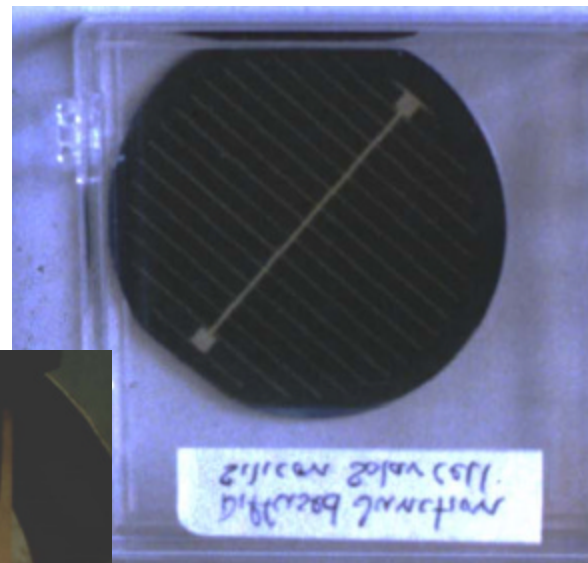
Maskmaking



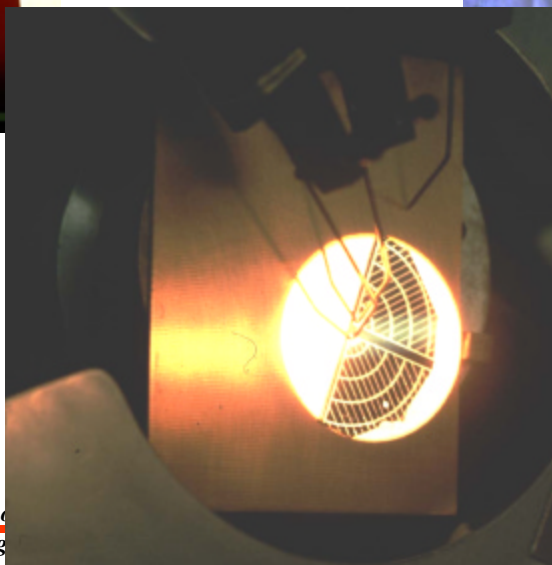
RIT'S FIRST SOLAR CELLS



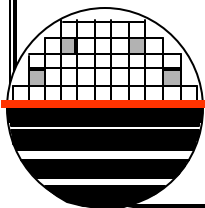
Layout



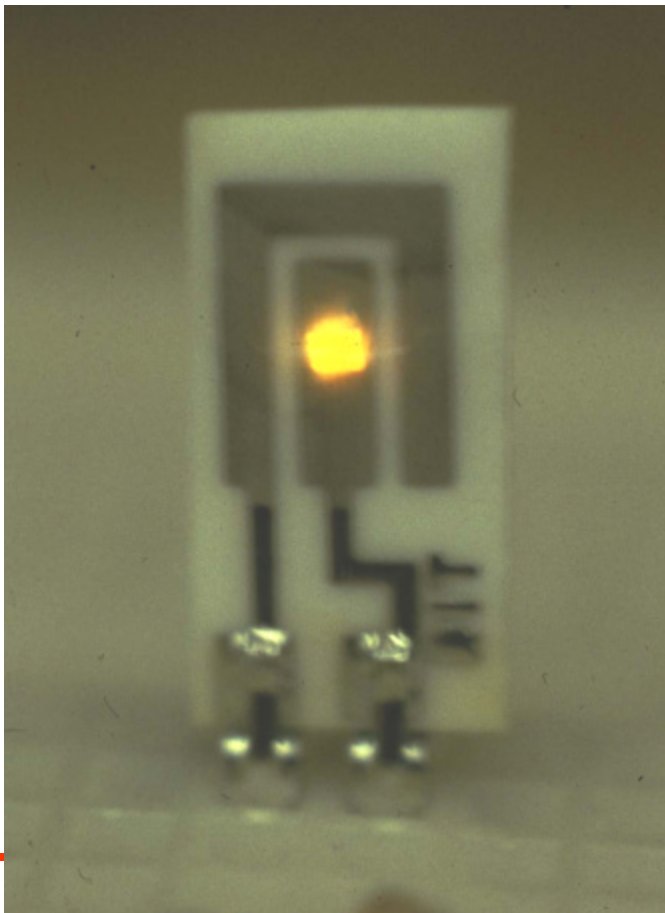
Completed device.



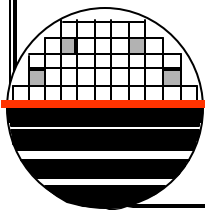
Testing



RIT'S FIRST GALLIUM PHOSPHIDE LED



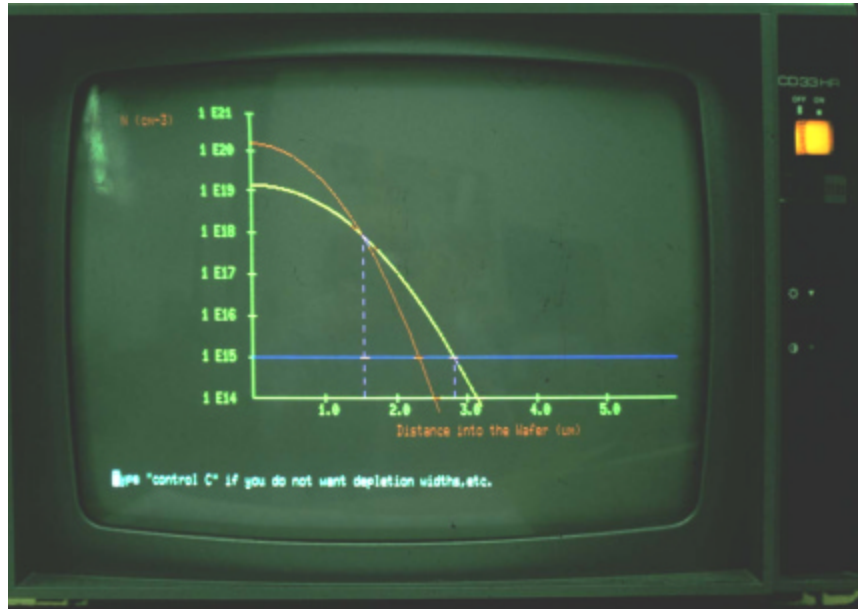
GaP wafers with n-type epilayer, add gold metal, dice and wire bond to RIT thick film ceramic package.



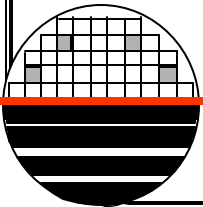
RIT FIRST TO OFFER MICRO MAJOR



RIT BISIM PROCESS SIMULATOR



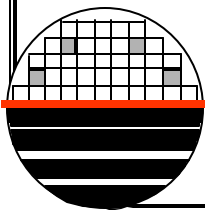
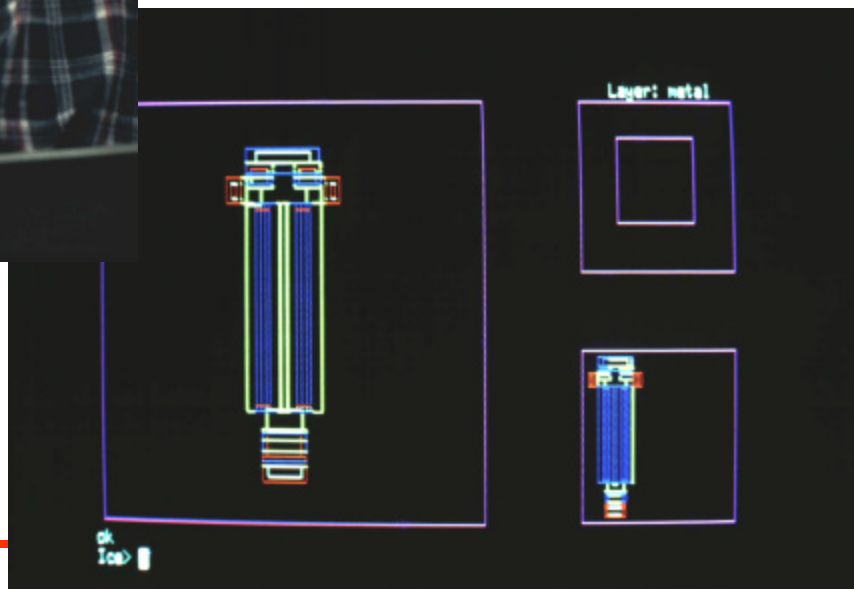
Chris Ludden wrote a FORTRAN program for simulation of diffusion and calculation of space charge layer thickness, sheet resistances and transistor current gain. This software was equivalent to SUPREM being developed at Stanford University at the same time.



RIT ICE LAYOUT EDITOR



Taylor Hogan created a “C” program for layout of integrated circuits. Output in Mann 2000 format for our optical pattern generator.

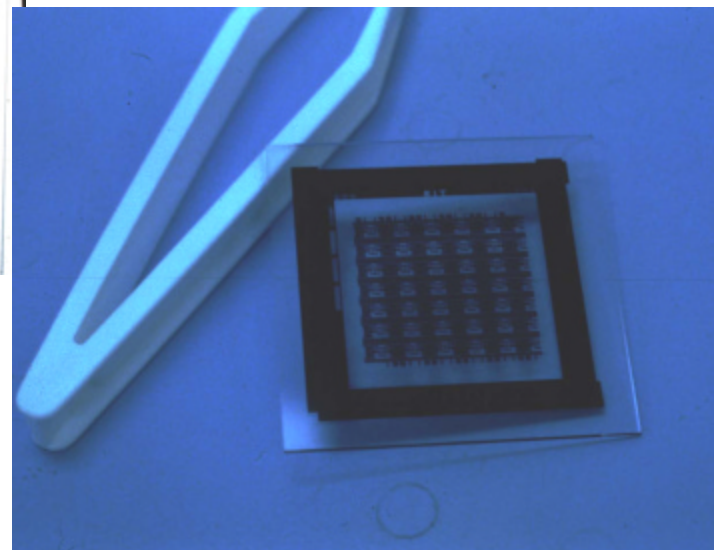


RIT'S FIRST OPTICAL PATTERN GENERATOR

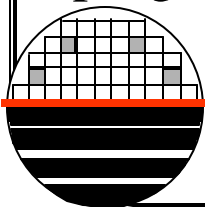


Mann 2000 PG

Ed Barry was the department technician for the 1st year of the program.



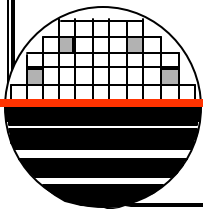
Reticle for Photorepeater



RIT'S FIRST PHOTOREPEATER

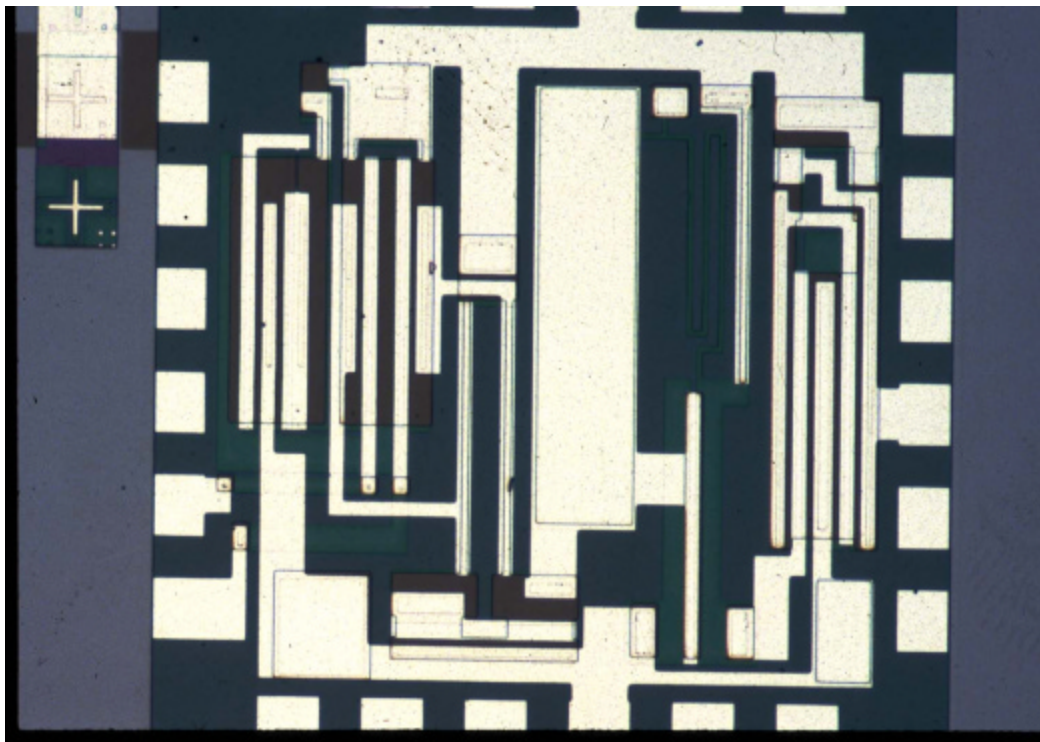


Jim Kawski makes 1X Photomask using RIT's photorepeater. The 1X masks were emulsion on glass.



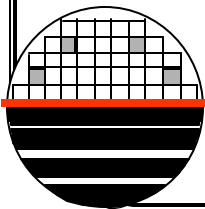
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RIT'S FIRST ALL PMOS OP AMP DESIGN



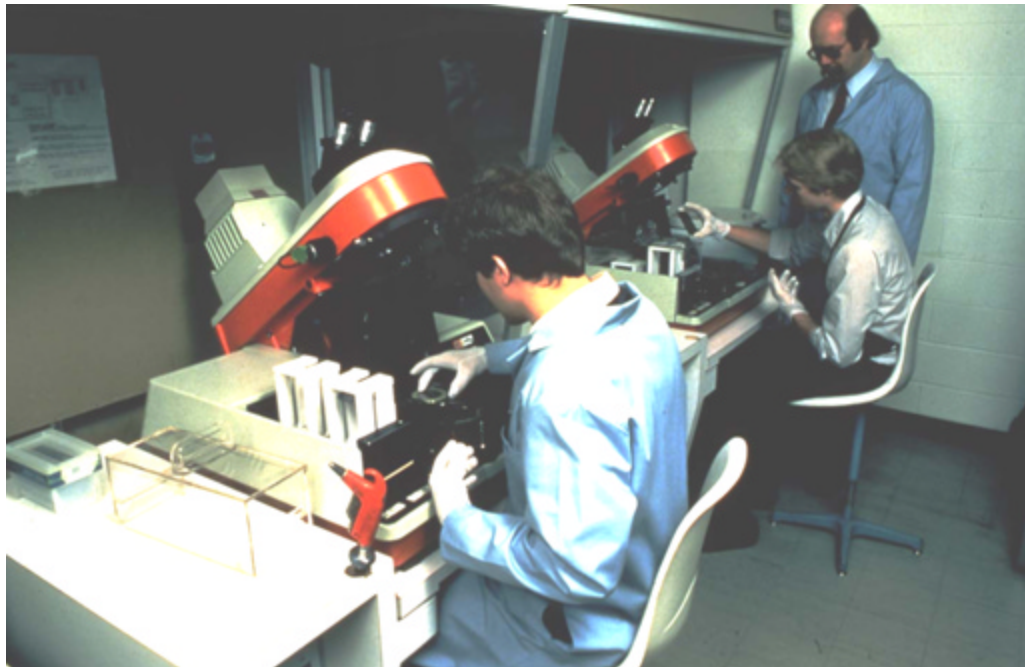
Jonathan Littlehale

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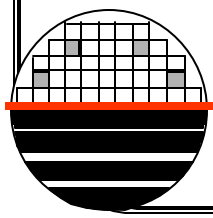
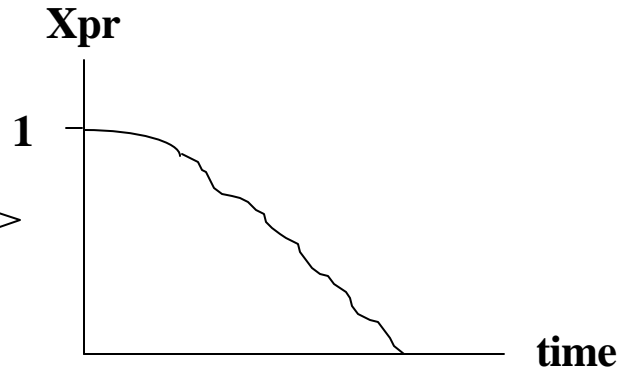
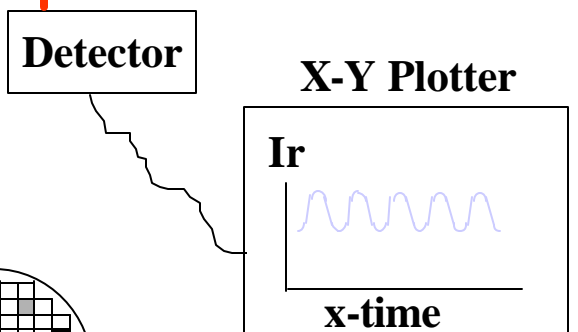
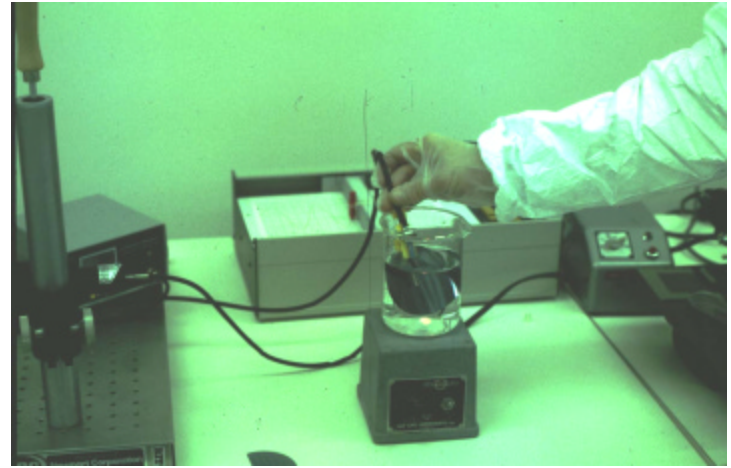
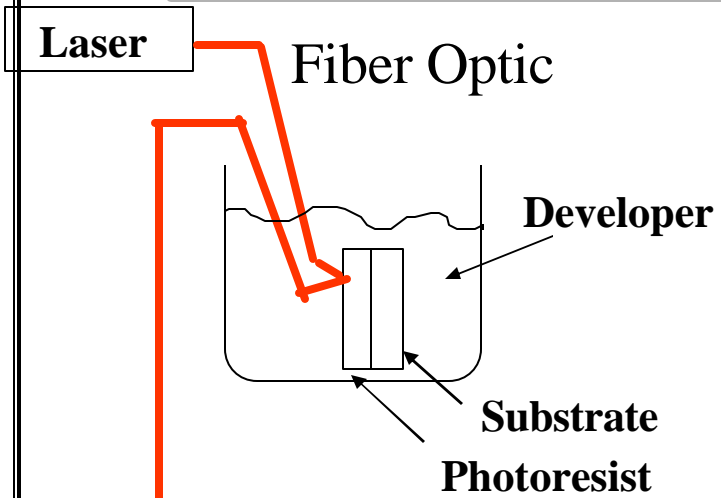
RIT'S FIRST LITHOGRAPHY COURSES



RIT was the only university to teach undergraduate lithography courses. UC Berkeley taught some courses at the graduate level. Even today few universities teach lithography courses.

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RIT'S FIRST DEVELOPMENT RATE MONITOR



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RIT'S FIRST GCA WAFER TRACK



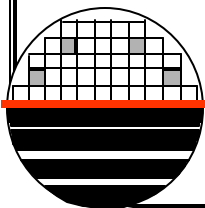
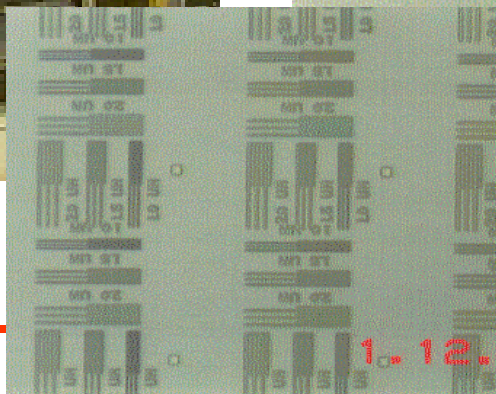
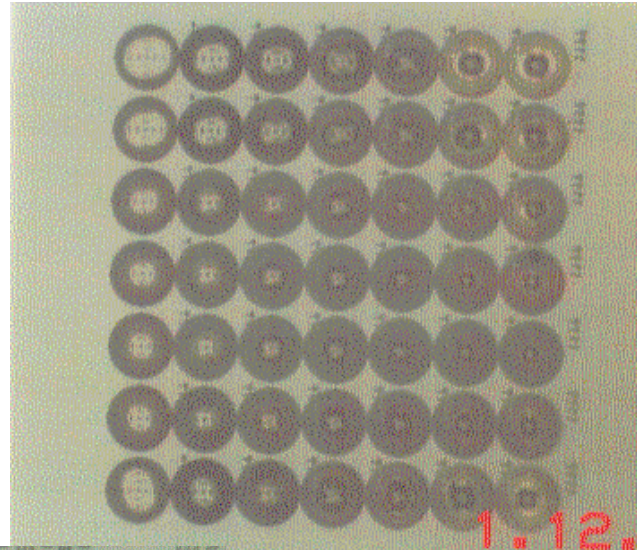
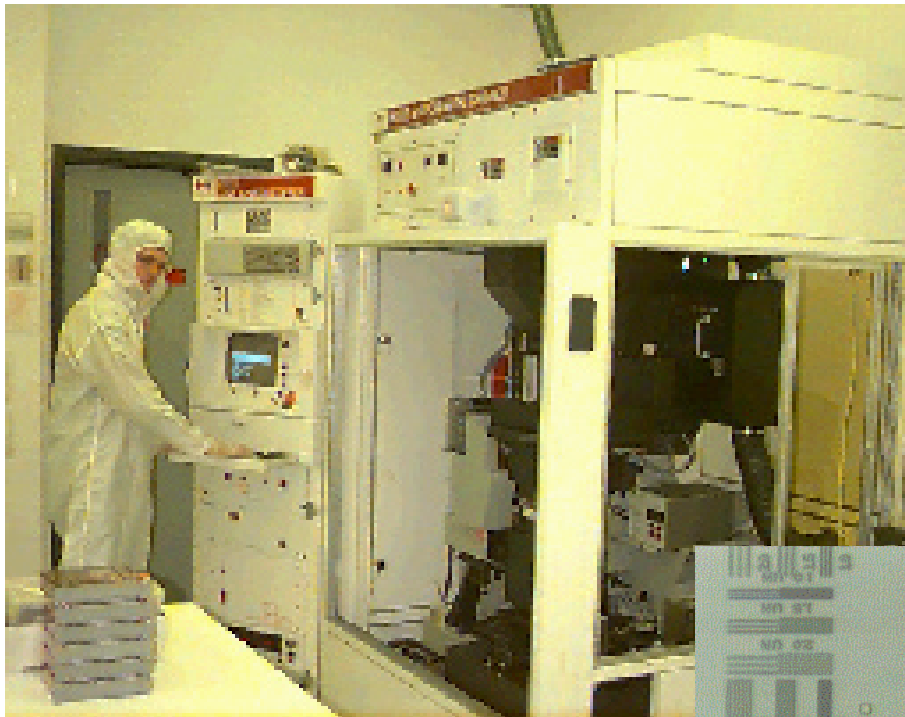
Used for process development and characterization laboratory.

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Scott Blondell

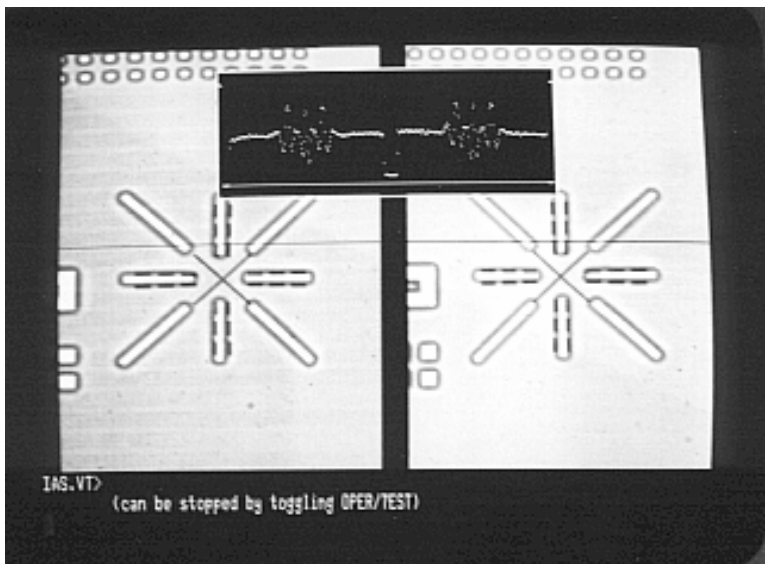
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RIT FOCUS AND EXPOSURE LAB

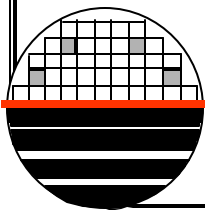
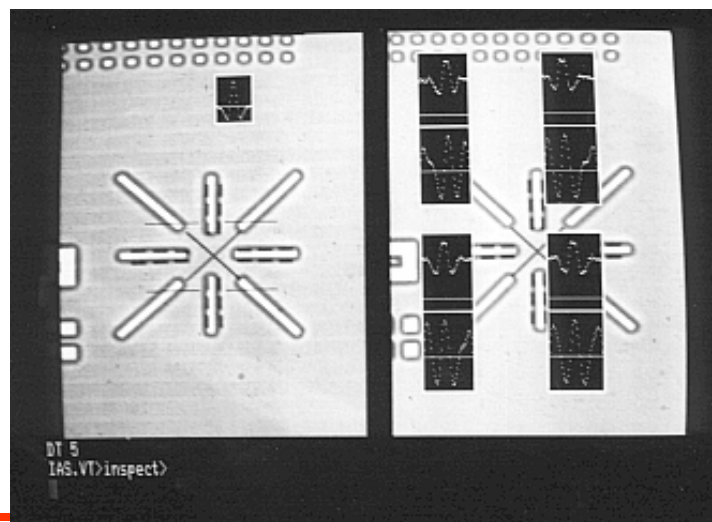


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AUTOMATIC OVERLAY LAB

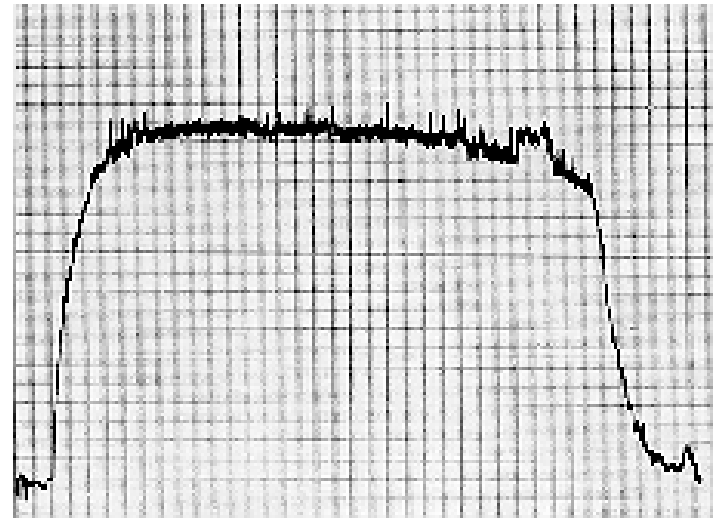


GCA 6700 Overlay Setup Images



FIRST END POINT DETECTION AT RIT

O₂, 30 sccm, 50 watts, 300 mTorr



0.0 TIME (min) 8.0

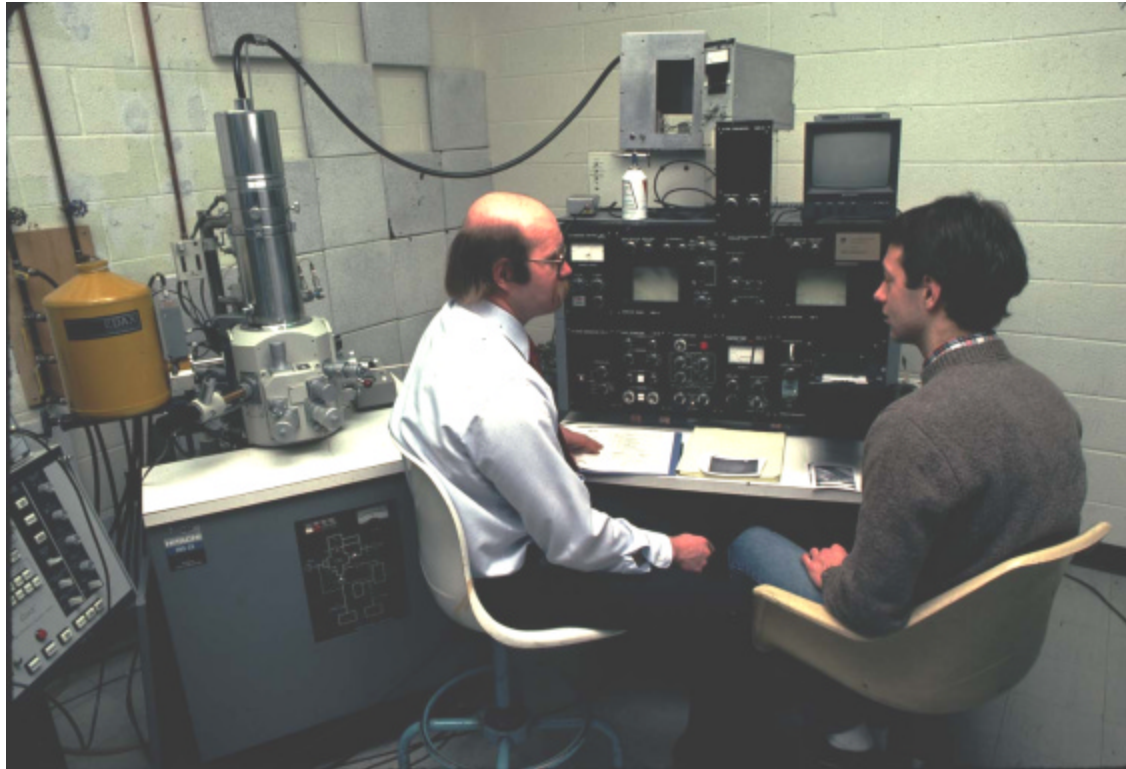
Monitor the CO peak at 483.5 nm. During photoresist stripping there are large numbers of CO molecules. At end of Photoresist stripping the number of CO molecules is reduced.

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Dick Lane

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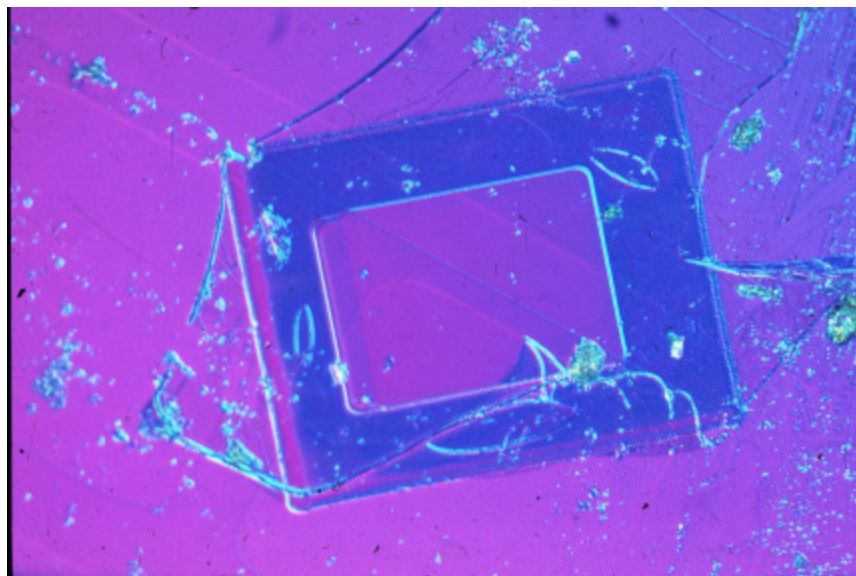
RIT'S FIRST SEM



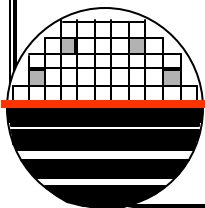
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FIRST E-BEAM LITHOGRAPHY AT RIT



Using a SEM we obtained thickness log dose curves.



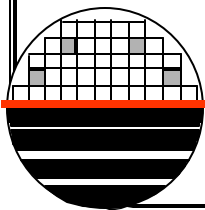
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FIRST RIT IC PROCESSING SHORTCOURSE



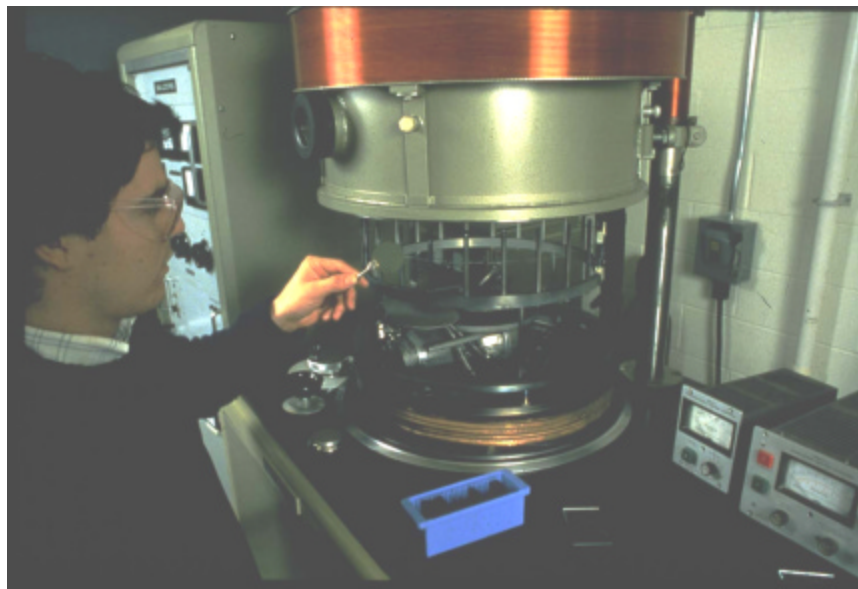
Students in first RIT IC processing short course. 1000's of students have taken our short courses over the years.



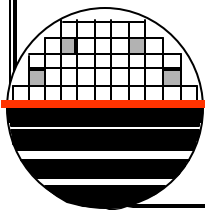
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FIRST SPUTTERING AT RIT



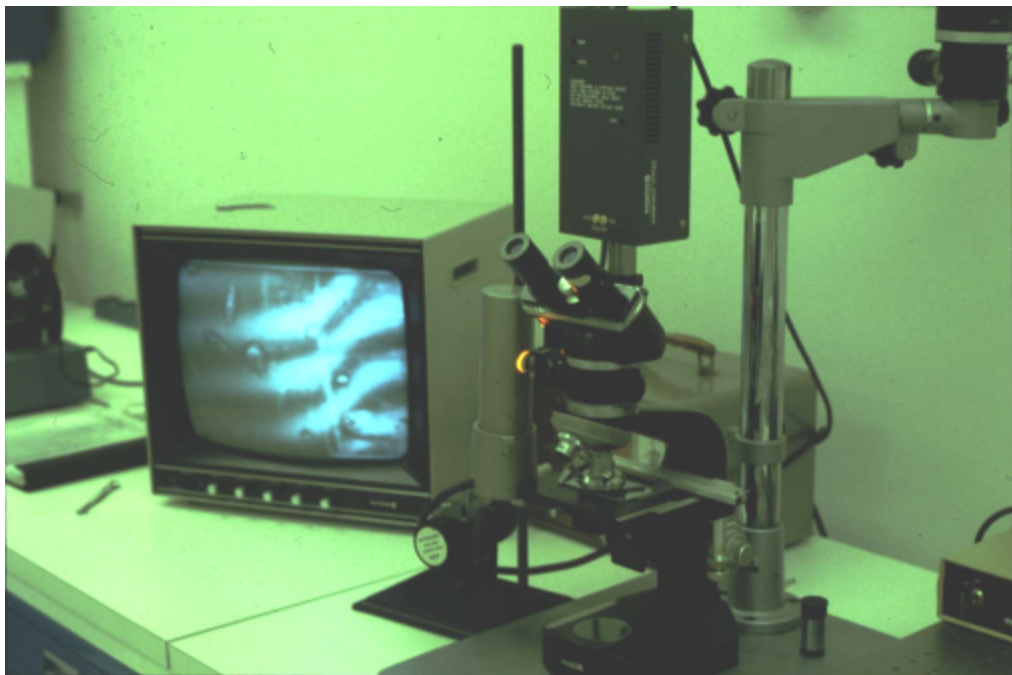
Juan Becerra sputtering in Balzars sputter tool.



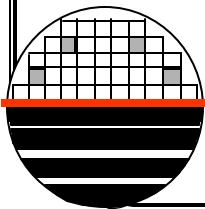
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RIT'S FIRST THICKNESS MEASUREMENT



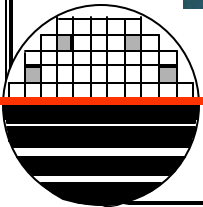
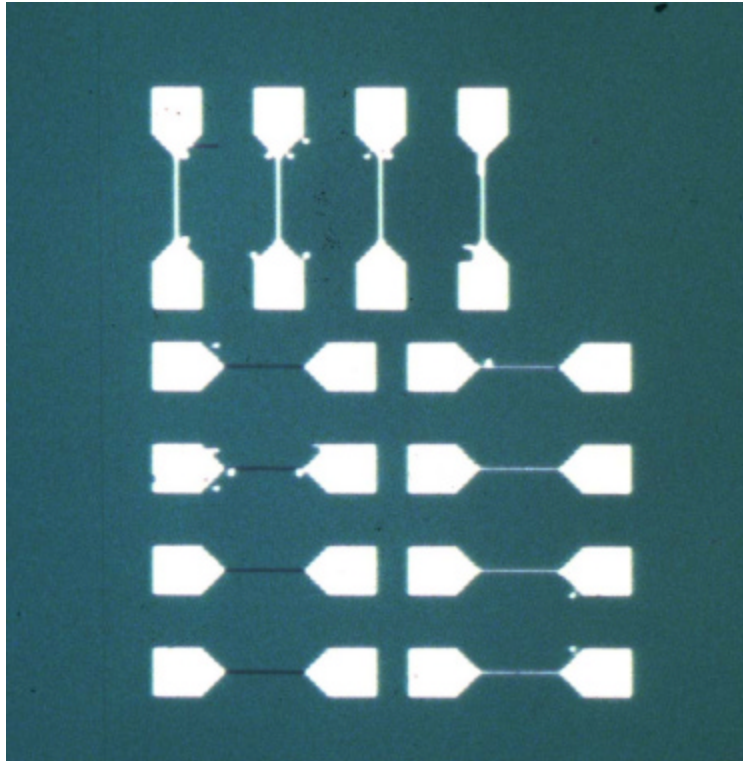
Interference microscopy for thickness measurement of opaque films.



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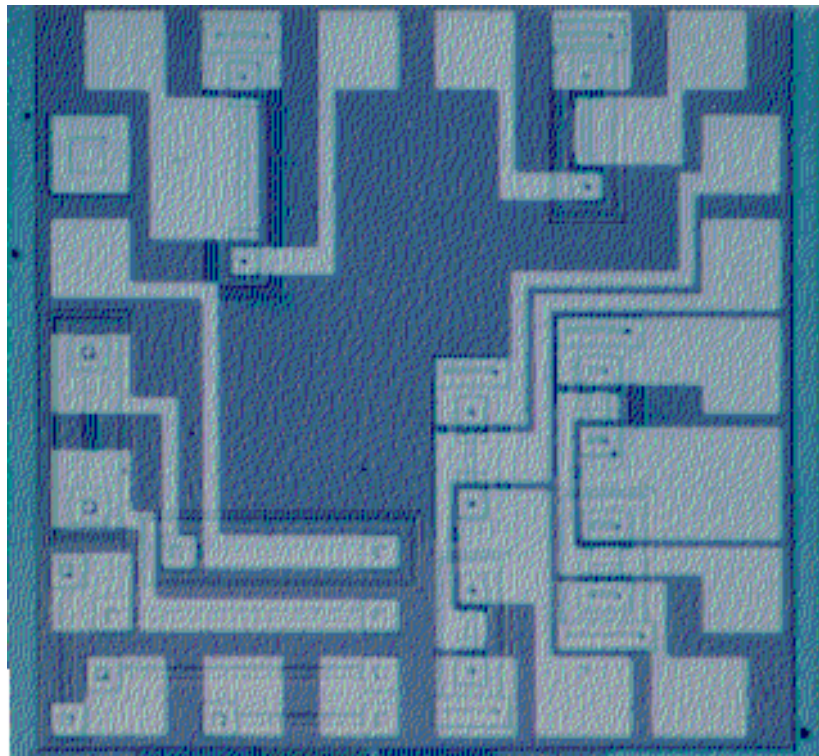
FIRST ELECTROMIGRATION STUDY RIT



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FIRST METAL GATE CMOS



Jim Pollard builds first metal
Gate CMOS, 1987

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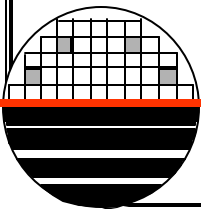
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FIRST \$50,000 OF MOTOROLA'S \$2,000,000

Dick Kenyon
Roger Hewett
Lynn Fuller
Fred Tucker



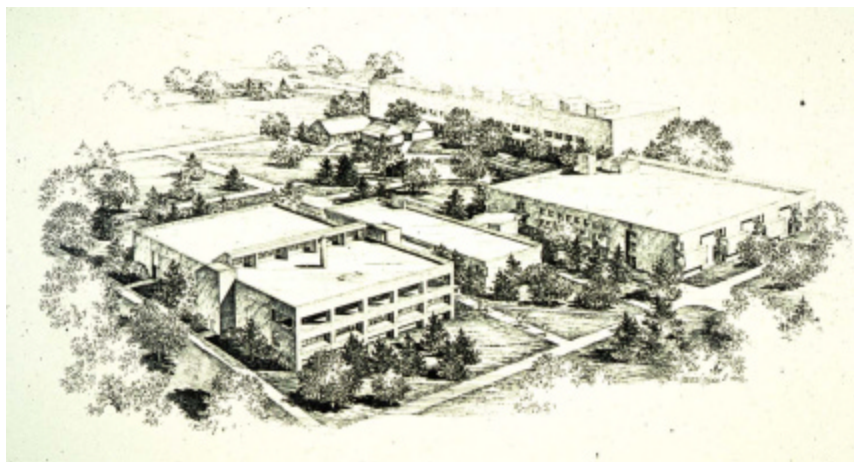
\$50,000



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Microelectronic Engineering*

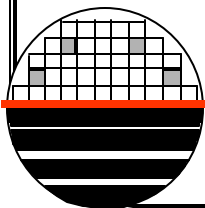
May 2001

THE NEW BUILDING



The department faculty and staff.
Dr. Turkman, Lynn and Sara missing.

Affiliate representatives



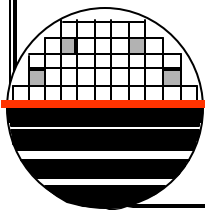
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RIT'S FIRST ION IMPLANTER



Varian 400 ion implanter.

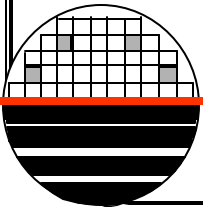


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Lynn Fuller
Scott Blondell

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RIT'S FIRST LPCVD POLY AND NITRIDE



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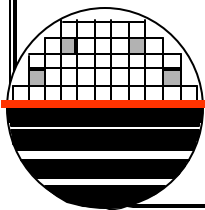
May 2001

RIT'S FIRST POLY AND NITRIDE ETCH TOOL



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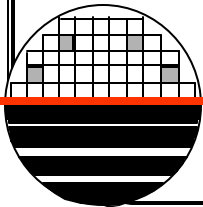
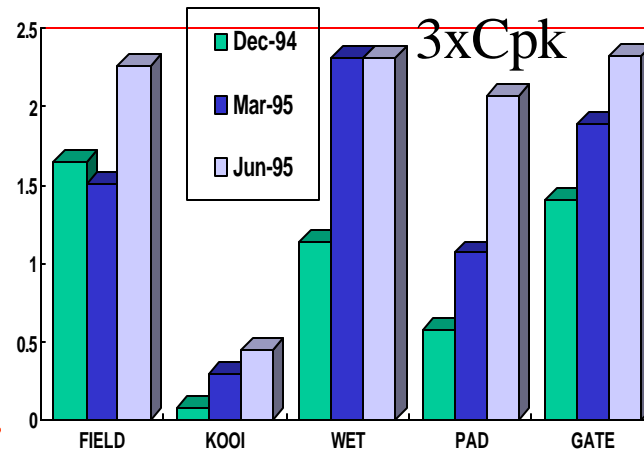
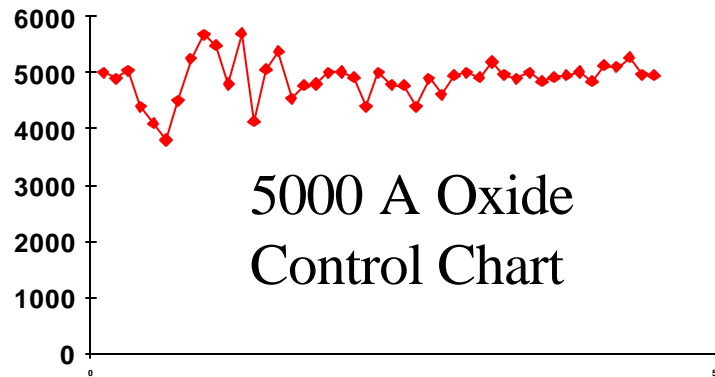
Dick Lane
Tom Grimsley



RIT'S MESA WIPTRACKING SYSTEM

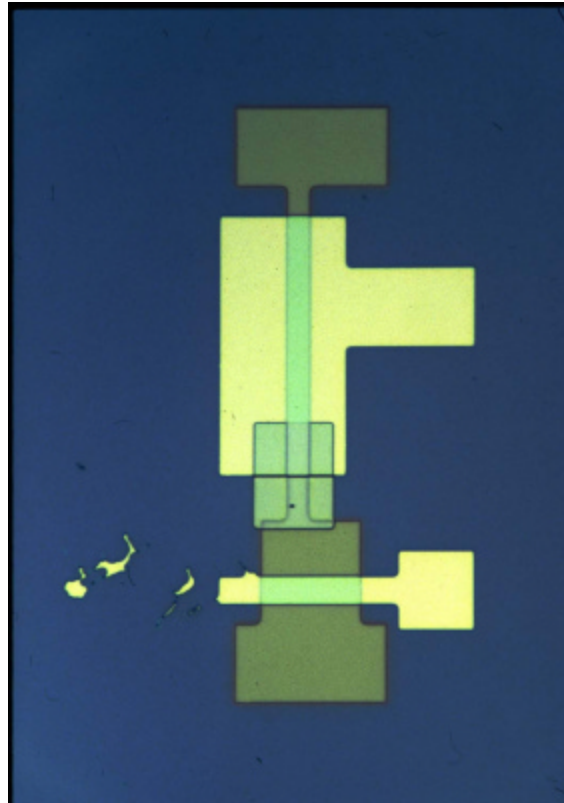


MESA Software
AS/400 Hardware

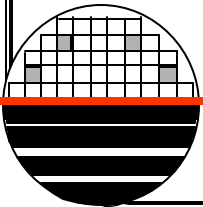


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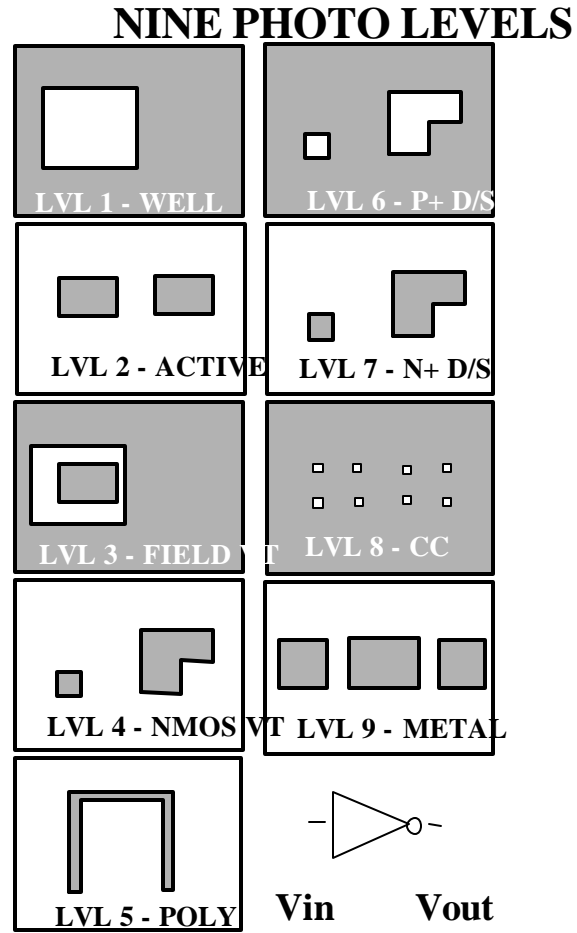
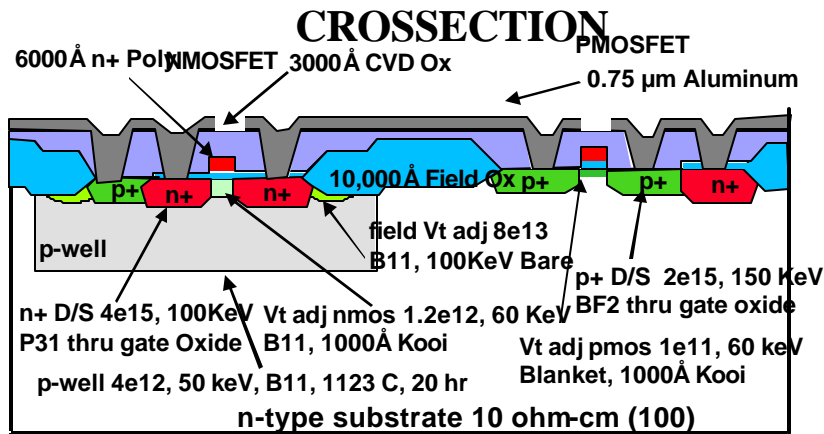
RIT'S FIRST NMOS INVERTER



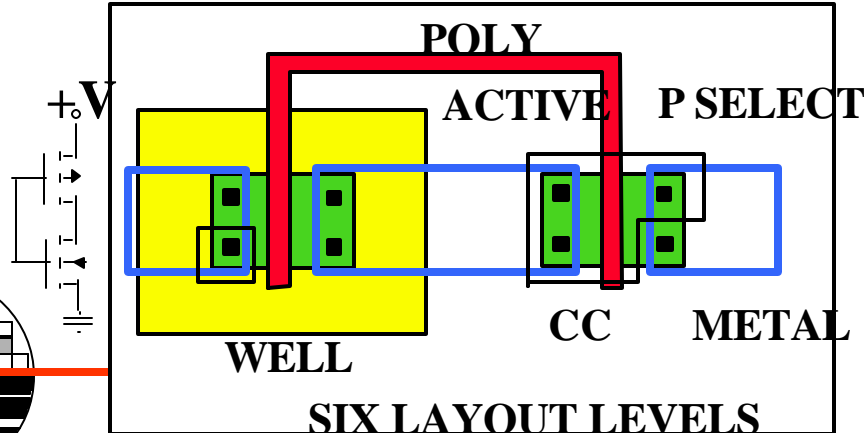
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RIT'S FIRST CMOS PROCESS

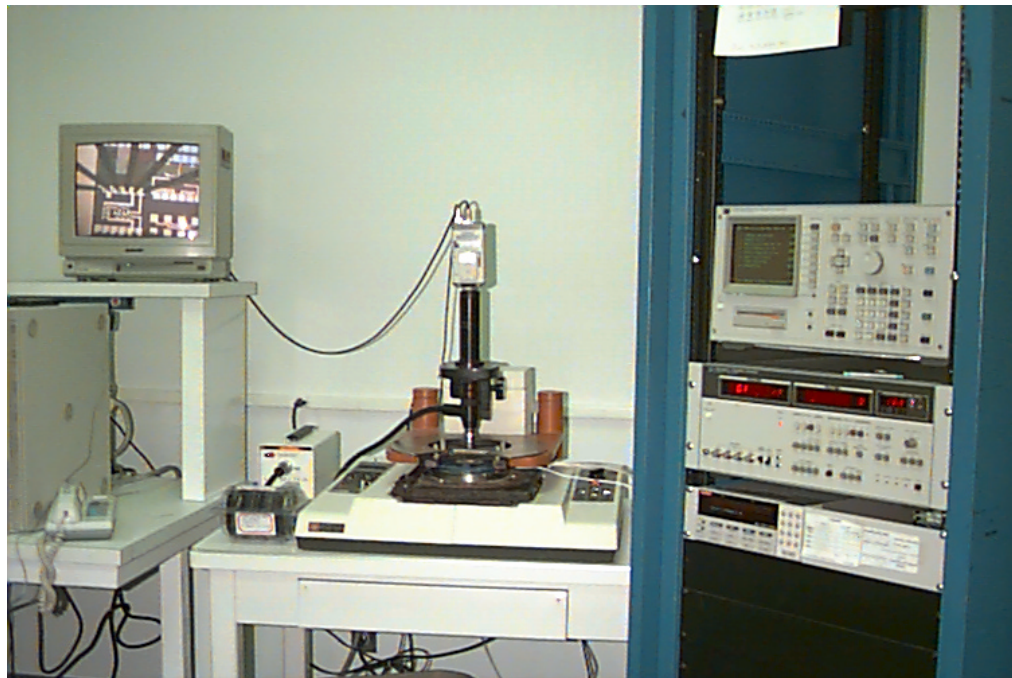


PLAYBACKNEXT

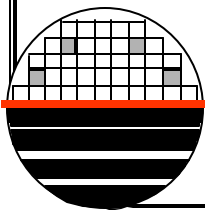


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RIT'S FIRST ANALOG PARAMETRIC TESTER



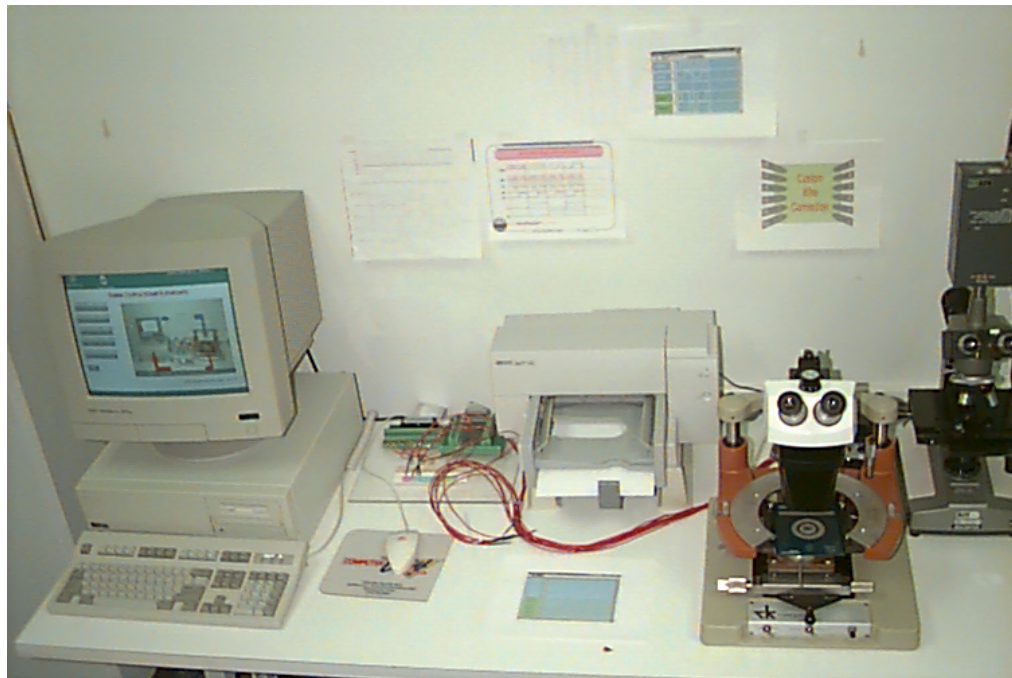
Rob Pearson



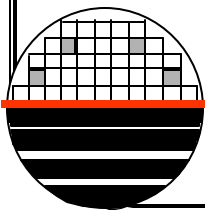
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RIT'S FIRST DIGITAL TEST SYSTEM



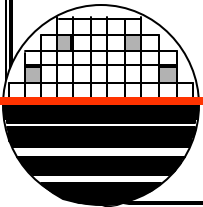
Suphong Yunrudee
Joanna Kiljan



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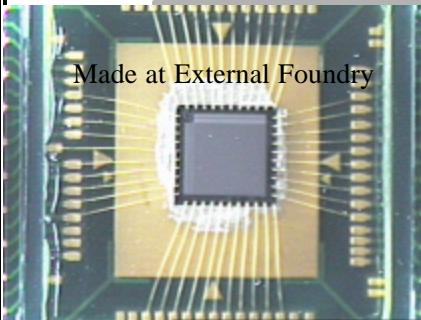
May 2001

MEBES MASKMAKING 1990

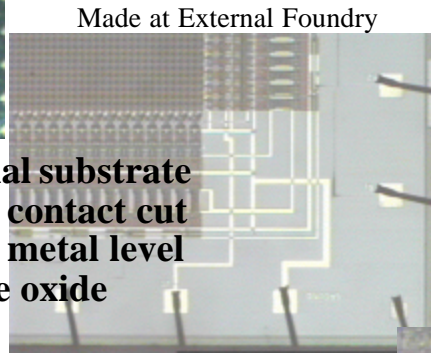


Rochester Institute of Technology
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RIT'S FIRST CID IMAGER CHIP



Made at External Foundry



Made at External Foundry

PMOS on n-type epitaxial substrate
6 micron gate, 4 micron contact cut
Double poly-silicon, one metal level
15 V process, 50 nm gate oxide

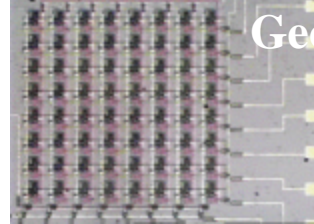
8 Photo levels

- Active
- Poly-1
- Poly-2
- p+ D/S Implant
- n+ Substrate Contact
- Pinning Implant
- Contact Cut
- Metal

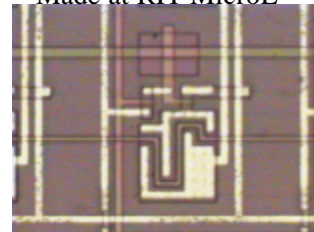
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800

Made at RIT MicroE



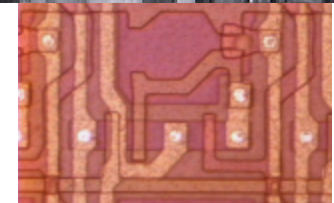
Made at RIT MicroE



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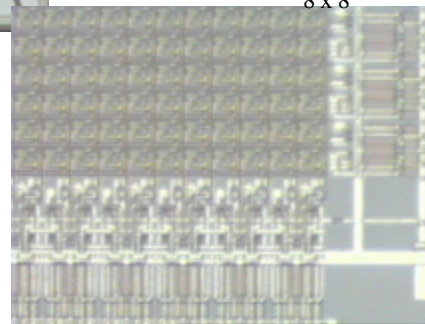
George Lungu



54 x 40

10,000

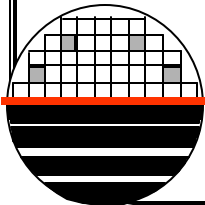
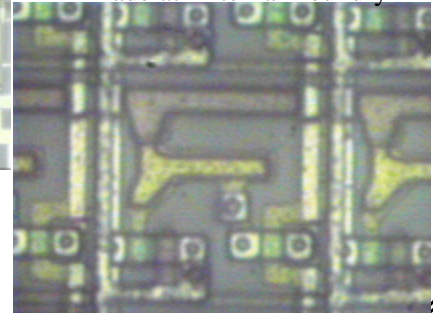
Made at External Foundry



128 x 128

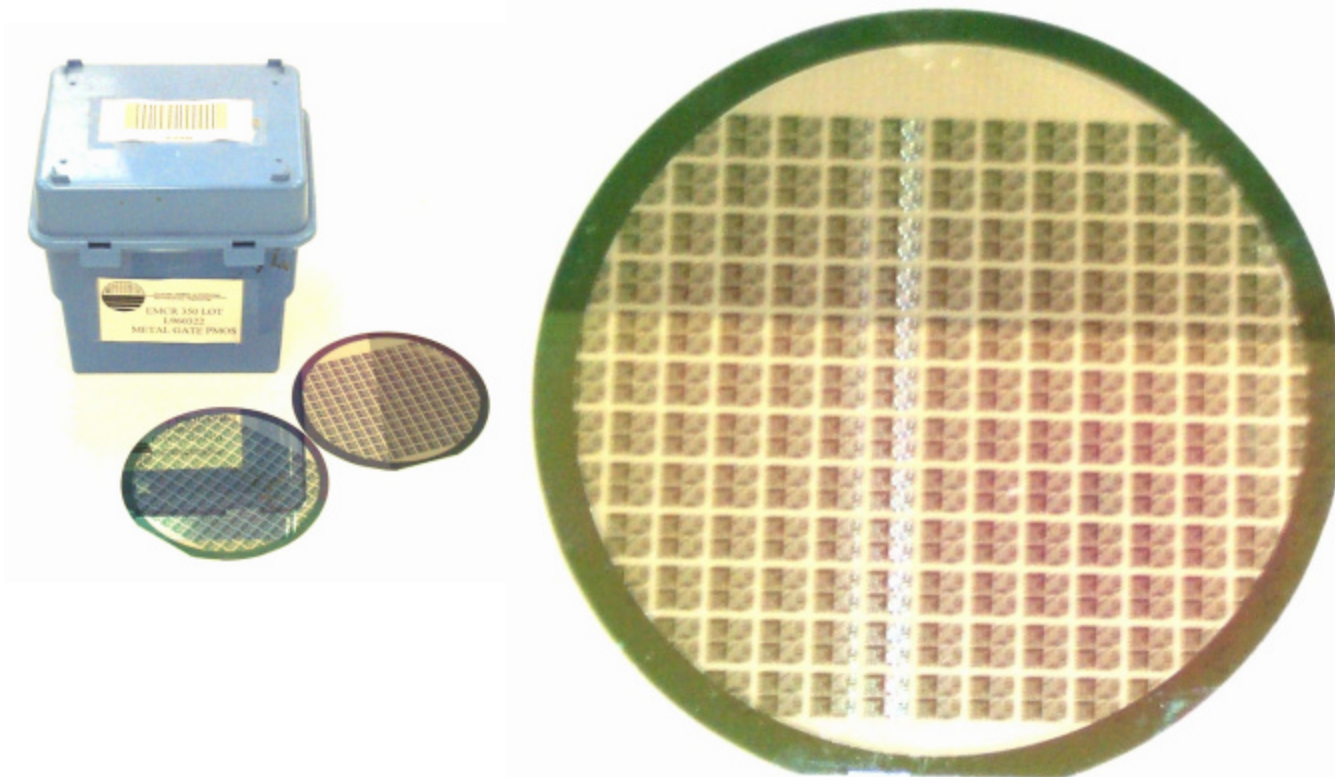
100,000

Made at External Foundry



May 2001

1996 RIT'S FIRST 6" WAFERS



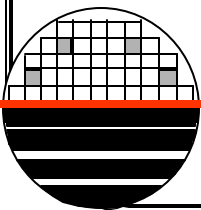
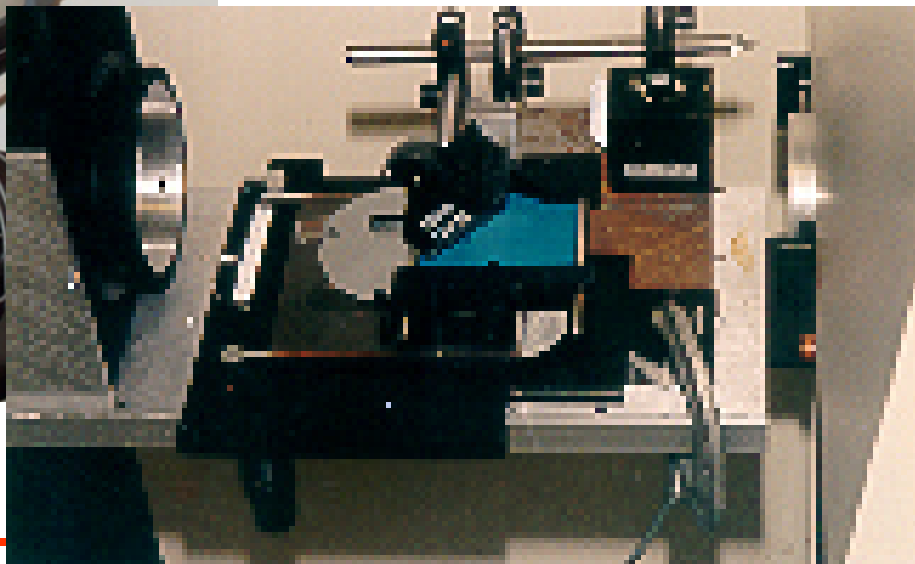
Karl Hirschman and
his EMCR 350 Class

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FIRST EXCIMER LASER LITHOGRAPHY



Laser light plus optics on a bench.



Bruce Smith

*Rochester Institute of Technology
Microelectronic Engineering*

RIT EARLY MEMS DEVICE

U.S. Patent

Oct. 25, 1994

Sheet 6 of 6

5,357,803



United States Patent [19] Patent Number: **5,357,803**
 Lane [45] Date of Patent: **Oct. 25, 1994**

- [54] **MICROMACHINED MICROACCELEROMETER FOR MEASURING ACCELERATION ALONG THREE AXES**
- [75] Inventor: Richard L. Lane, Penfield, N.Y.
- [73] Assignee: Rochester Institute of Technology, Rochester, N.Y.
- [21] Appl. No.: 866,667
- [22] Filed: Apr. 8, 1992
- [51] Int. Cl.³ G01P 15/13
- [52] U.S. Cl. 73/517 B; 361/280
- [58] Field of Search 73/517 B, 517 R, 516 R; 361/280, 283.1; 310/309; 384/439

- References Cited**
- U.S. PATENT DOCUMENTS**
- | | | | |
|-----------|---------|----------------|-----------|
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| 4,706,374 | 11/1987 | Murakami | |
| 4,736,629 | 4/1988 | Cole | |
| 4,893,509 | 1/1990 | MacIver et al. | |
| 4,901,570 | 2/1990 | Chang et al. | |
| 4,922,756 | 5/1990 | Henrion | |
| 4,932,261 | 6/1990 | Henrion | |
| 4,945,765 | 8/1990 | Rosshart | |

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- F. Rudolf, et al., "Silicon Microaccelerometer", *Transducers '87, Rec. of the 4th Int. Conf. on Solid-State Sensors and Actuators*, 1987, pp. 395-398.

Primary Examiner—John E. Chapman
Attorney, Agent, or Firm—Nixon, Hargrave, Devans & Doyle

[57] ABSTRACT

The present invention relates to a microaccelerometer employing a single free-mass and capable of measuring acceleration along three coordinate axes, and a process for fabricating through micromachining and microelectronic techniques a microaccelerometer employing a free-mass. A microaccelerometer preform is constructed by chemically coating and etching a silicon wafer to form a support member and a free-mass surrounded by the member. The free-mass is movable with respect to, but constrained by the silicon support member. Acceleration measurements are obtained by circuits which sense changes in the position of the free-mass with respect to an equilibrium position, induced by a change in the rate of acceleration of the accelerometer, and the electromagnetic force required to restore the free-mass to its equilibrium position.

18 Claims, 6 Drawing Sheets

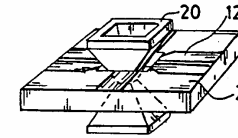


FIG. 15

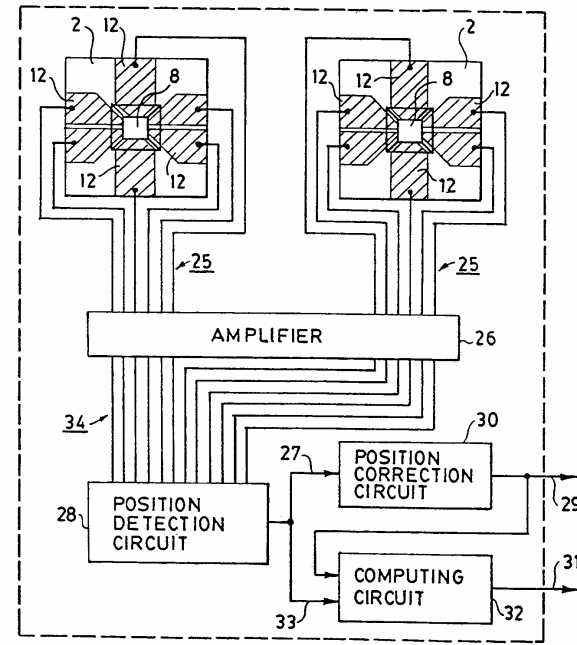
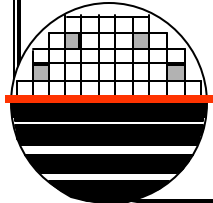
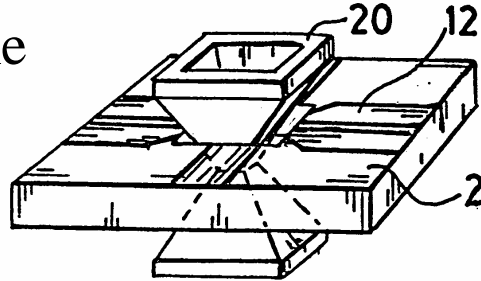
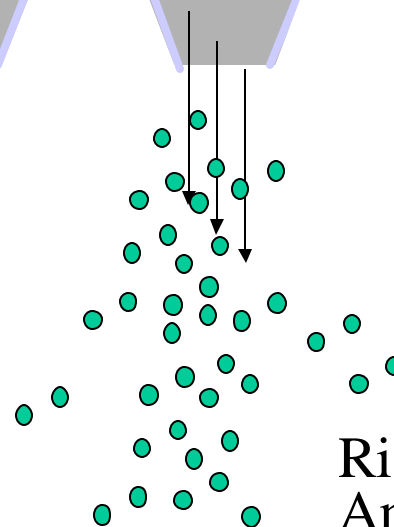
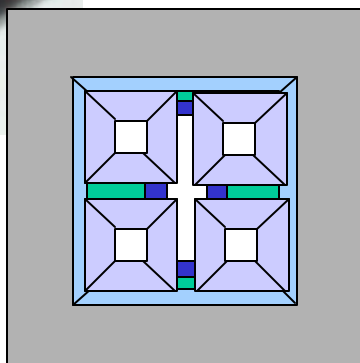
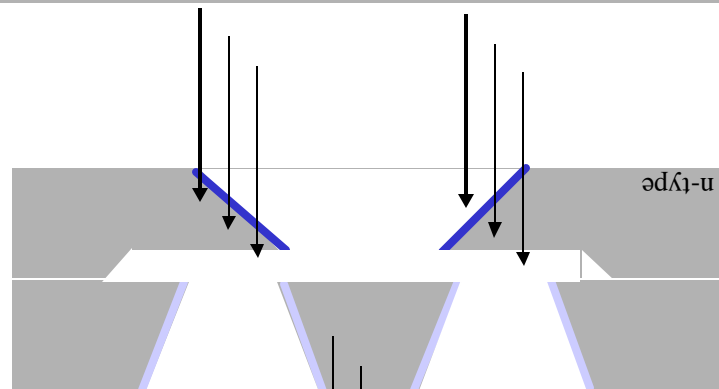


FIG. 16

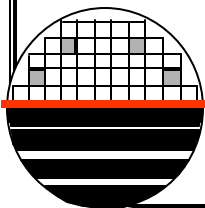
Dick Lane



OTHER RIT MEMS DEVICE

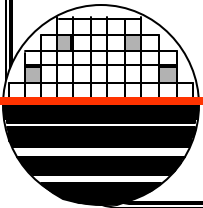


Risa Robinson
An Pham
Lynn Fuller



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RIT'S FIRST RTP TOOL



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RIT'S FIRST CMP TOOLS

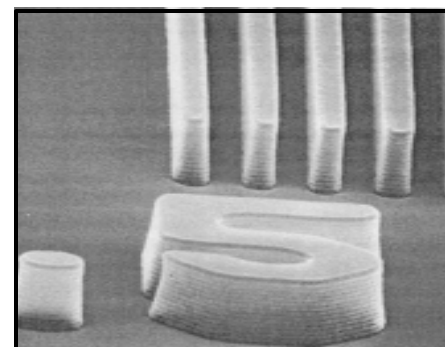


Westech/Speedfam CMP Tool

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RIT'S ADVANCED LITHOGRAPHY TOOLS



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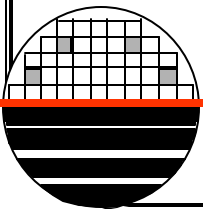
RIT'S ADVANCED ETCH TOOL & CD SEM



Quad Plasma Etch Tool

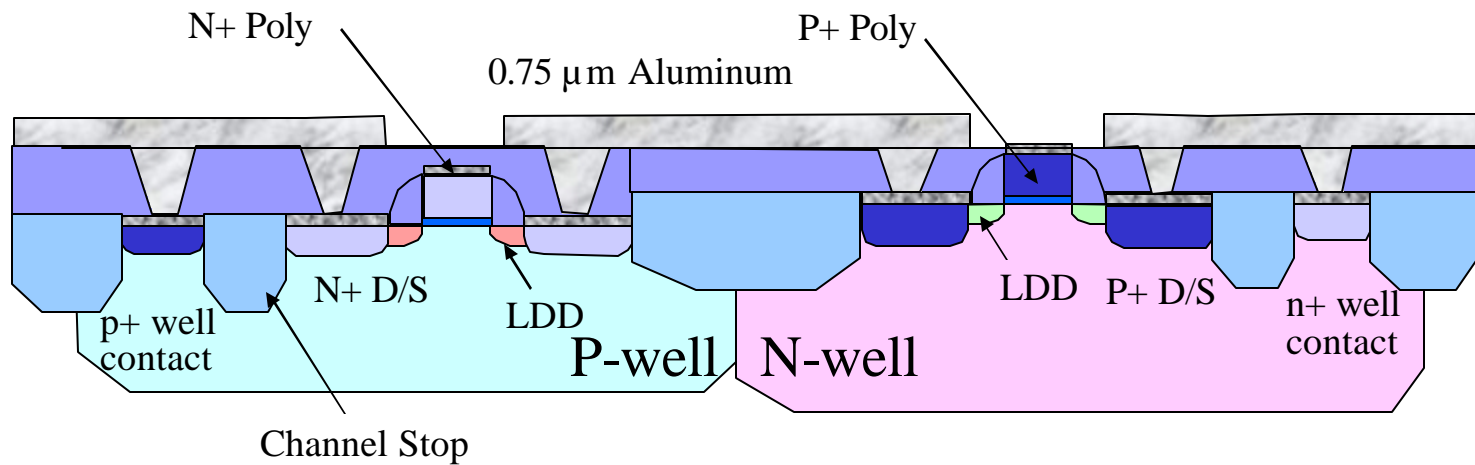


Hitachi 6780 CD SEM



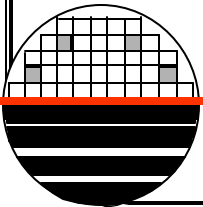
Rochester Institute of Technology
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RIT'S ADVANCED CMOS PROCESSES



0.5 μm Poly Gate Length CMOS

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Microelectronic Engineering

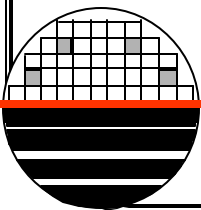


May 2001

RIT'S 1ST, 2ND & 3RD ABET ACCREDITATION



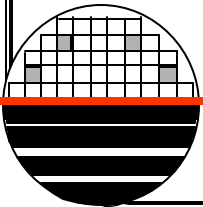
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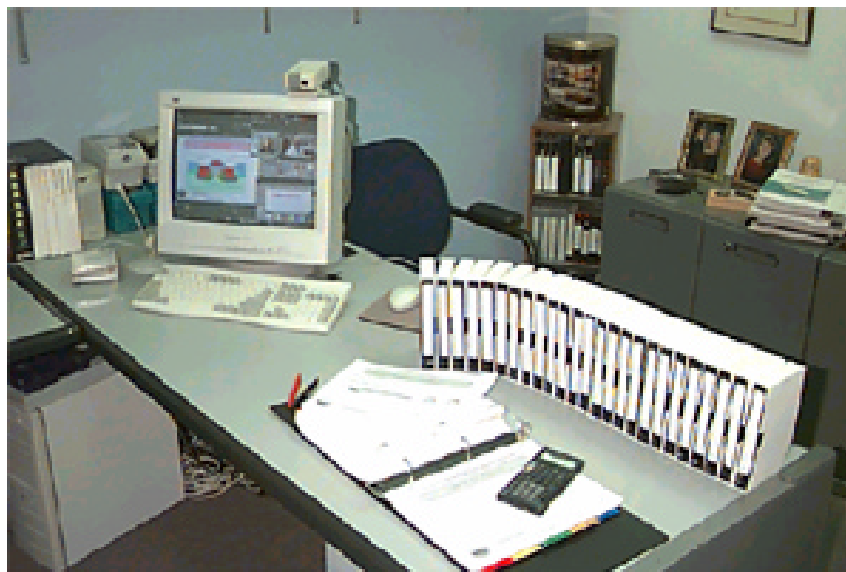
MASTERS DEGREES OFFERED IN μE

Master of Engineering in Microelectronics Manufacturing Engineering
Master of Science in Microelectronics Manufacturing Engineering

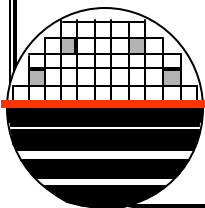


May 2001

MEMME OFFERED BY DISTANCE LEARNING



Video Tapes for Each Module, ~30/course
Paper Copies of Each Module Presentation ~1000 pages/course
Special Simulation Software Server, Textbook, WEB Based
Help



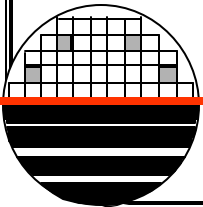
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May 2001

BRUCE SMITH - INVENTOR OF THE YEAR 2000

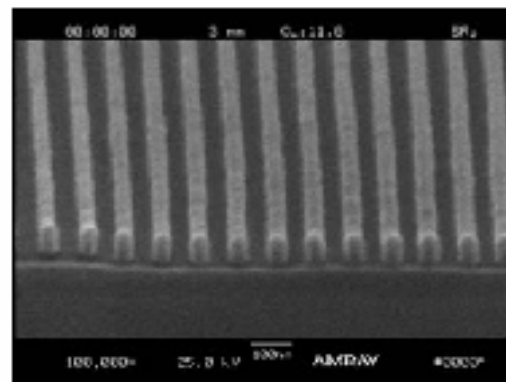


At a first-ever celebration of RIT inventors, professors Bruce Smith, Richard Lane and Joseph Hornak (left to right) stand with President Albert Simone holding patent plaques that bear drawings and descriptions of their inventions.

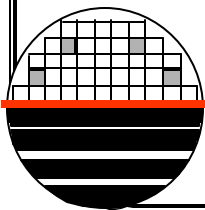


May 2001

DR. BRUCE SMITH – STARTS AMPHIBIAN SYSTEMS INC.



193i resist images 45nm resolution



Rochester Institute of Technology
Microelectronic Engineering

**STEVE CARLSON – MICROE BS GRAD 1987,
IMAGING SCIENCE MS GRAD 1990**

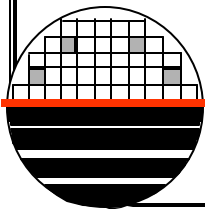
Distinguished RIT alumni receive



Alumni-award winners, left to right, Donald Naylor, Philip Rosenzweig, Steven Carlson, Philip Jacob, David Foy, Donald Lehmebeck and Michael Ramsager (absent: Daniel Carp, Mark Conboy)

*Rochester Institute of Technology
Microelectronic Engineering*

Senior VP Technology, Photronics, Inc.



NEWS AND PUBLICITY

Solid State Technology December 1999

“There is a shortage of engineering graduates, especially those from the pioneering and renowned IC manufacturing program at the Rochester Institute of Technology”, Stanley Wolf, author and professor at UCLA.

INDUSTRY INSIGHTS



Stanley Wolf

Needed: Cohesive education programs for IC manufacturing

At the height of the last boom in the semiconductor industry, we heard an industry-wide cry about the lack of properly educated and trained people entering the industry at all levels. Part of the concern was that US academia was not turning out enough engineers in general and, more specifically, with a few exceptions, was not offering programs with a strong emphasis in IC manufacturing.

Now, we've gone through a classic downturn and are entering what we anticipate is another boom. But it appears that IC manufacturing education at the university level in the US today has not changed appreciably. While engineers and scientists are well educated in specific disciplines, such as electrical engineering, chemistry, physics, materials science, mechanical engineering, and optics, they still enter the industry untrained for IC manufacturing. By-and-large, even at the engineering level, training in IC manufacturing is still occurring on the job. There has been no fundamental change in engineering education to support what is a cornerstone industry in today's society.

My best perspective of this trend comes from reading the shortage of recent, up-to-date semiconductor textbooks.

Only ~2000 textbooks specifically about semiconductor manufacturing are demanded to university bookstores each year and ~15% are returned because they are not purchased. Yearly enrollment in such

Stanley Wolf is the author of the three-part series *Silicon Processing for the VLSI Era* and owner of Lattice Press, PO Box 332, Sunset Beach, CA 90742, tel: 714/340-6010, fax: 662-592-1975, e-mail: stanwolf@home.com.

classes is about 1500. IC fabrication courses are offered at about 100 US universities, with an average enrollment that sells 15-20 books/year at each school. (This number may be skewed to the low side because at some schools, such as Stanford University, professors use their own notes as the course text.) Since 1986, Lattice Press has sold 20,000 copies of the book *Silicon Processing for the*

By-and-large, even at the engineering level, training in IC manufacturing is still occurring on the job, not at the university.

VLSI Era, Vol. 1: Process Technology (co-authored by myself and R. Tauber). A small percentage of these are being used in classes at MIT, UC Berkeley, UCLA, the University of Michigan, UT Austin, etc. But the widest use of this book has been for self-education, OJ training, or an internal program at IC manufacturers. The book's second edition has just been published (October 1999), but this has been long overdue.

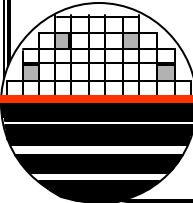
Four of the five top IC manufacturing textbooks, which constitute most of the 2000 mentioned above, have copyright dates circa 1990. This indicates that book publishers do not see a demand to keep these books up-to-date with the rapid pace of IC manufacturing technology. The current edition of See's *VLSI Technology* (McGraw Hill), which originated as notes for an internal training program at Bell Labs, was published in 1988. See, who is now at National Chiao Tung University, Hsinchu, Taiwan, republished his book in 1996 as *VLSI Technology* (McGraw Hill), but this volume eliminated chapters on oxidation, diffusion, and ion implantation, reducing its effectiveness as a textbook.

Other older textbooks include Runyan and Bean's *Semiconductor Integrated Circuit Processing Technology* (Addison-Wesley), published in 1990, and Gandhi's *VLSI Fabrication Principles* (Wiley), which was reissued as a second edition in 1994, although 90% of its references still pre-date 1985. Campbell's *Science and Engineering of Microelectronic Fabrication* (Oxford) was published in 1996 and currently owns ~35% of the textbook market. However, it contains almost no references more recent than 1991 and therefore does not describe the hottest process technologies of the 1990s, such as CMP, copper metallization, dual-damascene interconnects, step-and-scan alignment, and phase-shift masks.

Despite the fact that ~90% of IC manufacturing is CMOS-based, there is no single textbook in print today on CMOS technology. Chen's *CMOS Devices and Technology for VLSI* (Prentice-Hall, 1990) is out of print. This may be because only a very small number of courses are available at universities on the device physics of MOSFETs—offered by excellent professors such as Chennung Hu at UC Berkeley and John Bowers at the University of Arizona.

There is a shortage of engineering graduates, especially those from the pioneering and renowned IC manufacturing program at the Rochester Institute of Technology (RIT). Numbering about 35-351/year (approximately 30 BS, 10 MS, and 5 PhDs), the RIT graduates are only a small fraction of the engineers entering IC manufacturing every year. A few other similar programs have emerged, for example, at Boise State University and the University of Illinois at Chicago, but not enough to meet the need.

continued on page 87



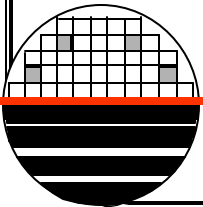
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SRC #1 RANKING

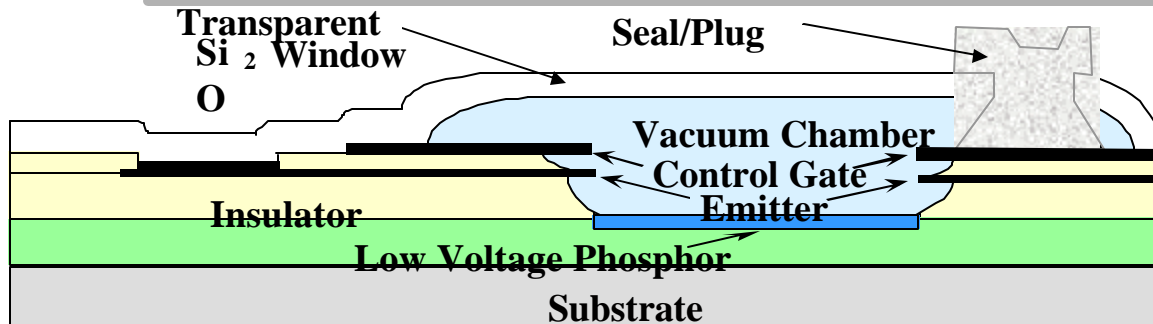
1991 Semiconductor Research Corp. survey results published in Semiconductor International:

RIT is number 1 (tied with University of Illinois) in education of engineers for the semiconductor industry.

Ranked below RIT: Texas A&M, MIT, Purdue, UC Berkeley, RPI, Arizona State, Cornell, Murray State, Rice, Stanford, UT Austin

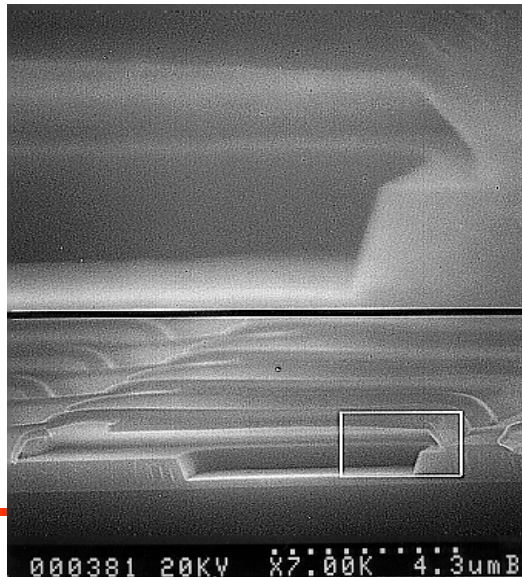


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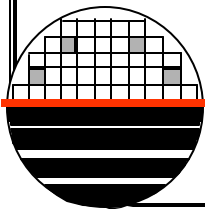
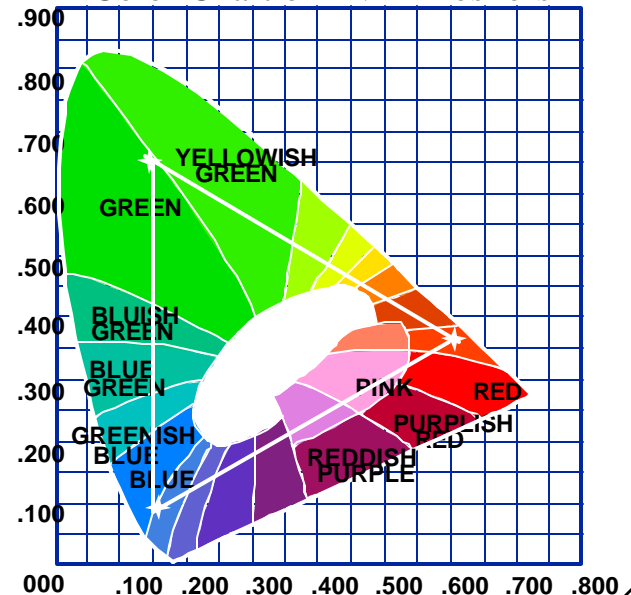


Integrated Phosphor
Field Emission
Device

Micro-encapsulated Chamber



Color Chart of AVT Phoshors



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Lynn Fuller

Bob Daly

Joe Altman

Cem Karacal

David Sumberg

Nassar Darweesh

Karl Hirschman

Bruce Smith

Mike Jackson

Renan Turkman

Philip Rack

Bill Grande

Santosh Kurinec

Dale Ewbank

An Pham

Richard Lane

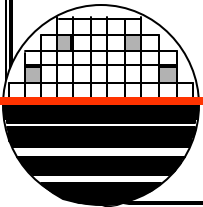
Jim Scanlon

Suraj Bhaskaran

Pamela Obiomon



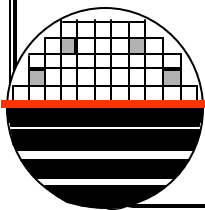
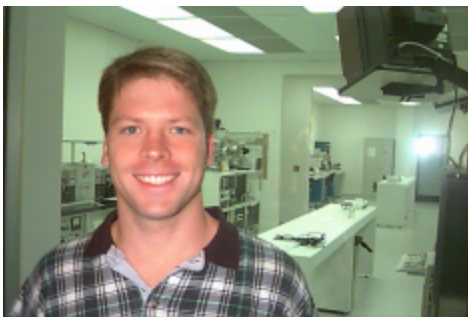
Rob Pearson



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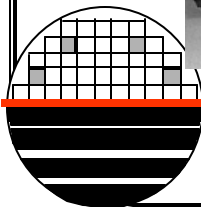
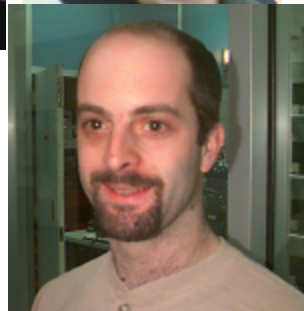
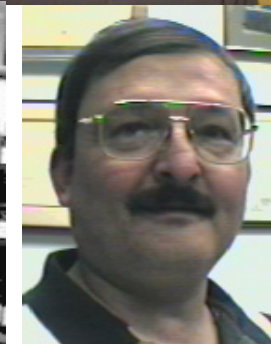
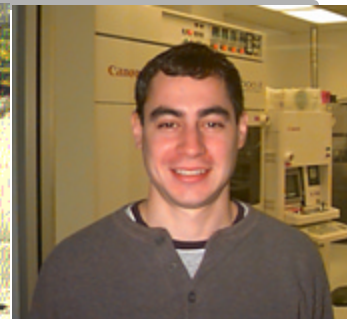
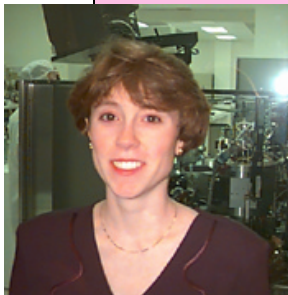
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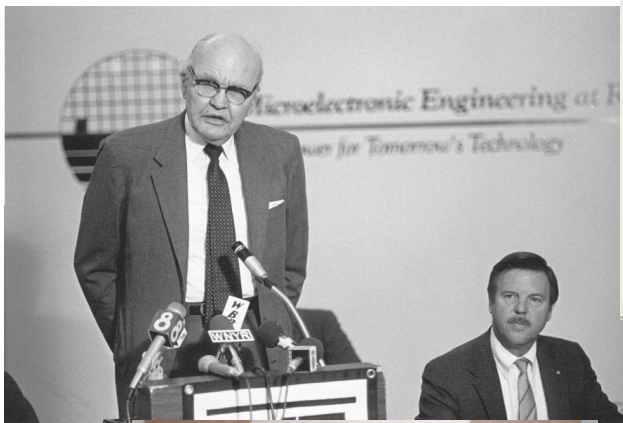
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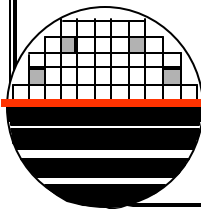
VISITORS and GUESTS



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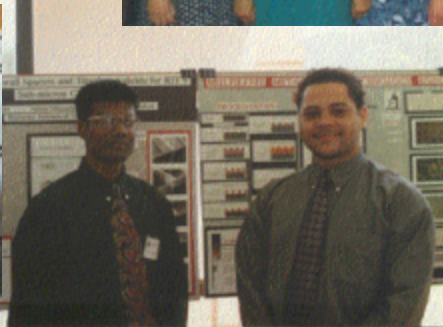
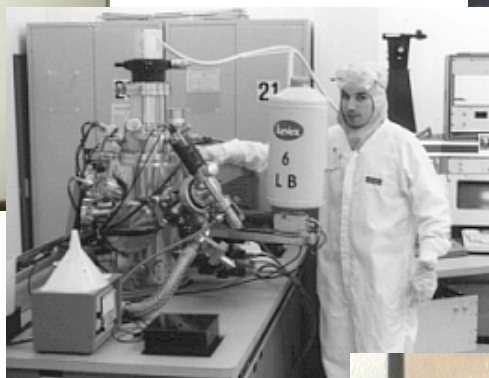
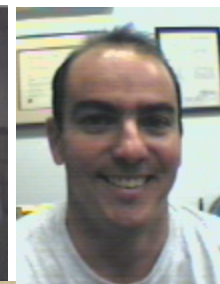
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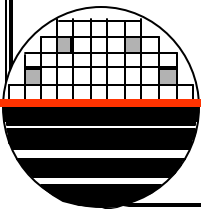


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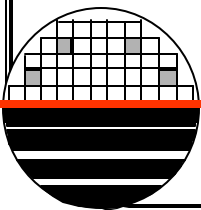
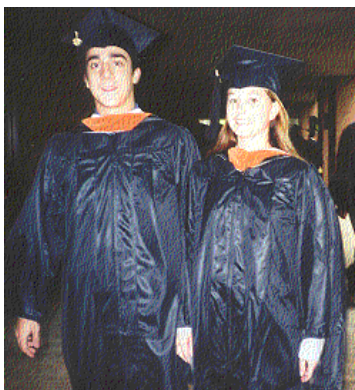


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