ROCHESTER INSTITUTE OF TECHNOLOGY MICROELECTRONIC ENGINEERING

BJT Amplifiers

Dr. Lynn Fuller

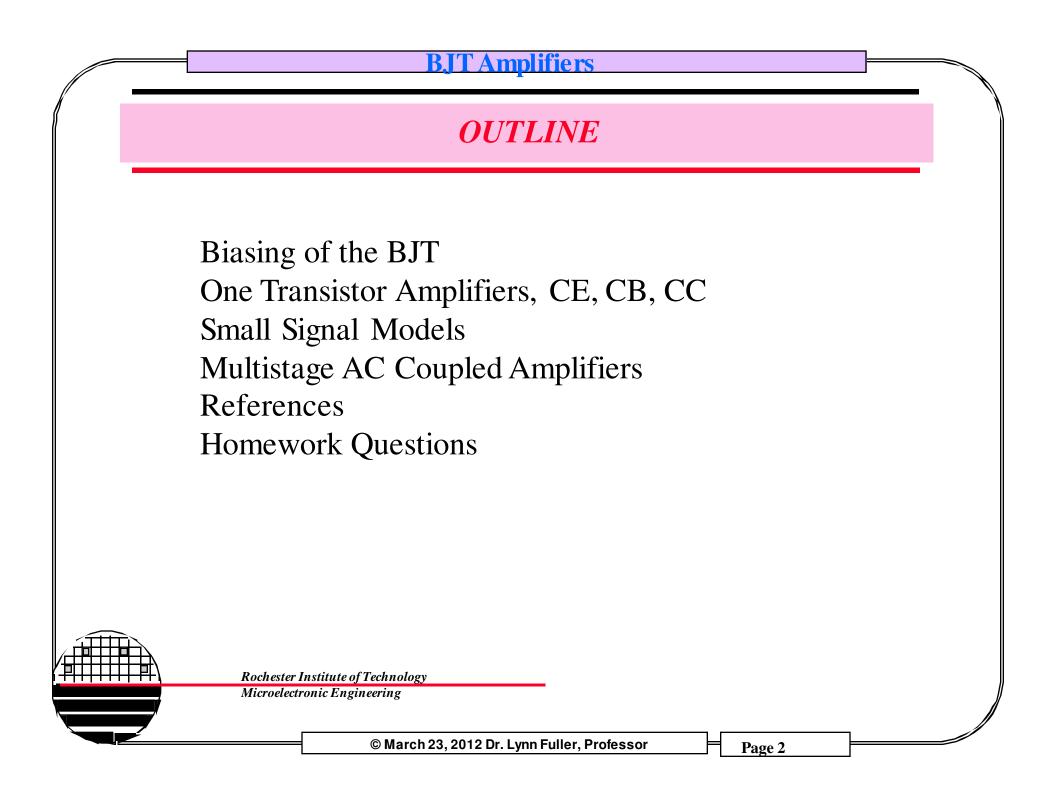
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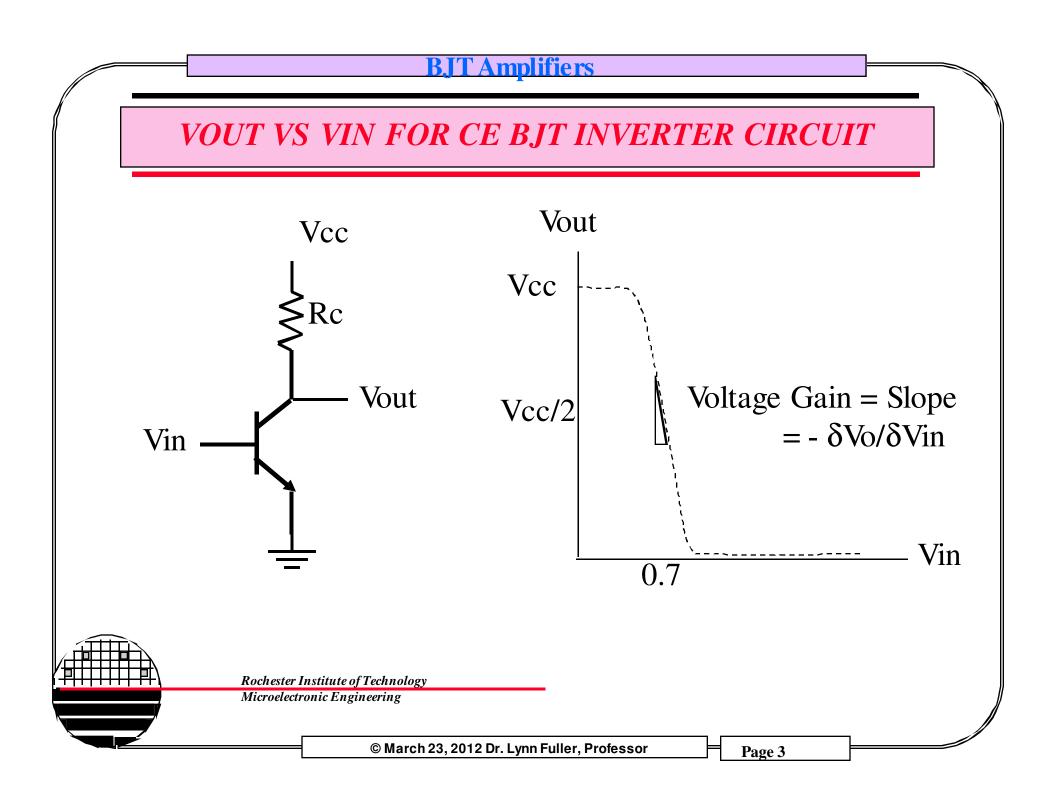
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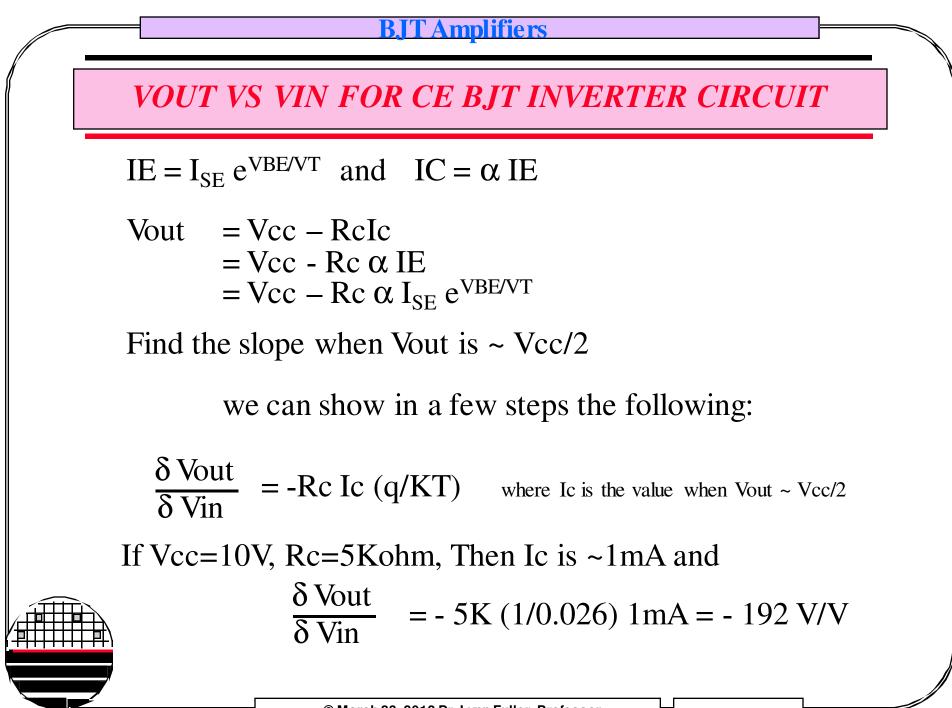


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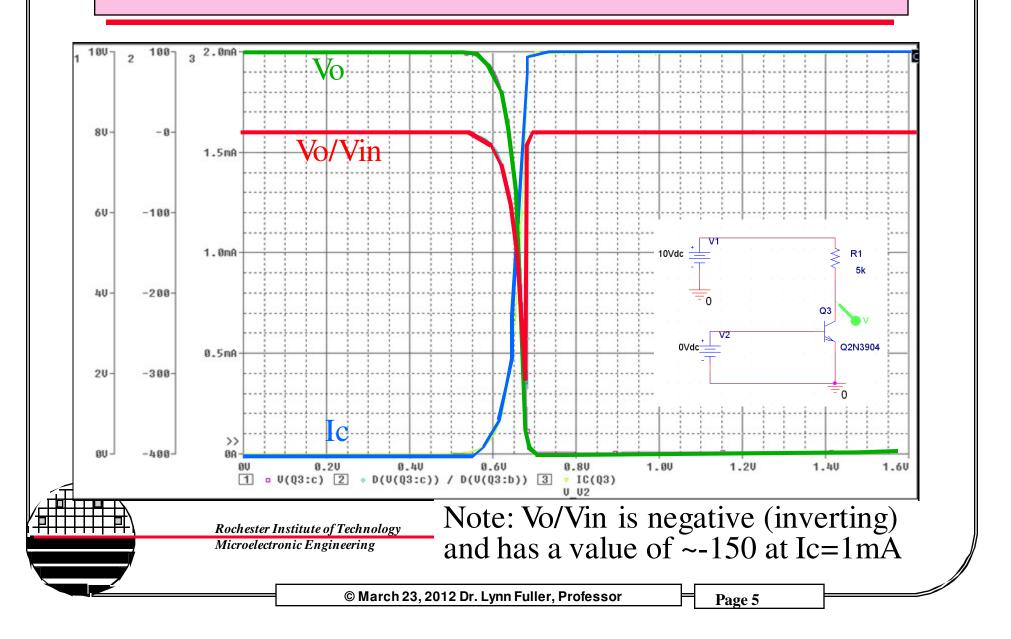
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SPICE ANALYSIS OF BJT INVERTER



SPICE OUTPUT FILE

** Profile: "SCHEMATIC1-BJT_Inverter" [C:\Documents and Settings\Iffeee\Desktop\SPICE\Project_3_BJT_Inverter\bjt_inverter-SCHEMATI **** CIRCUIT DESCRIPTION ** Creating circuit file "bit inverter-SCHEMATIC1-BJT Inverter.sim.cir" *Libraries: Note: see last page of this document for more .lib "C:\Program Files\OrcadLite\Capture\Library\PSpice\eval.lib" *Analysis directives: information on BJT SPICE parameters .DC LIN V V2 0 1.5.0001 .INC "bjt inverter-SCHEMATIC1.net" **** INCLUDING bjt inverter-SCHEMATIC1.net **** **** BJT MODEL PARAMETERS * source BJT INVERTER N00033 N00036 5k R R1 O2N3904 VV1N00036 0 10Vdc ŇPN VV2N00030 0 0Vdc IS 6.734000E-15 Q 03 N00033 N00030 0 Q2N3904 BF 416.4 **** RESUMING bit inverter-SCHEMATIC1-BJT Inverter.sim.cir **** NF 1 .INC "bit inverter-SCHEMATIC1.als" VAF 74.03 **** INCLUDING bit inverter-SCHEMATIC1.als **** IKF .06678 .ALIASES ISE 6.734000E-15 R1(1=N00033 2=N00036) R R1 NE 1.259 V1(+=N00036 -=0)V V1 BR .7371 VV2V2(+=N00030 -=0)NR 1 O3(c=N00033 b=N00030 e=0)0.03 RB 10 .ENDALIASES RC 1 **** RESUMING bjt inverter-SCHEMATIC1-BJT Inverter.sim.cir **** CJE 4.493000E-12 .END MJE .2593 CJC 3.638000E-12 MJC .3085 TF 301.20000E-12 XTF 2 VTF 4 ITF .4 TR 239.50000E-09 XTB 1.5 **Rochester Institute of Technology** CN 2.42 .87 D Microelectronic Engineering © March 23, 2012 Dr. Lynn Fuller, Professor Page 6

2N3904 DATA SHEET



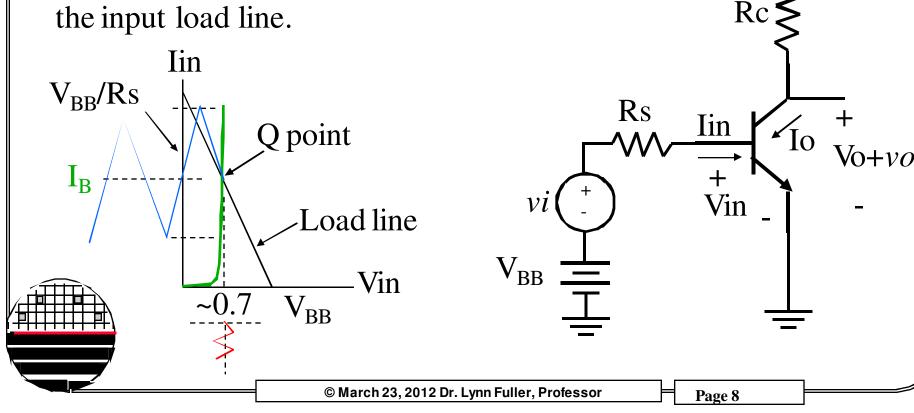
			2N3904 / MMBT3904 / PZT3904	NPN General Purpose Amplifi (continue						
			14 /	Electr	Electrical Characteristics T _A -25°C unless otherwise noted					
			ĭ Z	Symbol	Parameter	Test Conditions	Min	Max	Units	
I	PZT3	904	1BT3	OFF CHAI	RACTERISTICS					
			00	V _{(BR)CEO}	Collector-Emitter Breakdown Voltage	I _C = 1.0 mA, I _B = 0	40	i i	V	
	c .		4	V(BRICBO	Collector-Base Breakdown Voltage	I _c = 10 μA, I _E = 0	60		v	
	6			V(BR)EBO	Emitter-Base Breakdown Voltage	I _E = 10 μA, I _C = 0	6.0		V	
			Ň	IBL	Base Cutoff Current	V _{CE} = 30 V, V _{EB} = 3V		50	nA	
			3	ICEX	Collector Cutoff Current	Vce = 30 V, Vee = 3V		50	nA	
5	SOT-223	в	3904	ON CHAR	ACTERISTICS*	1		<u>.</u>	•	
				h _{FE}	DC Current Gain	$\begin{array}{l} I_{o}=0.1 \text{ mA}, \ V_{OE}=1.0 \ V \\ I_{o}=1.0 \ \text{mA}, \ V_{OE}=1.0 \ V \\ I_{o}=10 \ \text{mA}, \ V_{OE}=1.0 \ V \\ I_{o}=50 \ \text{mA}, \ V_{OE}=1.0 \ V \\ I_{o}=100 \ \text{mA}, \ V_{OE}=1.0 \ V \end{array}$	40 70 100 60 30	300		
				$V_{\text{CE(sat)}}$	Collector-Emitter Saturation Voltage	I _c = 10 mA, I _B = 1.0 mA		0.2	V	
				V	Reso Emitter Seturation Voltage	I _c = 50 mA, I _B = 5.0 mA	0.65	0.3	V	
				V _{BE(sat)}	Base-Emitter Saturation Voltage	l _c = 10 mA, l _B = 1.0 mA l _c = 50 mA, l _B = 5.0 mA	0.65	0.85	v	
	alue 40	Units V		f⊤	GNAL CHARACTERISTICS Current Gain - Bandwidth Product	Ic = 10 mA, Vct = 20 V, f = 100 MHz	300		MHz	
	60	V		Cobo	Output Capacitance	V _{CB} = 5.0 V, I _E = 0, f = 1.0 MHz		4.0	pF	
	6.0 200	V mA		Cibo	Input Capacitance	V _{EB} = 0.5 V, I _C = 0, f = 1.0 MHz		8.0	pF	
	to +150	°C		NF	Noise Figure	I _c = 100 μA, V _{cE} = 5.0 V, R _B =1.0kΩ,f=10 Hz to 15.7kHz		5.0	dB	
ipaired.				SWITCHIN	NG CHARACTERISTICS			•	•	
uty cycle operat	lons.			ta ta	Delay Time	V _{cc} = 3.0 V, V _{BE} = 0.5 V,		35	ns	
				t	Rise Time	I _c = 10 mA, I _{B1} = 1.0 mA		35	ns	
				ts	Storage Time	V _{cc} = 3.0 V, I _c = 10mA		200	ns	
				t,	Fall Time	I _{B1} = I _{B2} = 1.0 mA		50	ns	
Max *MMBT39 350	1,0	Units 13904 100 mW		*Puise Test: I	L Pulse Wildh ≤ 300 μs, Duty Cycle ≤ 2.0%					
2.8	8	.0 mW/°C °C/W		Spice	Model					
357	1:	25 °C/W		NPN (Is=	6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=4	16.4 Ne=1.259 Ise=6.734 lkf=66 i	78m Xtb=1	.5 Br=.737	1 Nc=2	
:m².	-		•	Isc=0 Ikr	=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=. =4 Xtf=2 Rb=10)					
	N	lote: see la	ist pag	ge of the	is document for mo	re information or	I BJT	SPIC	CE pa	
	la (D 0010 0		- Eullor	Professor	Page 7				

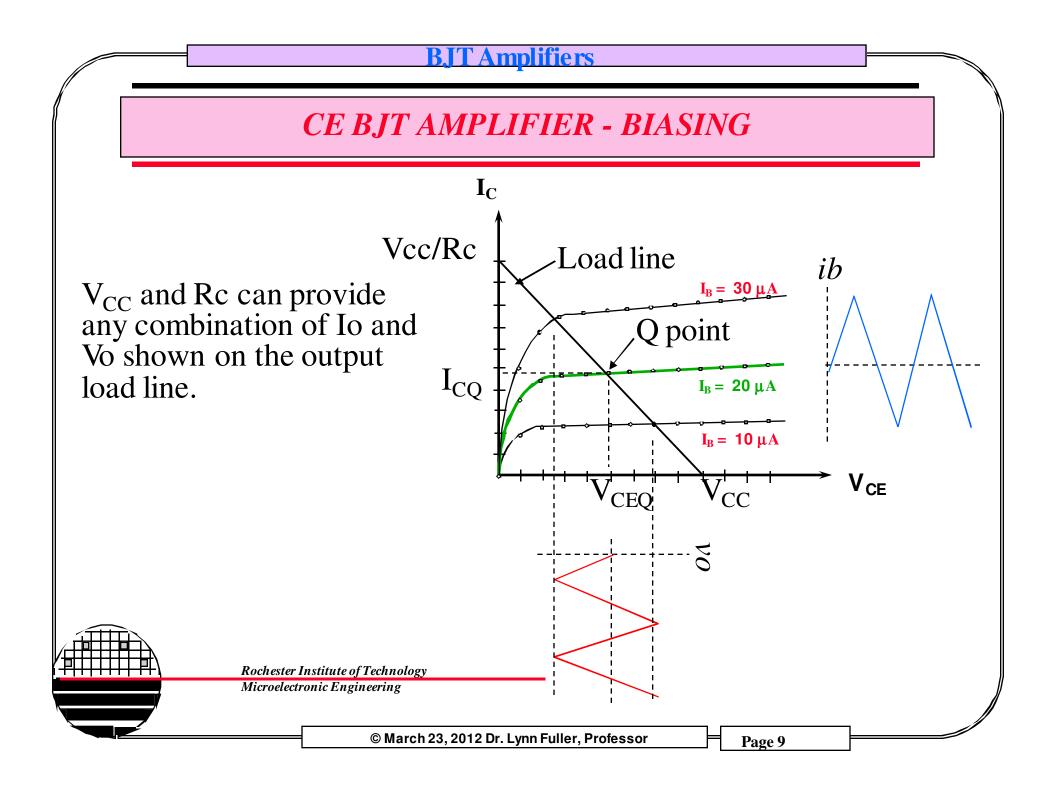
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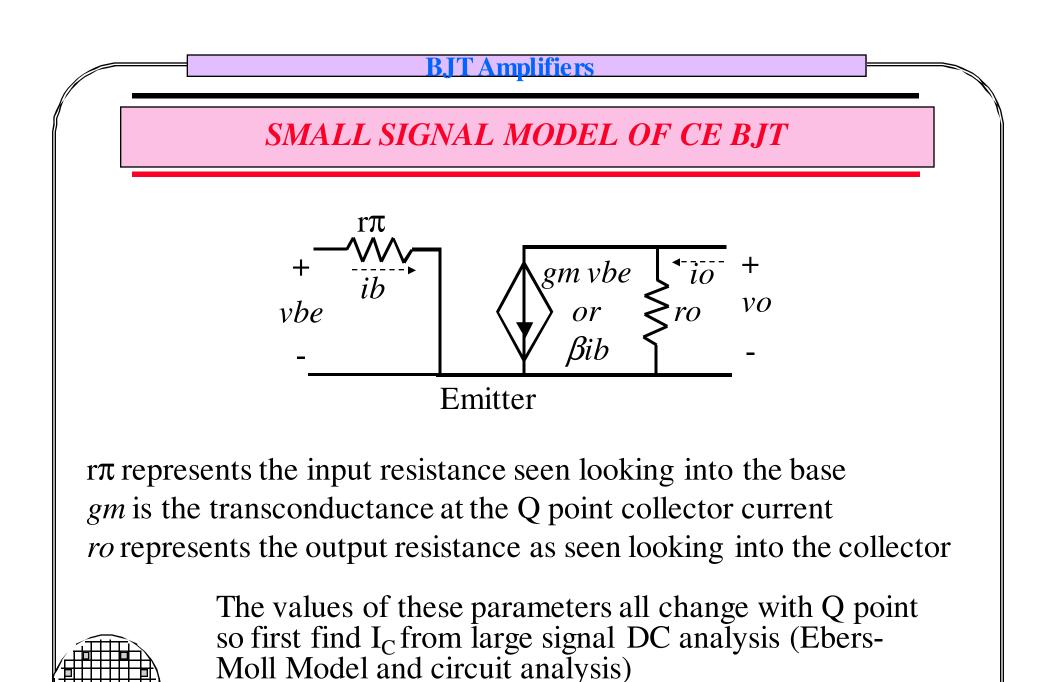
CE BJT AMPLIFIER - BIASING

We want to forward bias the BE junction and reverse bias the BC junction and then add a small changing voltage to the input and realize a larger changing voltage at the output.

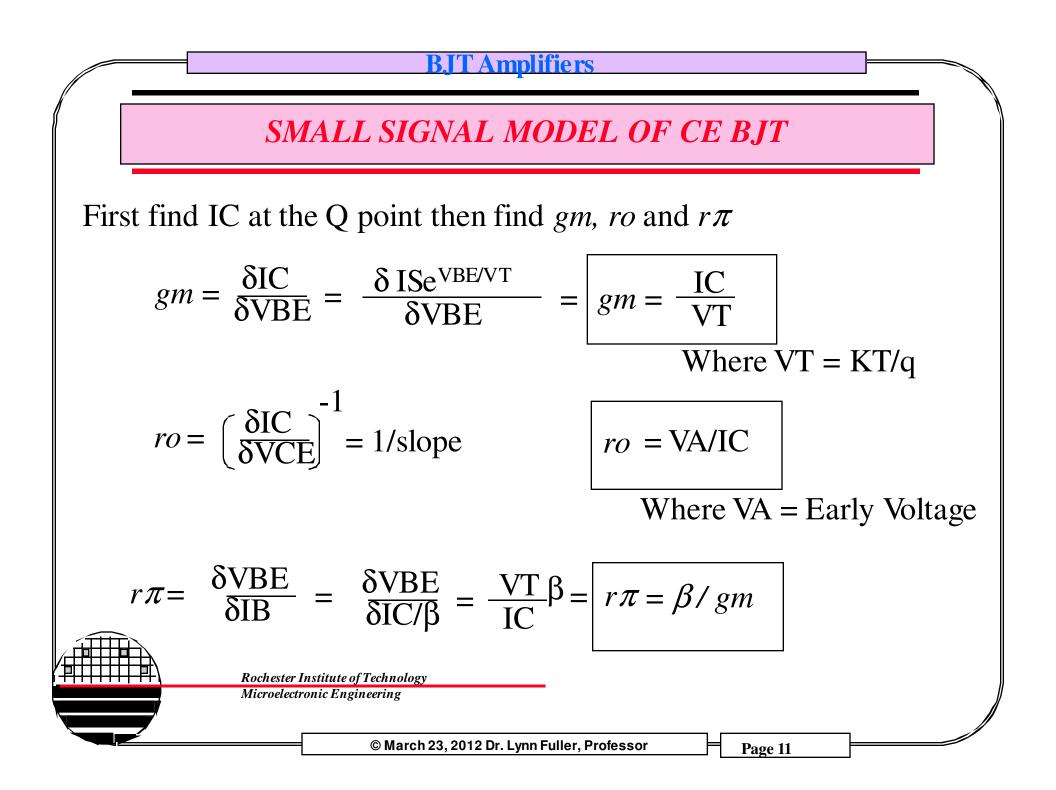
 V_{BB} and Rs can provide any combination of Iin and Vin shown on the input load line.





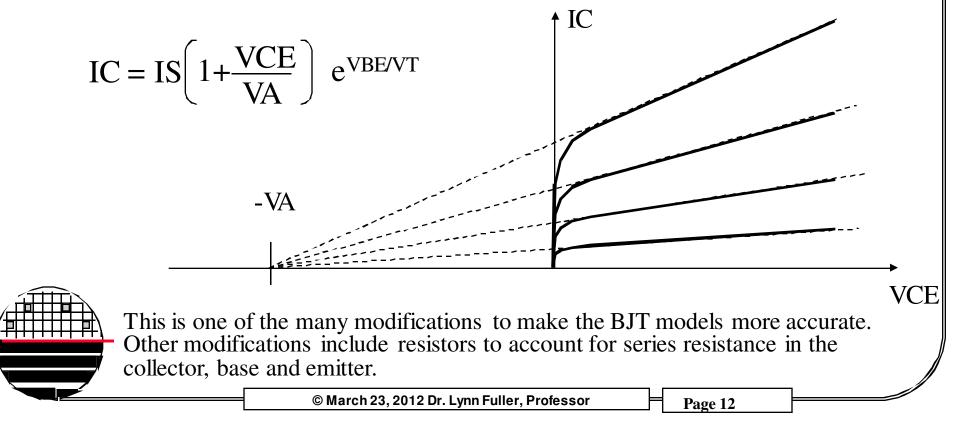


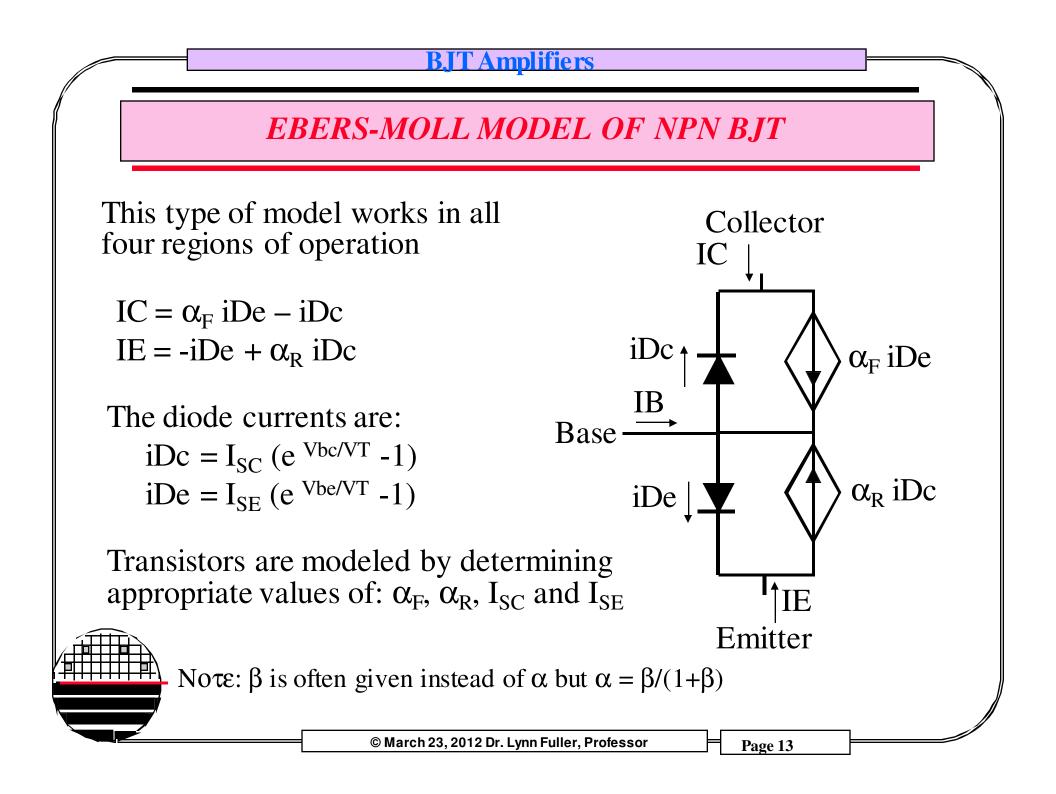
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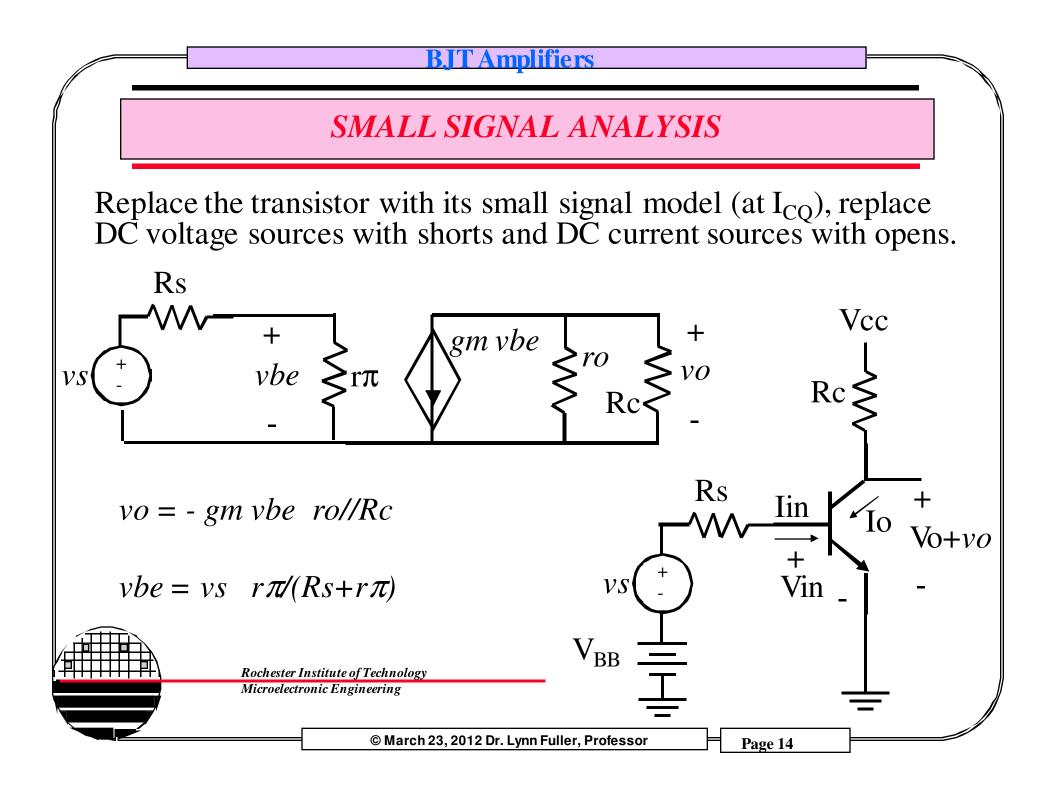


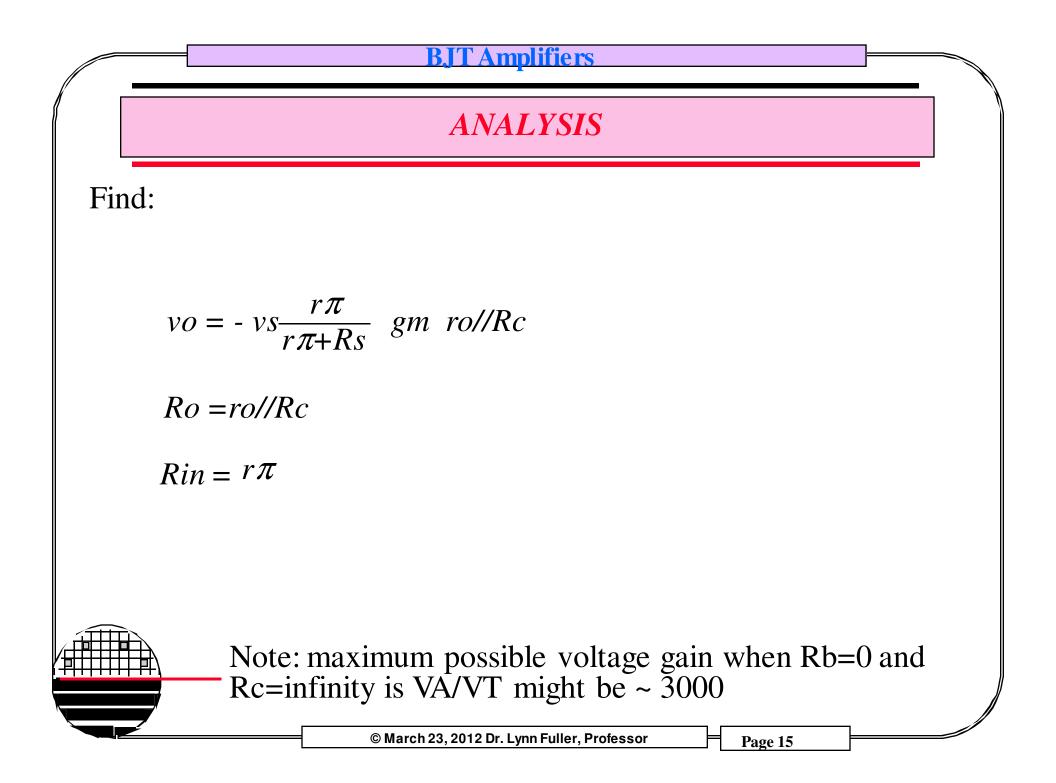
EARLY VOLTAGE

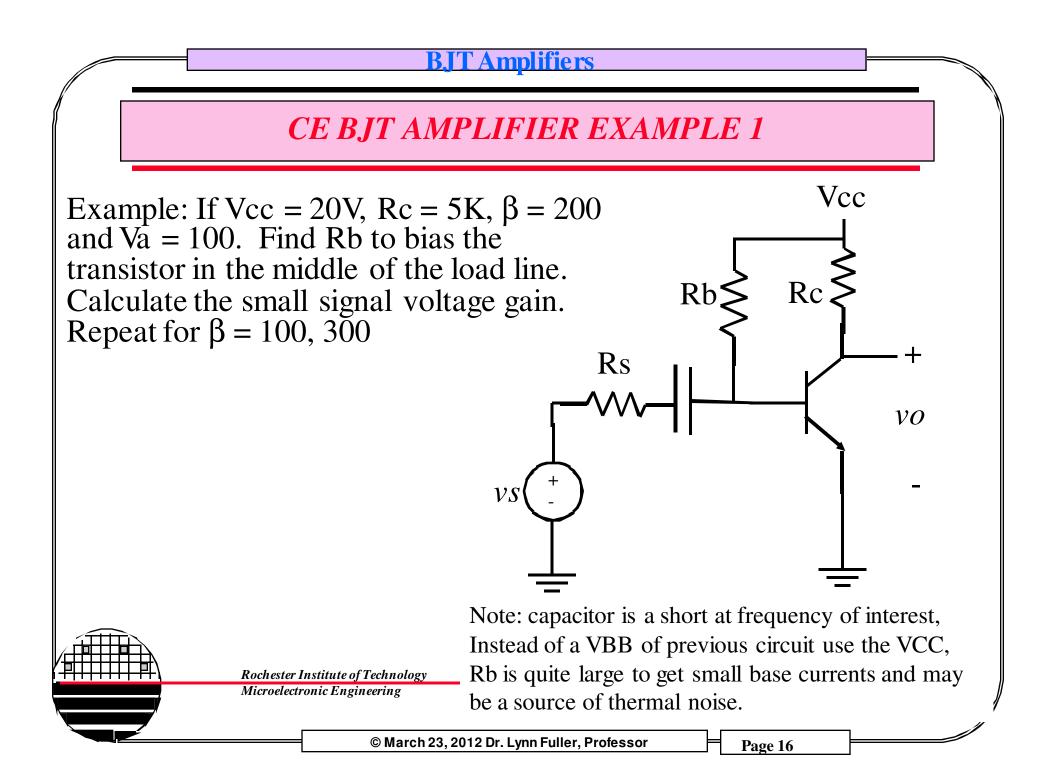
Increasing VCE increases the reverse bias on the BC junction increasing the width of the space charge layer resulting in a decrease in the base with an increase in concentration gradient and an increase in collector current. To account for this the equation relating the collector current to the VBE can be modified slightly as shown:

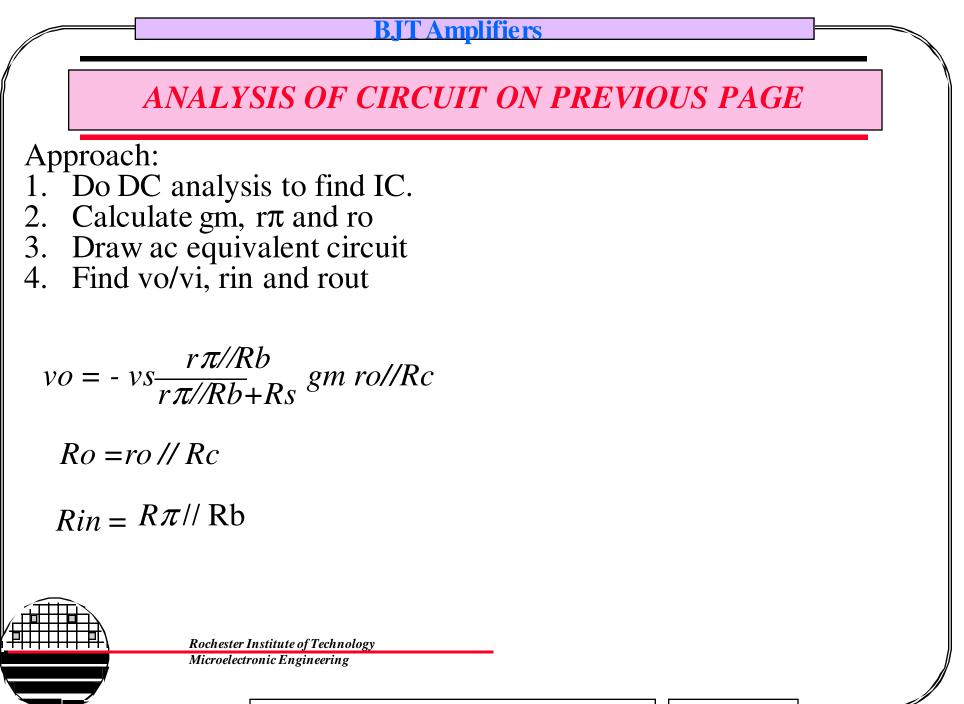




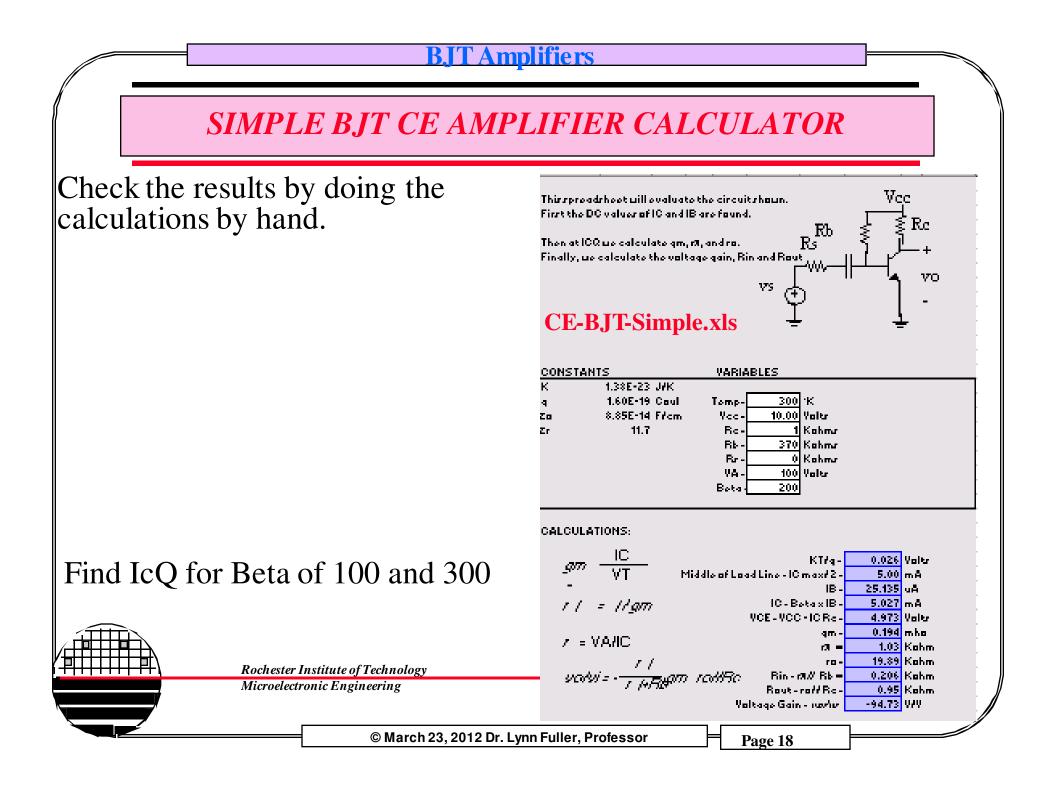


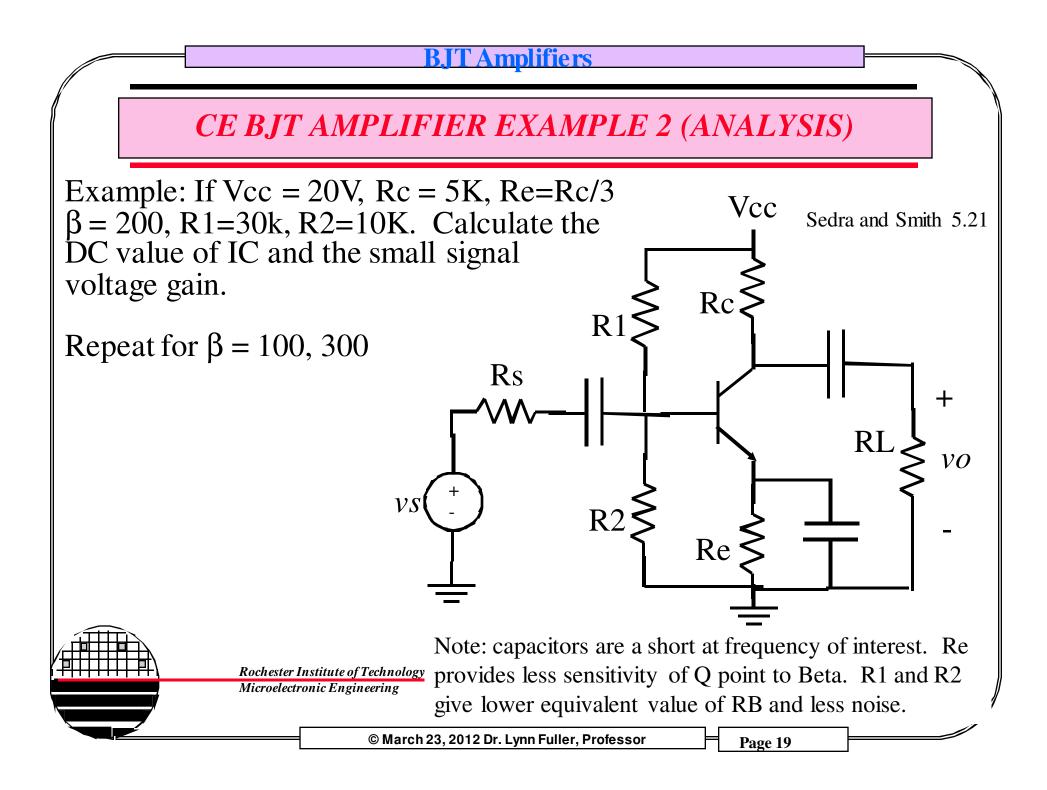






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ANALYSIS OF CIRCUIT ON PREVIOUS PAGE

Approach:

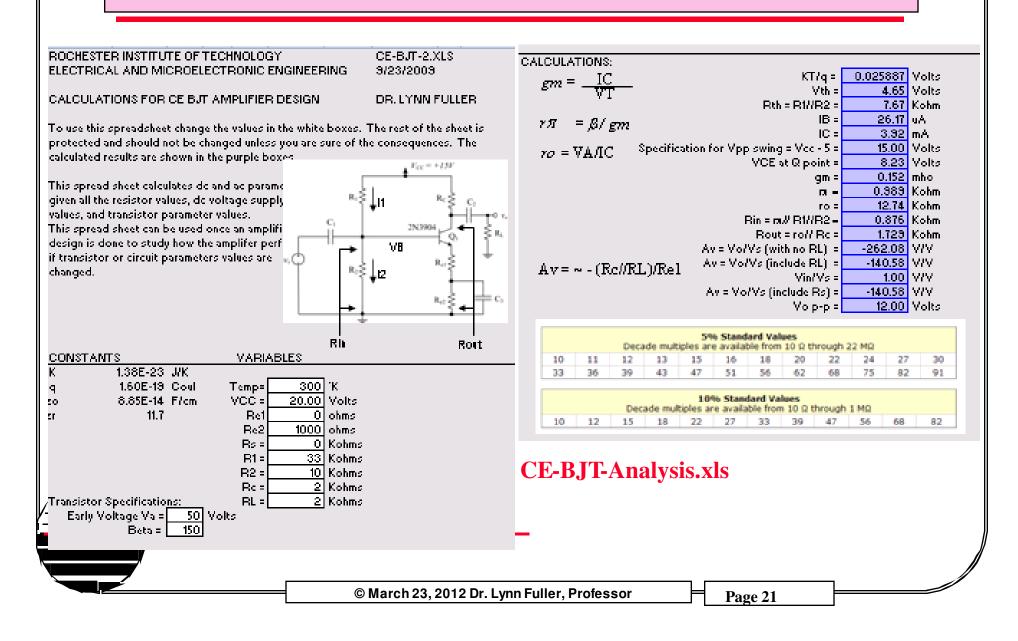
- 1. Find Thevenin equivalent of R1, R2 and VCC.
- 2. Do KVL around the BE loop to find IB.
- 3. Find IC = Beta IB
- 4. Calculate gm, $r\pi$ and ro.
- 5. Draw the ac equivalent circuit.
- 6. Find the voltage gain vo/vi, rin and rout

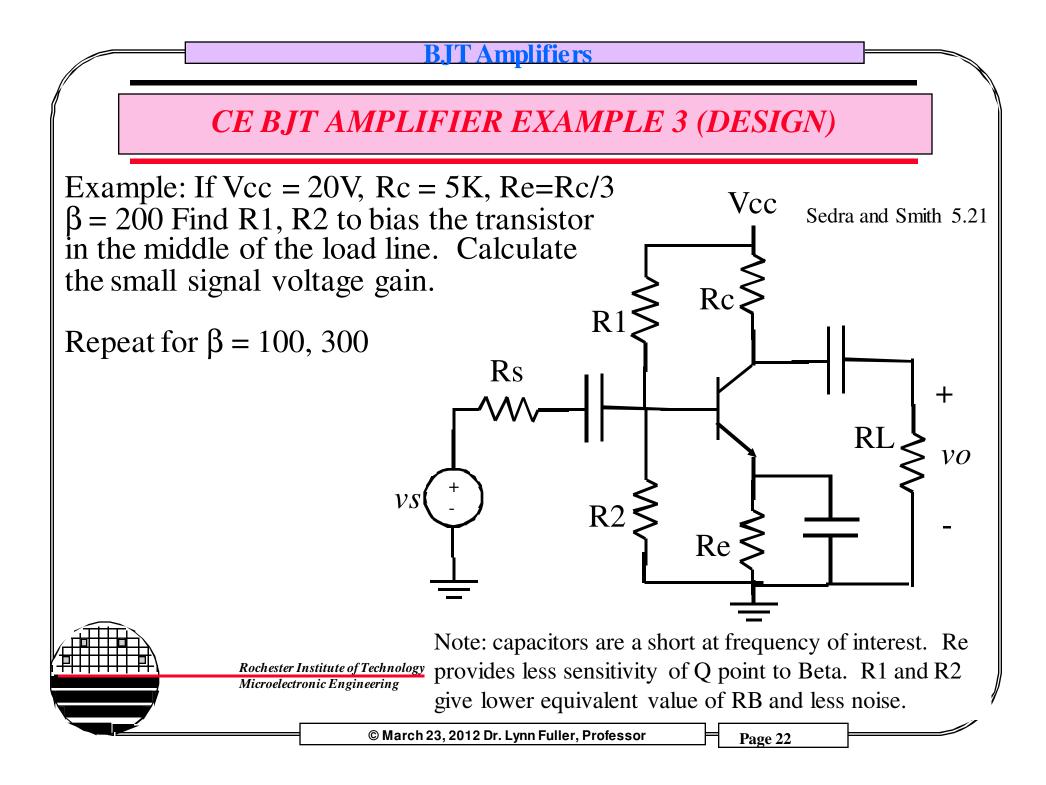
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SPREAD SHEET ANALYSIS PREVIOUS CIRCUIT

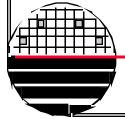




DESIGN CALCULATIONS FOR CIRCUIT ON THE PREVIOUS PAGE

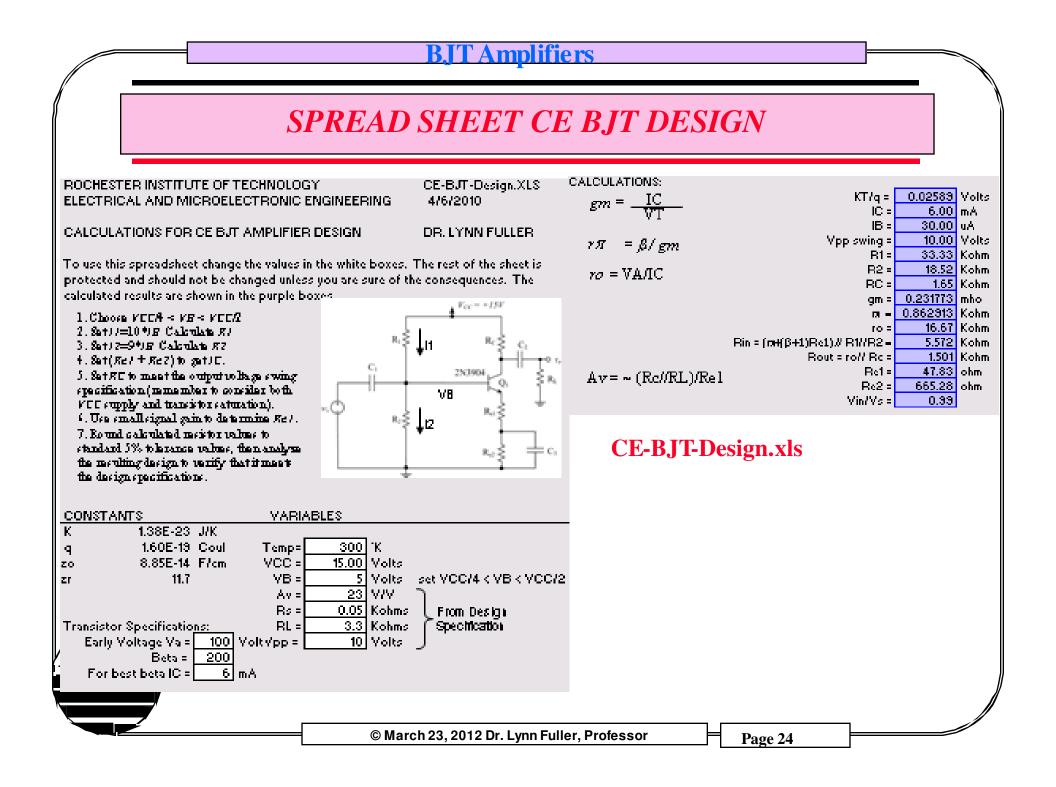
Approach:

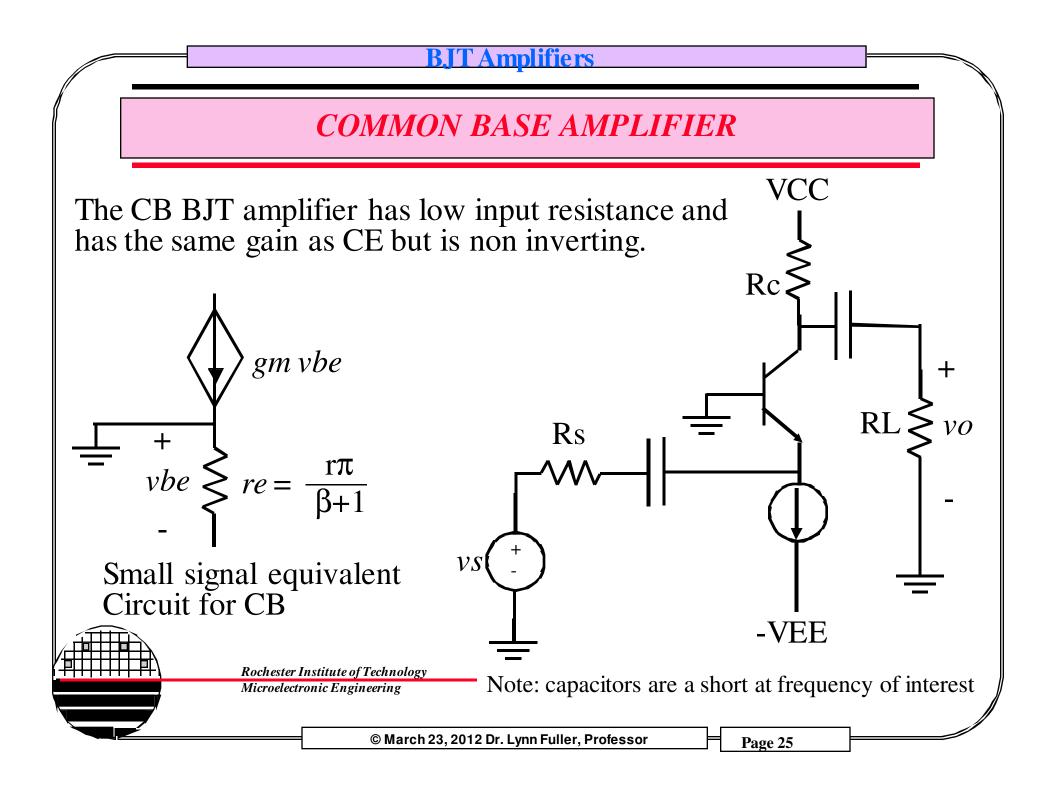
- 1. Pick supply voltage, VCC.
- 2. Pick IC where transistor has good Beta, etc.
- 3. Choose VB between VCC/4 and VCC/2 say VCC/3
- 4. Set I1 = 10 IB find R1
- 5. Set I2 = 9 IB find R2
- 6. Calculate RE to get IC
- 7. Calculate RC to place VCE near middle of DC load line.
- 8. Calculate gm, $r\pi$, ro
- 9. Draw ac equivalent circuit, include selection of RL and RS
- 10. Calculate vo/vi, rin and rout

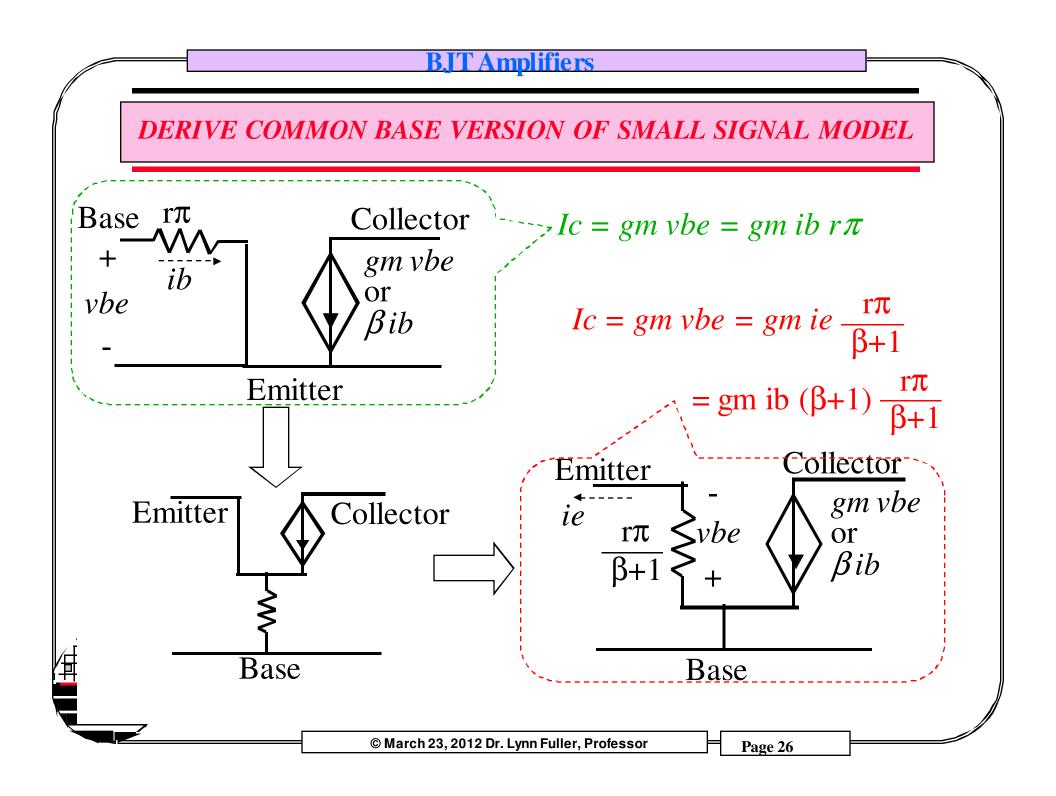


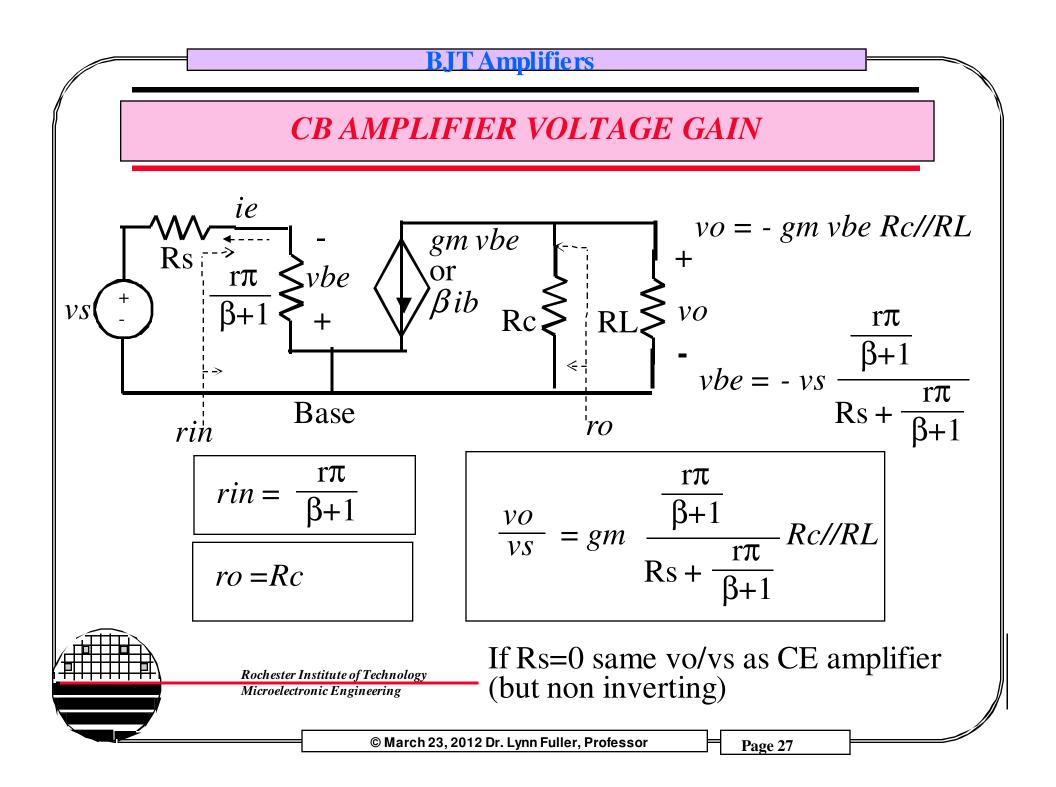
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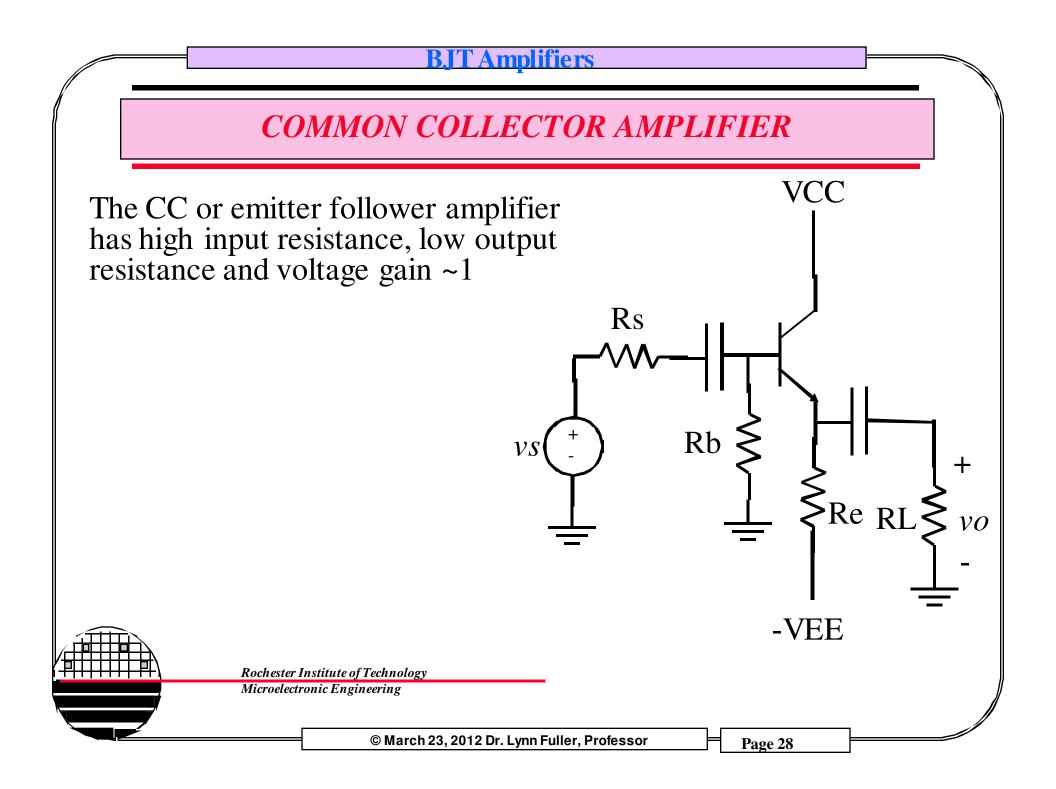
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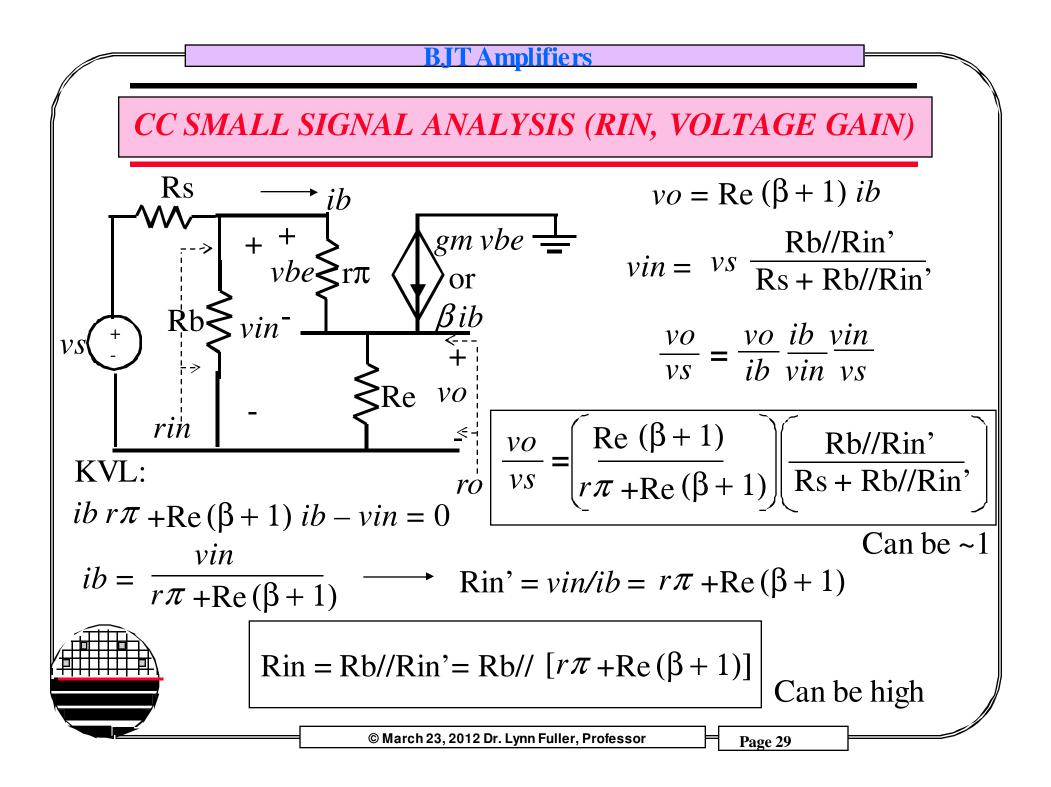




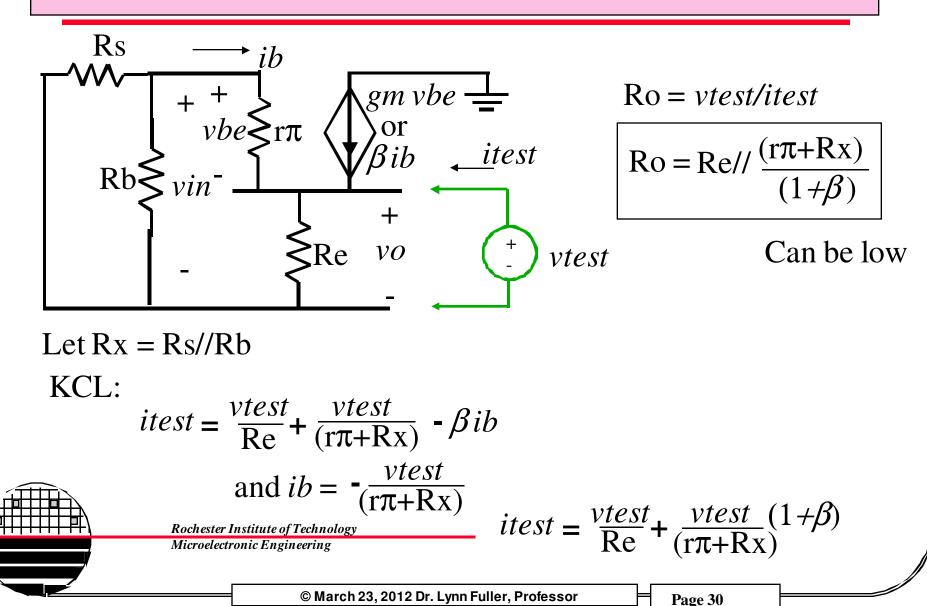


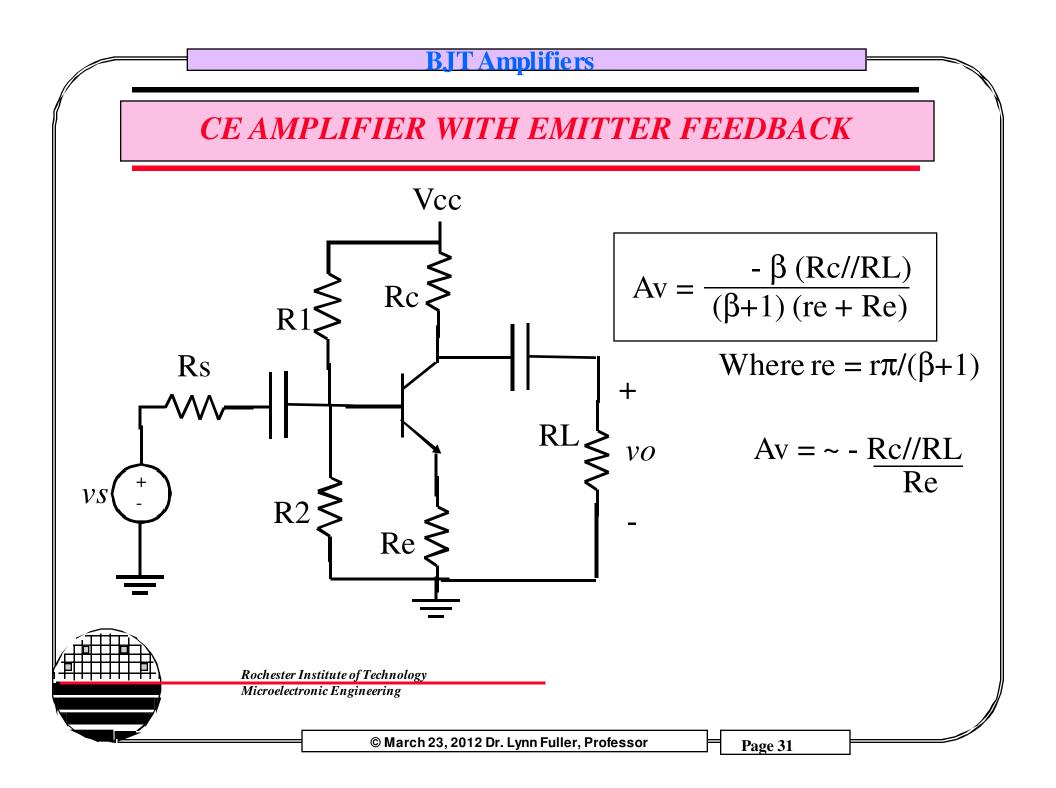






CC SMALL SIGNAL ANALYSIS (OUTPUT RESISTANCE)



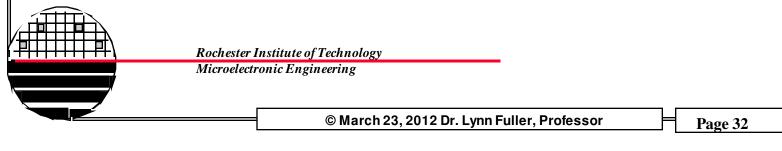


SUMMARY FOR SINGLE TRANSISTOR AMPLIFIERS

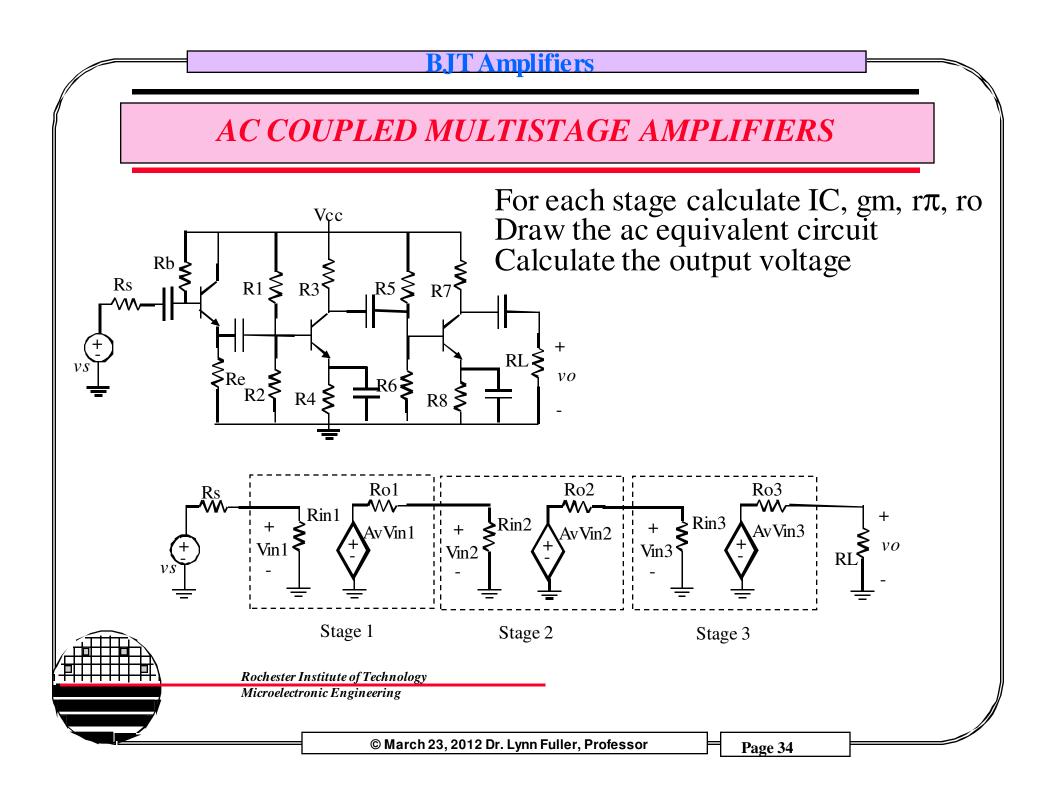
	СЕ	СВ	CC	CE plus Re
Rin	Medium	Low	Highest	High
Ro	Rc	Rc	Low	Rc
Av= vo/vin	High	High	<1	~Rc/Re

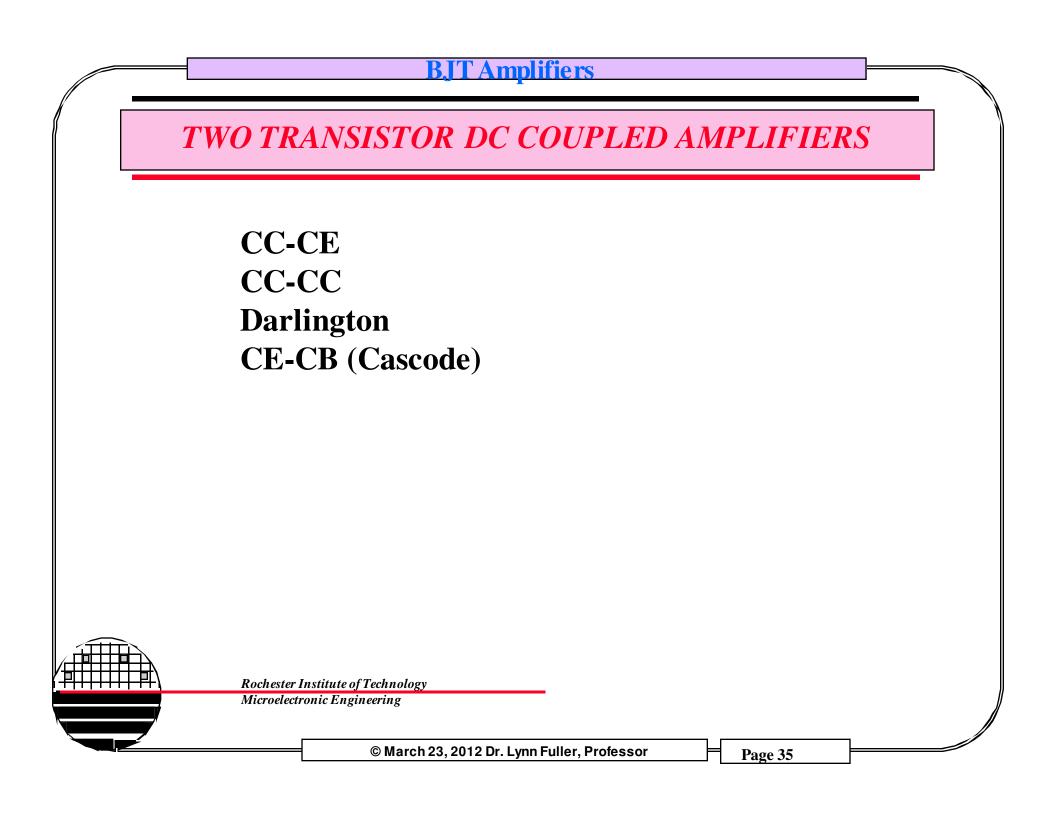
If you wish to include the effect of the source resistance RS on overall voltage gain *vo/vs* then reduce the gain by multiplying *vo/vin* by Rin/(Rin+RS)

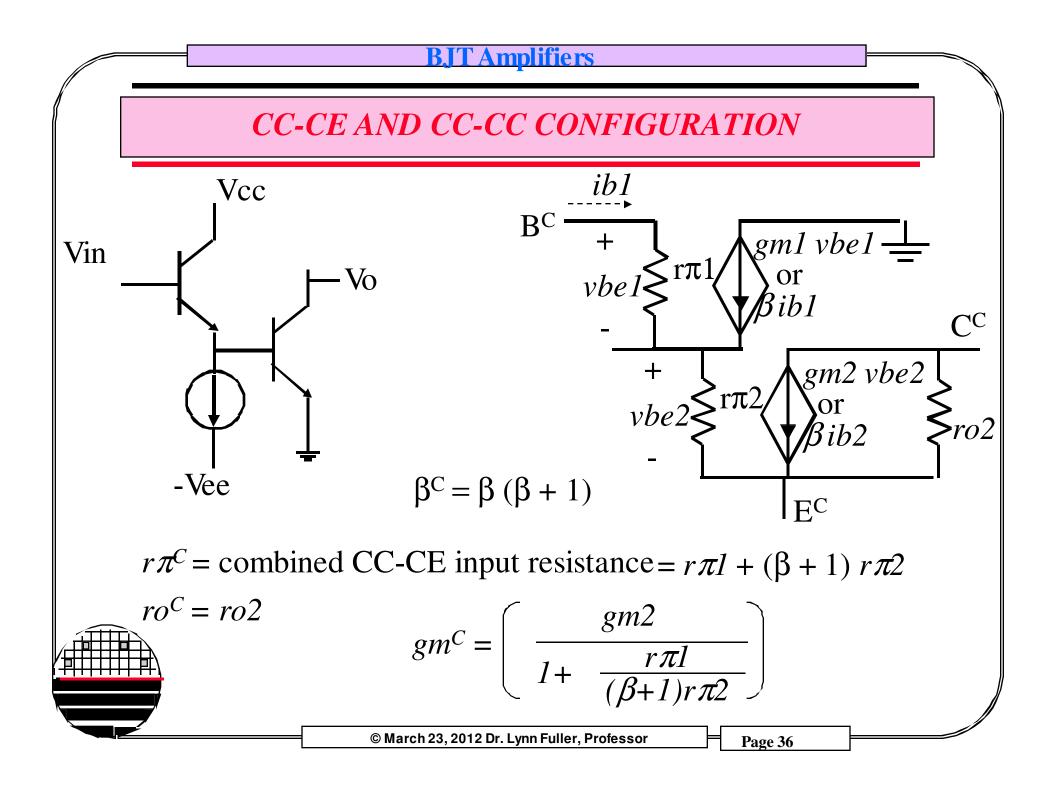
If you wish to include the effect of a load resistor RL on the overall voltage gain *vo/vs* then replace Rc with Rc//RL



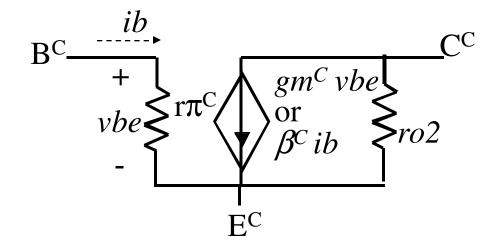
				BJT Ampl	ifiers				
SUMMARY FOR SINGLE TRANSISTOR AMPLIFIERS									
α	=IC/I	E					$\alpha = \beta/(\beta+1)$ $\beta = \alpha/(1-\alpha)$		
$\beta = IC/IB$ Rth = Thevenin equivalent of Base DC Bias network $\beta = \alpha/(1-\alpha)$									
	CE			СВ	CC		CE plus Re		
	Rin	$r\pi$ // Rth		$[r\pi/(\beta+1)]//Rth$	$Rth//[r\pi + (\beta+1)(RE//RL)]$		Rth//[$r\pi$ + (β +1)RE]		
	Ro	RC//ro		RC//ro	RE//[($r\pi$ + (RS//Rth))/(β +1)]		RC//ro		
	Av = o/vin	-gm (RC//RL//ro)		+ <i>gm</i> (RC//RL// <i>ro</i>)	$\frac{(\text{RE}//\text{RL}) (\beta+1)}{r\pi + (\text{RE}//\text{RL}) (\beta+1)} = \sim 1$		~ RC/RE		
$gm = IC/VT$ $mathbf{W} = 0.026 \text{ at room T}$ $ro = VA/IC$ $mathbf{W} = Barly \text{ Voltage}$ $\pi = \beta / gm$ $where VA = Early \text{ Voltage}$ $\pi \pi = \beta / gm$ $where VA = Early \text{ Voltage}$ $mathbf{W} = \frac{\beta}{23}$							AvVin +		







DARLINGTON CONFIGURATION



1. The darlington, when used in the CC configuration is the CC-CC configuration already discussed.

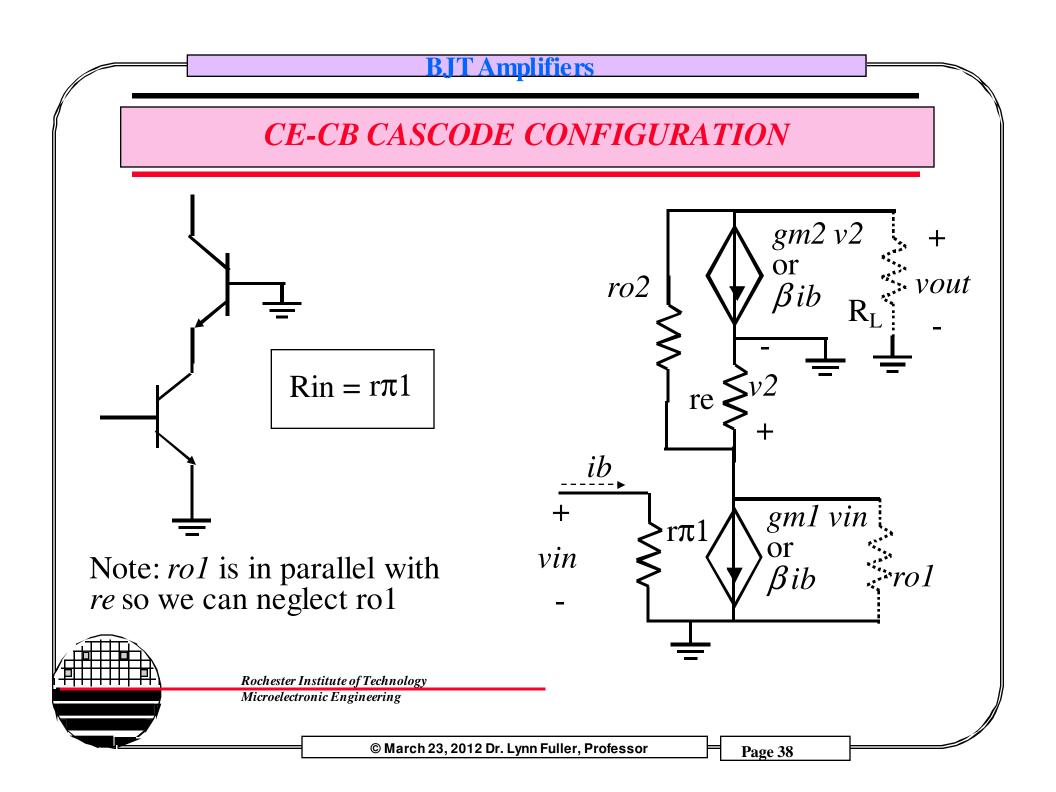
2. In the common emitter configuration the darlington is similar to the CC-CE configuration except that the collector of Q1 does not go to the supply, but rather it goes to the output. This reduces the output resistance and increases the input capacitance. Thus the CC-CE is preferred over the darlington.

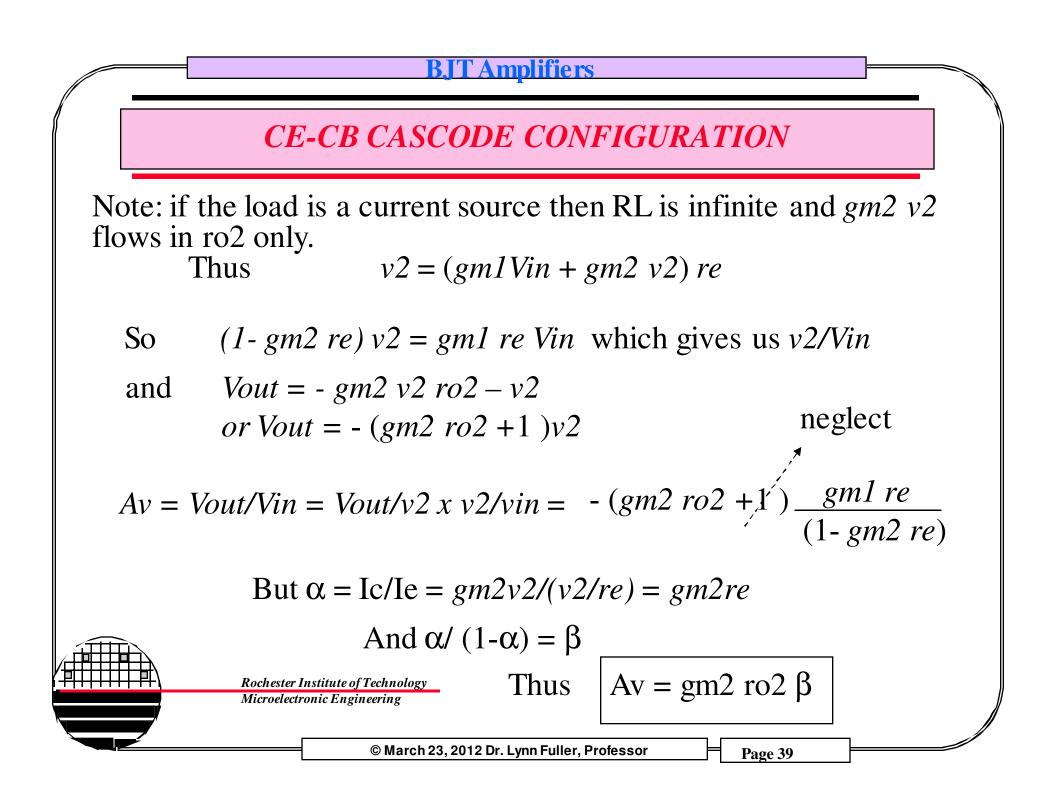
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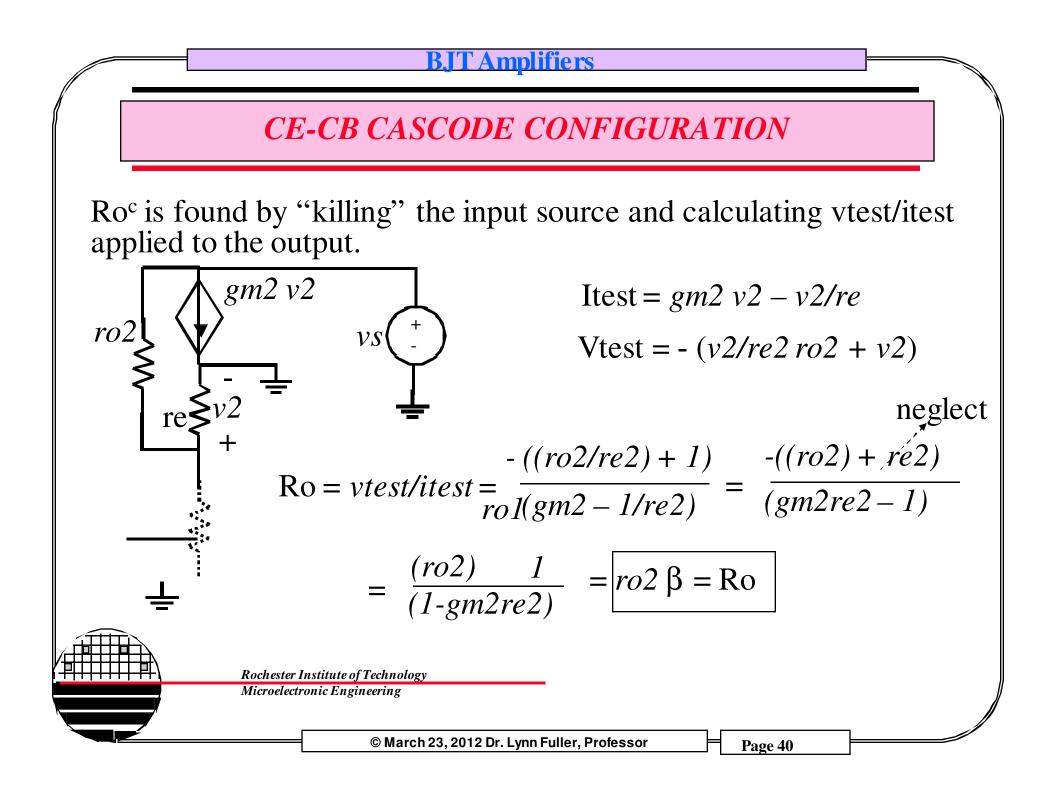
 $\mathbf{B}_{\mathbf{C}}$

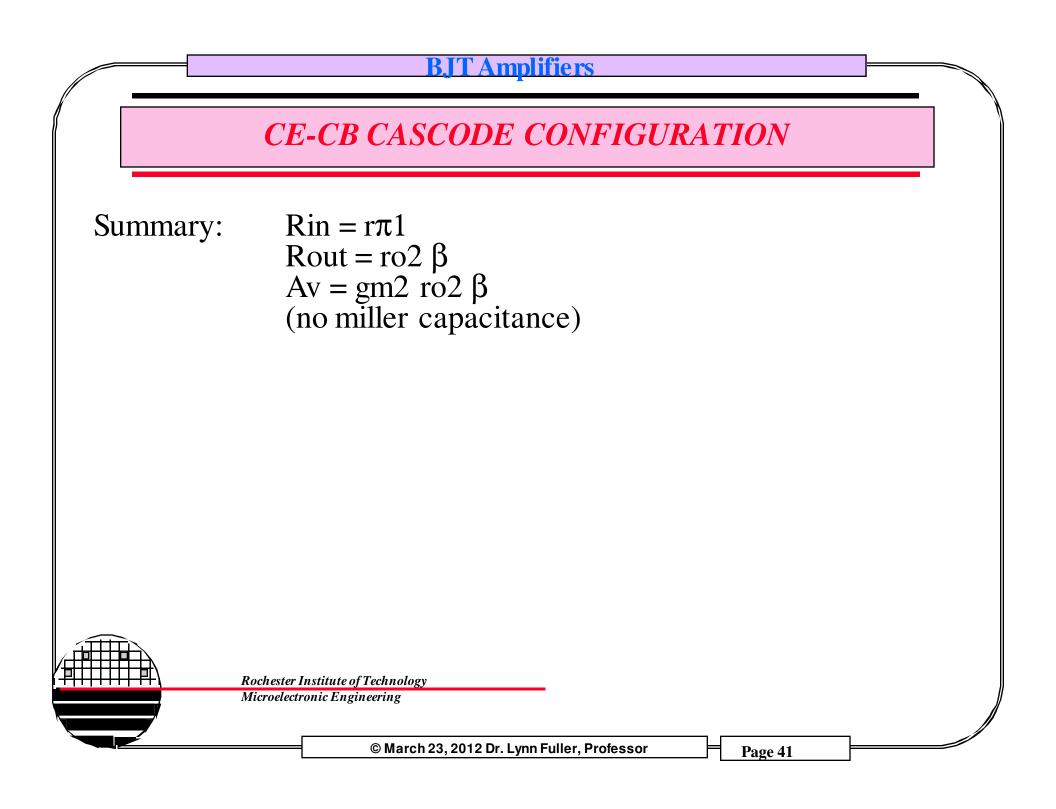
~C

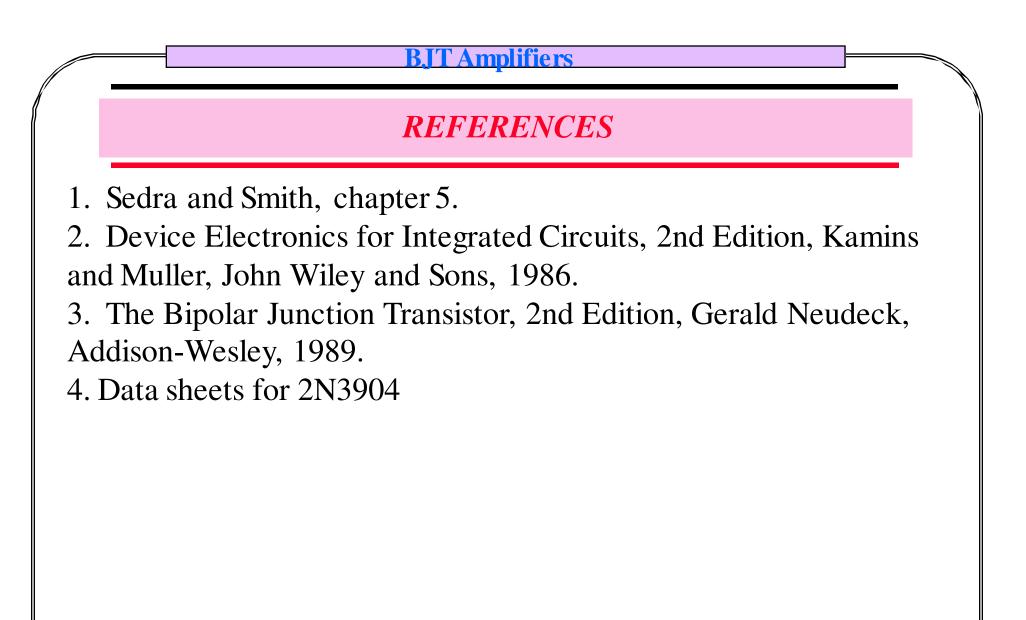
EC









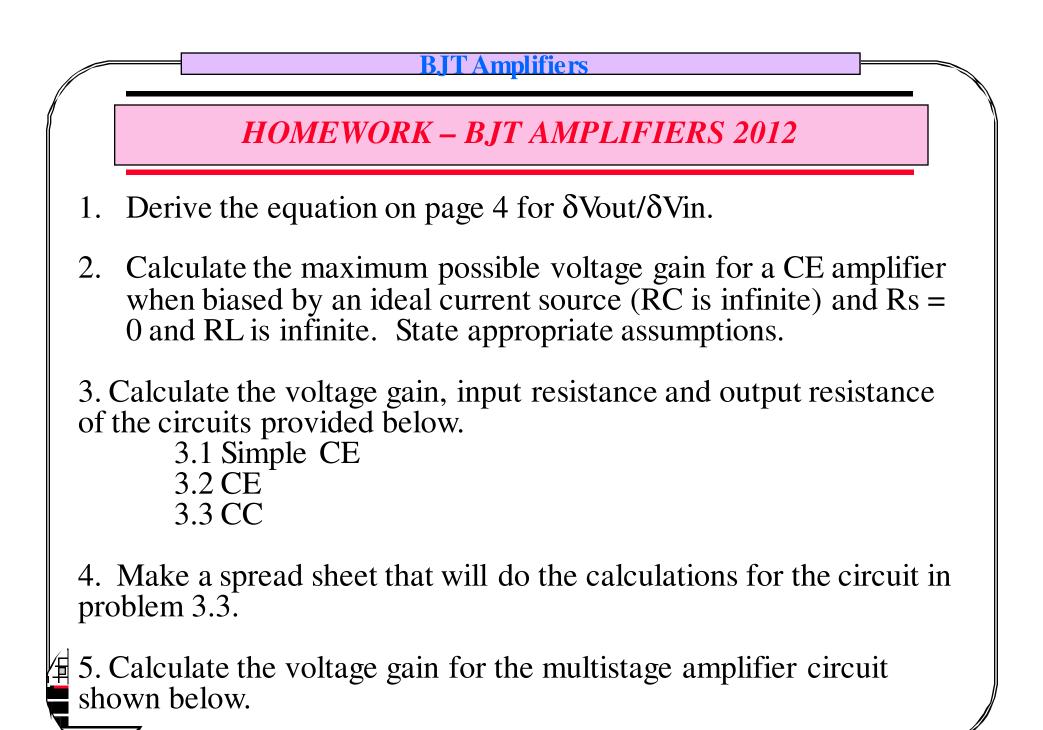


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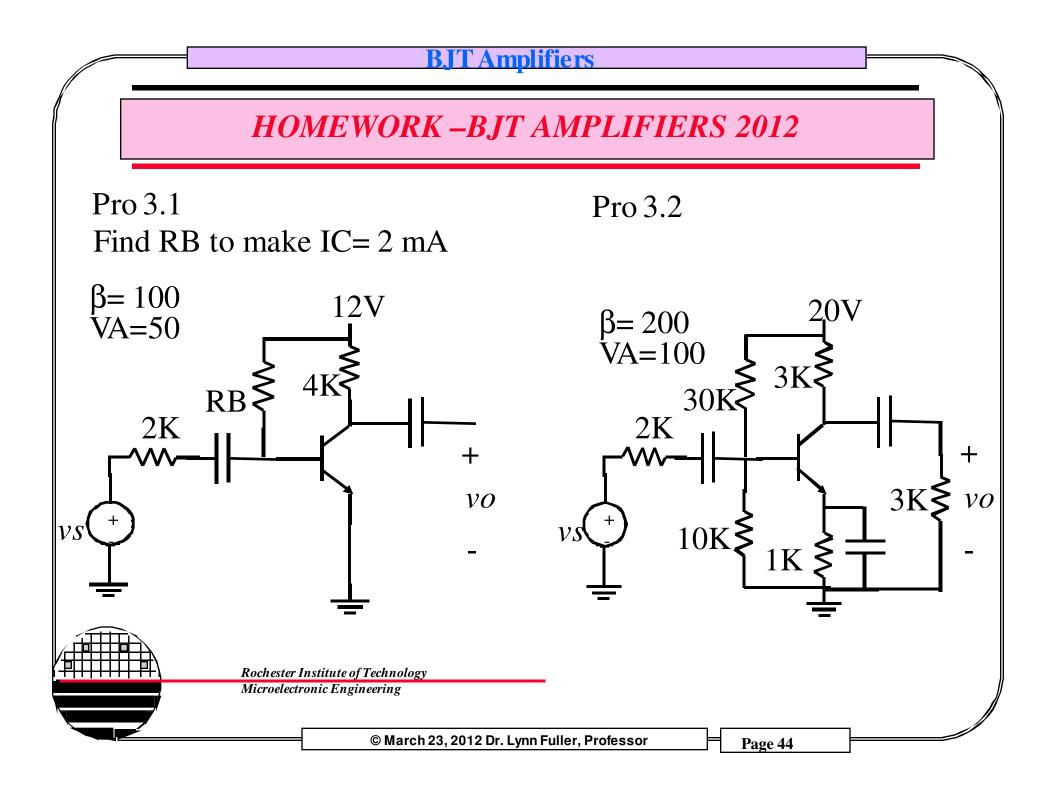
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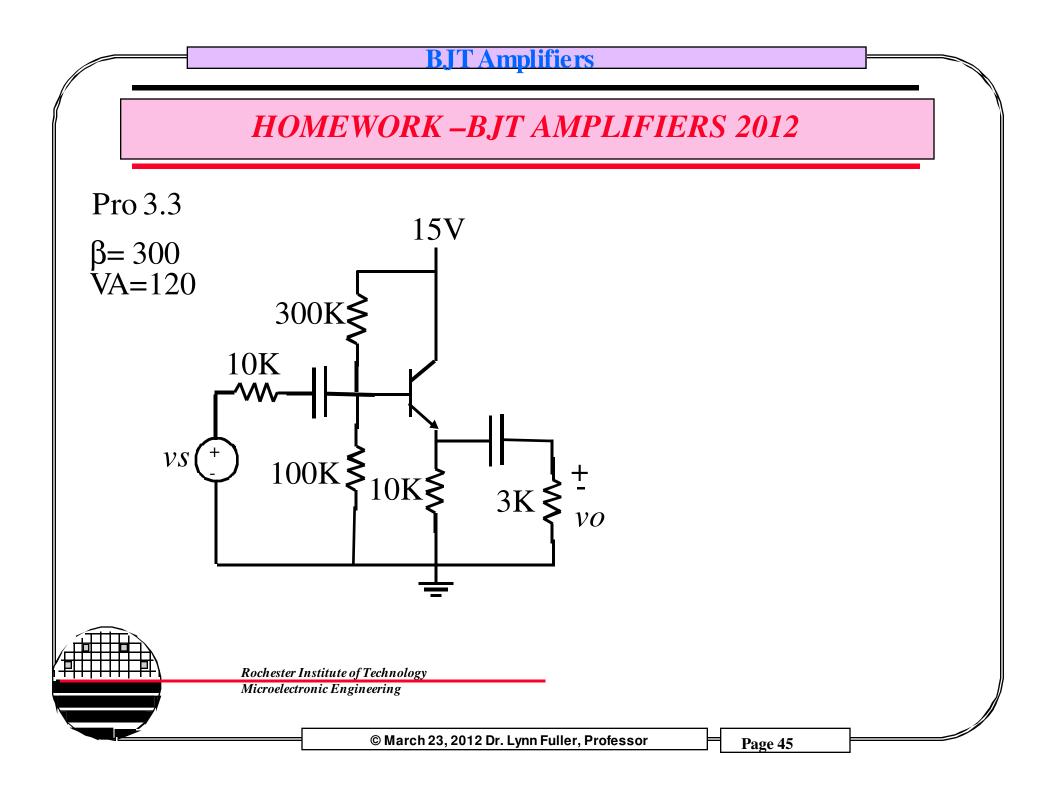
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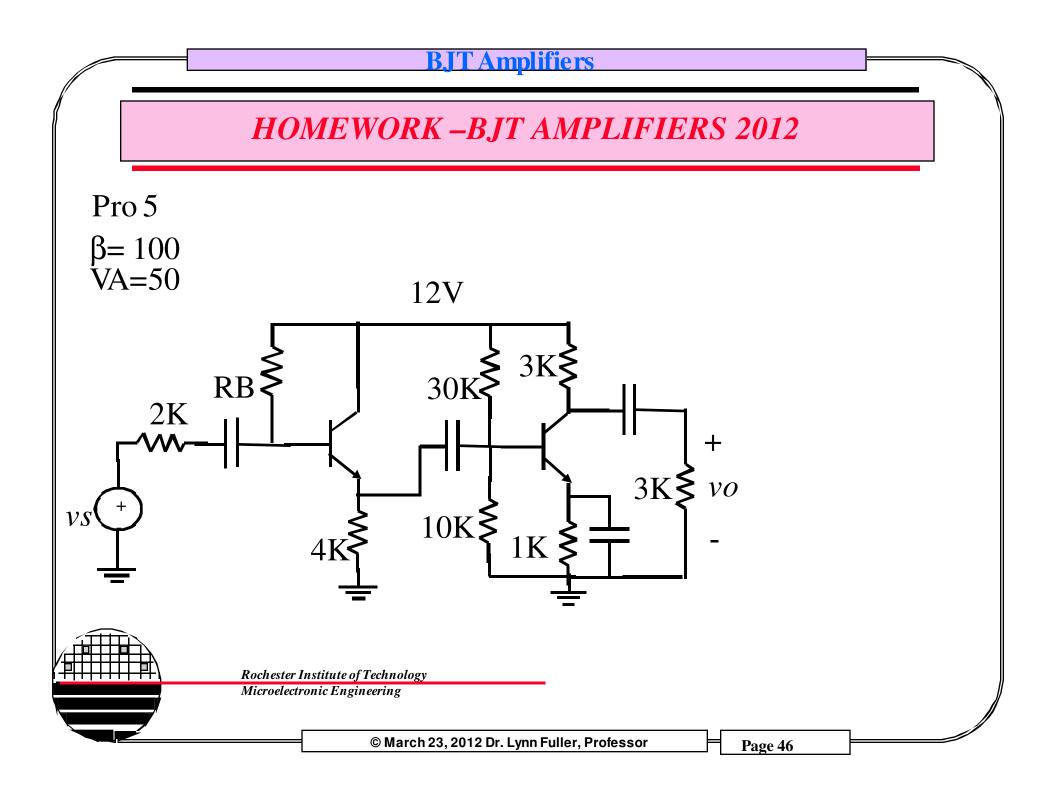


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BJT SPICE PARAMETERS

Name	Parameter	Unit	Default
IS	transport saturation current	А	1.0E-16
BF	ideal maximum forward beta	-	100
NF	forward current emission coefficient	-	1.0
VAF	forward Early voltage	V	infinite
IKF	corner for forward beta high current roll-off	А	infinite
ISE	B-E leakage saturation current	А	1.0E-13
NE	B-E leakage emission coefficient	-	1.5
BR	Ideal maximum reverse beta	-	1
NR	reverse current emission coefficient	-	1
VAR	reverse Early voltage	V	infinite
IKR	corner for reverse beta high current roll-off	А	infinite
ISC	B-C leakage saturation current	А	0
NC	B-C leakage emission coefficient	-	0.5
NK	high current roll-off coefficient	-	0.5
ISS	substrate p-n saturation current	А	0
NS	substrate emission coefficient	-	0.5
RE	emitter resistance	Ohm	0
RB	zero bias base resistance	Ohm	0
RBM	minimum base resistance	Ohm	RB
IRB	current where RB falls halfway to RBM	А	infinite
RC	collector resistance	Ohm	0
CJE	B-E zero-bias depletion capacitance	F	0
			/
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BJT SPICE PARAMETERS

Name	Parameter	Unit	Default
VJE	B-E built-in potential	V	0.75
MJE	B-E junction exponential factor	-	0.33
CJC	B-C zero-bias depletion capacitance	F	0
VJC	B-C built-in potential	V	0.75
MJC	B-C junction exponential factor	-	0.33
XCJC	fraction of B-C capacitance connected to base	-	1
CJS	zero bias collector substrate capacitance	F	0
VJS	substrate junction built-in potential	V	0.75
MJS	substrate junction exponential factor	-	0
FC	coeff. Forward bias depletion capacitance	-	0.5
TF	ideal forward transit time	sec	0
XTF	coefficient for bias dependence of TF	-	0
VTF	voltage describing VBC dependence of TF	V	infinite
ITF	TF dependency on IC	А	0
PTF	excess phase at freq=1.0/(TF2pi) Hz	deg	0
TR	ideal reverse transit time	sec	0
QCO	epitaxial region charge factor	Coul	0
RCO	eitaxial region resistance	Ohm	0
VO	carrier mobility knee voltage	V	10
GAMM	A epitaxial region doping factor	-	1E-11
EG	energy gap for temperature effect on IS	eV	1.11
more			

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STANDARD RESISTOR VALUES

5% Standard Values Decade multiples are available from 10 Ω through 22 MΩ											
10	11	12	13	15	16	18	20	22	24	27	30
33	36	39	43	47	51	56	62	68	75	82	91

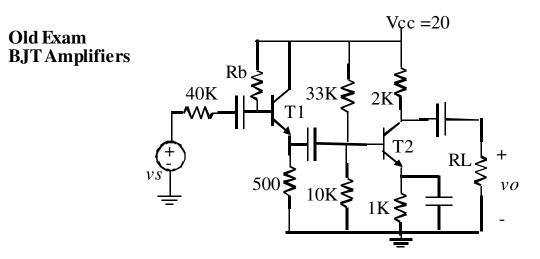
10% Standard Values Decade multiples are available from 10 Ω through 1 MΩ											
10	12	15	18	22	27	33	39	47	56	<mark>68</mark>	82

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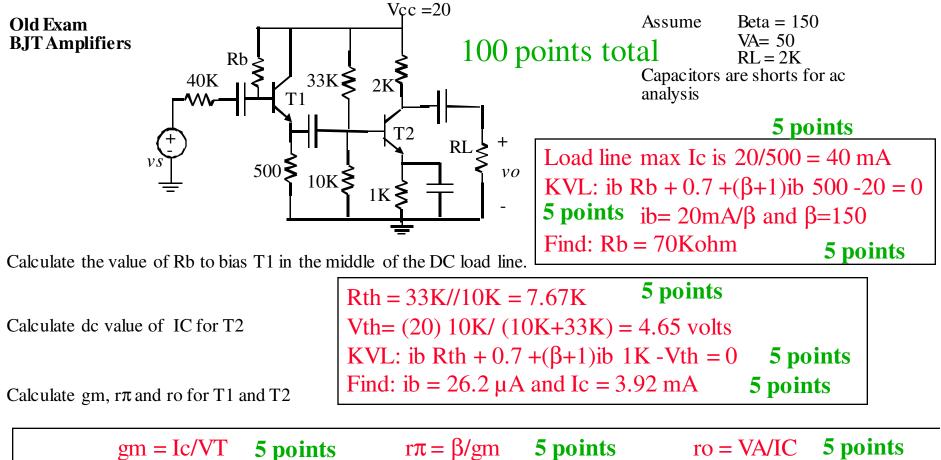
Assume Beta = 150VA= 50RL = 2KCapacitors are shorts for ac analysis

Calculate the value of Rb to bias T1 in the middle of the DC load line.

Calculate dc value of IC for T2

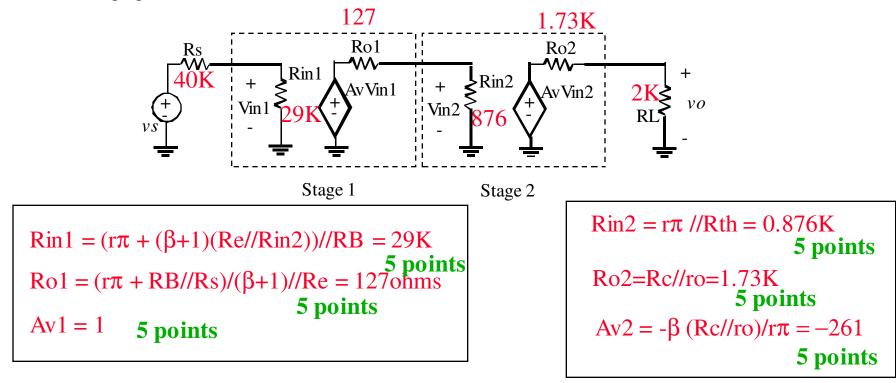
Calculate gm, $r\pi$ and ro for T1 and T2

Calculate the voltage gain volvs



	gin – ic/ v i S points	n – prgm – prgm	10 - VAIC 3 points
For T1:	gm = 20mA/0.026=0.769 S	$r\pi = 150/gm = 195$ ohm	ro = 50/20mA = 2.5K
For T2	gm = 3.92mA/0.026=0.151 S	$r\pi = 150/gm = 0.989Kohm$	ro = 50/3.92mA = 12.7K

Calculate the voltage gain volvs



vo= {RL/(RL+Ro2)}Av2 {Rin2/(Ro1+Rin2)} Av1 {Rin1/(Rs+Rin1)} vs 5 points vo/vs = -(0.54)(261)(0.862)(1)(0.42)= -51.7 5 points