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Microstructural and Chemical Analysis of HgCdTe/CdTe/ZnTe/Si (211) for Infrared Detectors

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HgCdTe, (MCT), has been the predominant material for Infrared (IR) focal-plane-array (FPA) technology for the past 50 years [1]. However, growth of high quality MCT on scalable preferred substrates, such as Si, has been hindered due to the dislocation density induced by the large lattice mismatch (i.e. 19.5%) between Si and MCT [2]. In the present work, MCT layers were grown by molecular beam epitaxy on 2x2 cm^2 composite (211) substrates consisting of thin (~15 nm) ZnTe and thick (~10 µm) CdTe . The MCT structures consisted of LWIR or SWIR (nominal x=0.22 and 0.45, respectively) with varying thickness HgTe buffer layers (0, 4.7 or 18.8 nm thick) at the MCT/CdTe interface. The SWIR epilayers were grown with a final CdTe capping layer. Etch-pit density (EPD) measurements were obtained using Benson etch to determine which buffer reduced the defect density [3]. EPD indicates a slight improvement with a 15s (~4.7 nm) HgTe buffer layer. These samples were investigated by TEM to determine the effectiveness of the HgTe buffer layer as a defect blocking layer. <110> XTEM samples were prepared using standard mechanical polishing and dimpling to thicknesses of about 10-12 µm, with subsequent argon-ion milling at liquid nitrogen temperature to minimize possible ion-milling-induced artifacts [4]. For final thinning and to minimize formation of amorphous layers, low-angle, low voltage (approximately 2keV) milling was used. Cross section samples were studied using bright-field and high-resolution TEM, using Philips CM200-FEG, and JEOL JEM-4000EX, respectively.

Figure 1(a) shows SWIR material with 60 sec HgTe initial layer, with defects at the MCT/CdTe interface and in the upper regions of MCT that would be likely to affect the IR detector performance. Density of defects is larger at the CdTe/Si interface, Fig. 1(b), but decreases as the CdTe thickness increases. Higher magnification images of MCT/CdTe interface, Figs. 1(c) and (d), shows a (~14 nm) HgTe layer between the MCT/CdTe layers. Figure 2(a) shows a highly defective ZnTe layer between CdTe and Si which was intended to relieve strain during growth of the thick CdTe layer. Higher magnification inset at the left corner shows the presence of {111} stacking faults at the ZnTe/Si interface. The SAD pattern shows a 3.7 degree rotation between CdTe and Si crystal lattices, as expected based on previous work [5]. FFT calculations and EDS line scan profiles, Fig. 2(b), also confirm that this layer is ZnTe. Overall, the TEM observations showed that growth without the HgTe buffer layer had significantly more defective growth [6].

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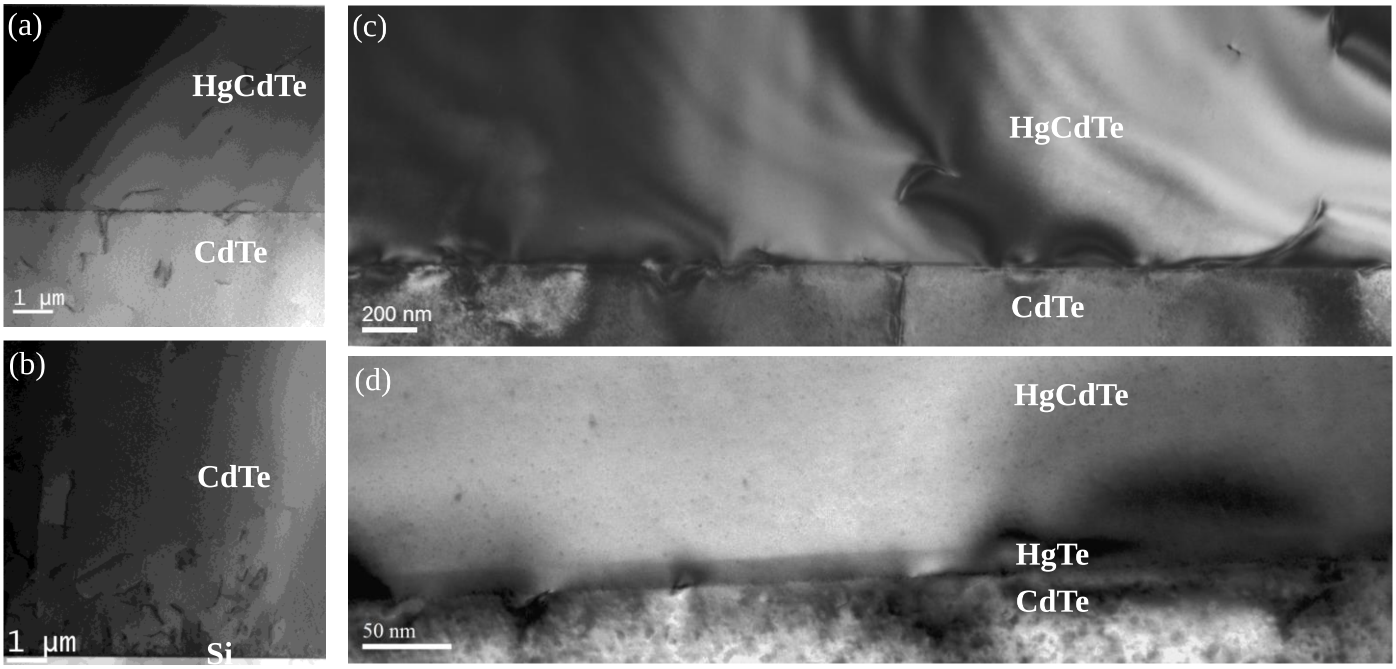

Figure 1. XTEM images of MCT/MT/CT/Si Heterostructure: (a) Low-mag image of MCT/CT, (b) Low-mag image of CT/Si, (c&d) High-mag images of HgCdTe/HgTe/CdTe interface region.

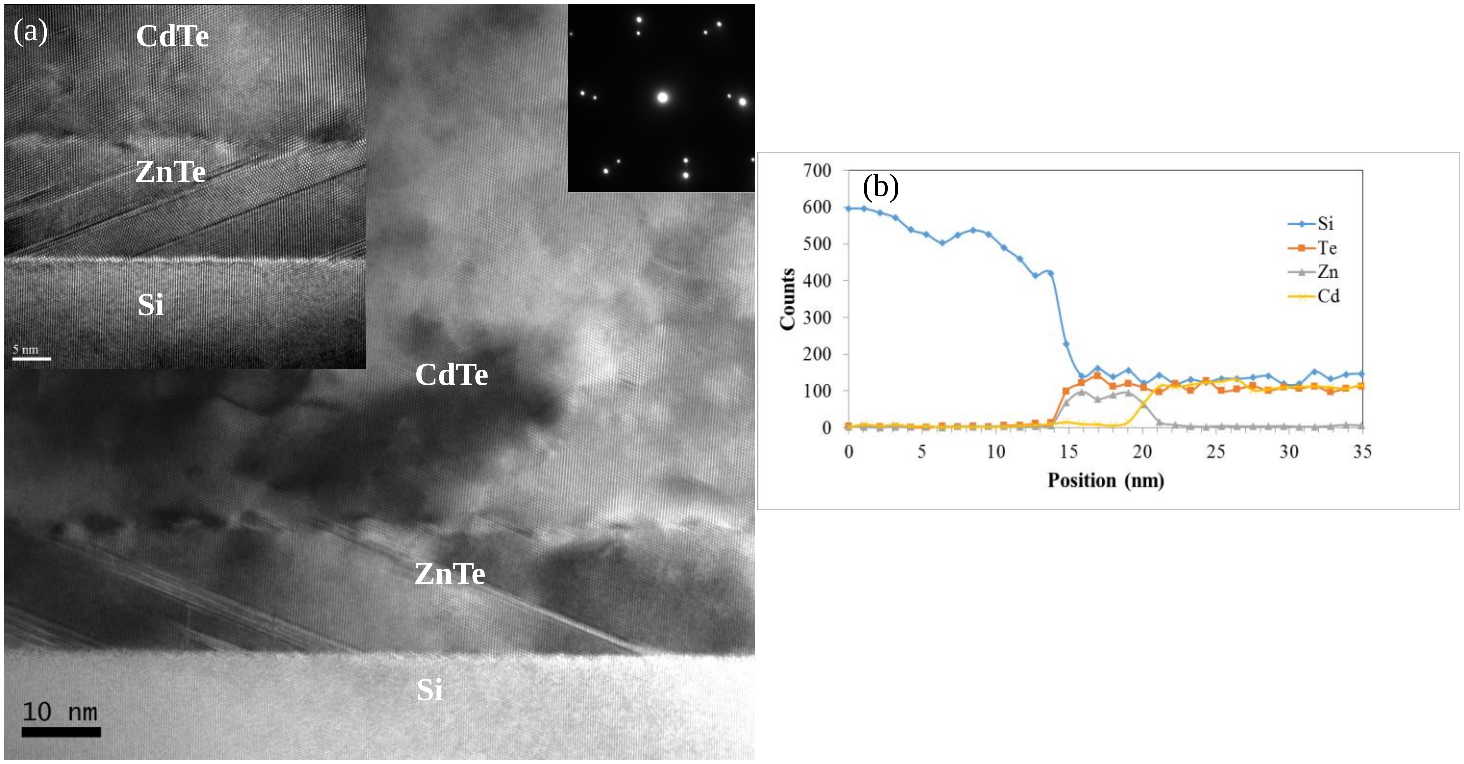

Figure 2. (a) XTEM images of CdTe/ZnTe/Si interface region, at two different magnifications with SAD pattern as inset, (b) EDS line scan profile across CdTe/ZnTe/Si interface.