

Using 3D Nanotomography to Visualize Defects in the Fabrication of Superconducting Electronics.

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Superconducting electronics is an established technological field for sensors, quantum computation and quantum-based standards and is emerging as an important low-power alternative to semiconductors. As with any electronics fabrication, the production of complex circuits requires many iterations and stringent quality control. In particular, post-fabrication metrology of buried circuit elements to diagnose device failures is of utmost importance to increase the yield [1] and complexity of superconducting based electronics. To fill this need, we have developed methods for the 3D visualization of superconducting electronic components based on focused ion beam – scanning electron (FIB-SEM) nanotomography.

Unlike in the semiconductor industry, which has long used FIB-SEM methods to investigate and edit circuits [2], superconducting electronics have not benefited from this technique. Since the basic structure of superconducting electronics is different than that of semiconducting electronics, device specific optimization has been required [3]. This optimization has led to the ability to produce tomograms of buried features at high speeds and visualize defects that are common in the fabrication of superconducting electronic devices.

To build these 3D tomograms, device structures of interest are selected and then milled at the highest rate that provides the needed resolution. As these structures are milled, SEM images are acquired at regular intervals. The resulting images are then corrected for drift, thresholded by relative brightness for the material of interest, and selectively cropped to produce a series of aligned images of the region and material of interest. This series of images is then viewed using the appropriate 3D visualization software [4]. In this way we create a 3D representation of fabricated structures that are used to explore both functioning and faulty devices allowing feedback to improve the fabrication of superconducting electronics.

Variations in the development and treatment of photoresist based etch masks can cause important variations in the geometry of devices. In Figure 1 A, the presence of residual resist has caused a sloped etch profile in the device layer. As with any multi-level electronics microfabrication process, each layer has the potential to introduce defects and reduced device yield in a multitude of ways. The layer to layer alignment or registration is a critical parameter. Misalignments of layers can cause shorts, improper etch masking and other device failures. In figure 1 B, a 3D rendering of a short is shown, along with a typical 2D electron micrograph. This short is caused by a registration error and effectively bypasses the circuit's active element, a Josephson junction. If the material coverage and edge profiles of each layer are not optimal underlying layers can be attacked by subsequent etching steps. In figure 2, the first and last image frames of a tomographic series are shown. In this series, extended defects at the interface of Nb, SiO₂ and Si are highlighted in 3D reconstructions by isolating the material of interest through brightness and repeatedly reconstructing the data to show the effect of the defects on different layers. In summary, we will present the methods and results of using FIB nanotomography in superconducting electronics for post fabrication 3D visualization.

References:

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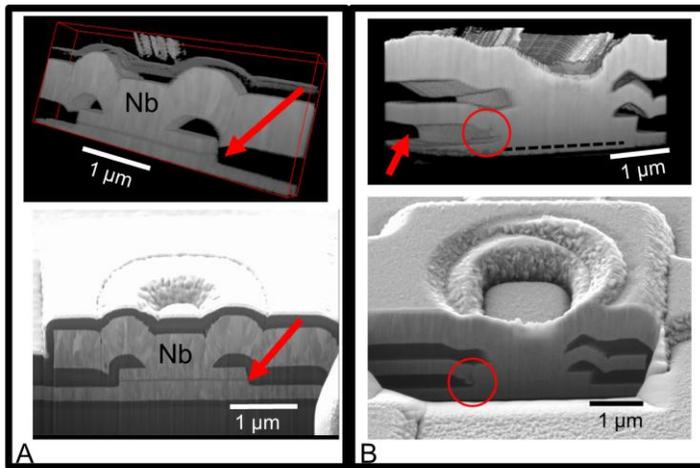


Figure 1. Sloped etch profile and short visualized by FIB nanotomography A) A raw slice illustrating a sloped device wall resulting from photoresist etch mask residue (red arrow), and the 3D tomogram (top) showing that it propagates along the device. B) A raw slice with an area circled for reference and the 3D tomogram (top) showing a buried short (red arrow).

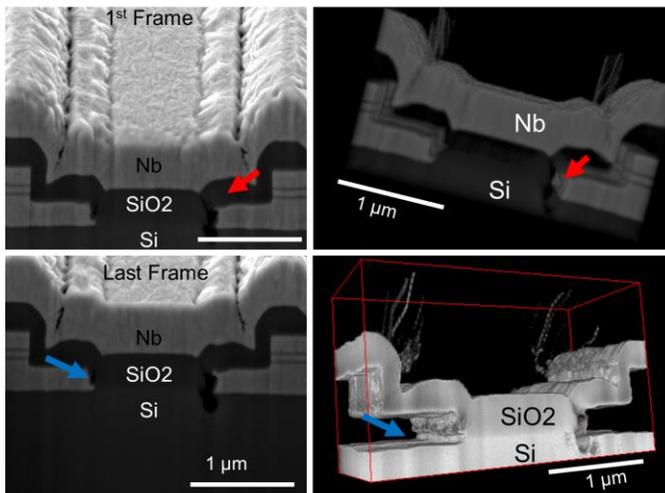


Figure 2. Extended defects at complex interfaces highlighted by brightness based material selection. Left, the first and last raw image processed to create the 3D tomogram. A void left by etching at the interface of a metal device layer, an oxide layer and the Si substrate (red arrow) is seen to extend into the device structure (top right). A similar etch defect is seen on the interface of only the oxide and metal (blue arrows) as shown in the 3D tomogram on the bottom right.