

The Perfect Cut: Focused Ion Beam Preparation for In Situ TEM

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In situ TEM techniques have improved considerably in recent years with respect to their ability to understand materials behavior with high temporal and spatial resolution. While significant advances have been made in elucidating atomic-scale mechanisms that control properties of materials for a wide range of applications, geometric compromises made to accommodate in situ TEM experiments could play a detrimental role in the ability to apply data to “real-life” structures or devices.

In recent years, focused ion beam (FIB) preparation has gained a stronghold in the in situ TEM community as it allows for complex architectures to be prepared for specific holders. Because of the requirements and limitations of many in situ experiment geometries, the FIB provides a necessary platform toward achieving the proper lay-out, ranging from connecting electrical contacts to fabricating nanopillars. The overarching drawbacks of ion beam damage and preparation time, however, remain a challenge.

This talk examines the interplay between the need to mimic a true application and the need to access microstructural features at the nanoscale, and how this can be achieved using FIB lift-out procedures. Case studies of high electron mobility transistors [1], ferroelectric memory devices [2-4], and alloys for nuclear energy applications will be reviewed. Specifically, the preparation of gated device structures for electrical degradation measurements and the analysis of microstructure-specific corrosion in Zircaloy will be presented.

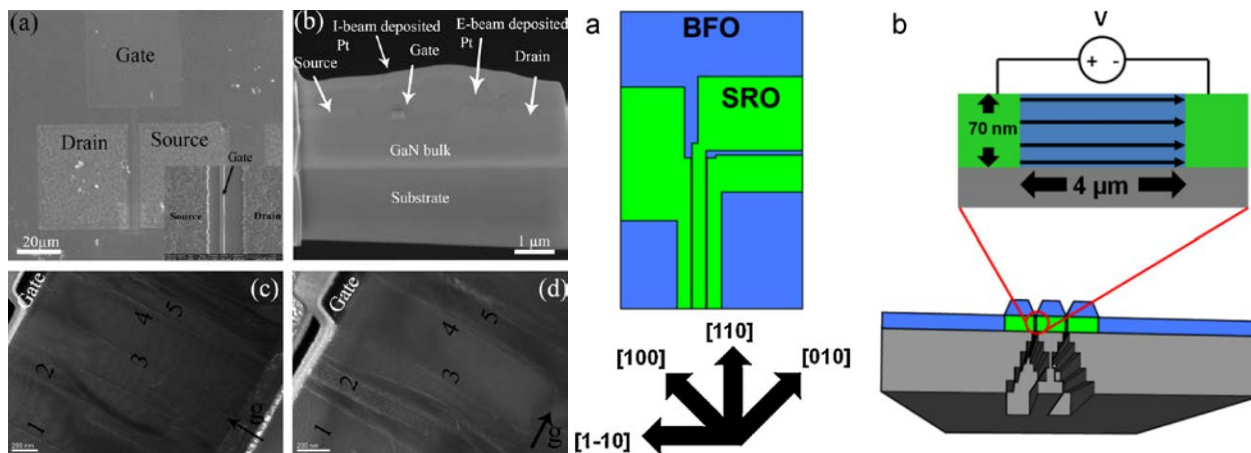


Figure 1. (a) SEM image of a typical AlGaIn/GaN HEMT in the pristine (unbiased) state, (b) Crosssection view of the lift-out indicates the features of the device as well as the Pt protective layers. (c) and (d) represent weak-beam dark-field TEM images of drain-gate region at two different diffraction conditions of $g \frac{1}{4} \frac{1}{2} 0002$ and $g \frac{1}{4} \frac{1}{2} 1120$, respectively. Scale bars are 200 nm and the threading dislocations are labeled as 1–5, from [1]

Figure 2. Schematic diagrams of an in situ biasing geometry for BFO (ferroelectric) domain switching experiments, revealing: (a) a plan-view of BFO device structure with SRO electrodes, (b) a side-view of FIB-thinned region of STO substrate with an enlarged schematic showing the planar applied voltage between the SRO electrodes, from [3]

References

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