Silicon for thin-film transistors

Sigurd Wagner*, Helena Gleskova, I-Chun Cheng, Ming Wu

Department of Electrical Engineering and POEM, Princeton University, Princeton, NJ 08544, USA
Aegis Semiconductor, 78 Olympia Avenue, Woburn, MA 01810, USA

Abstract

We are standing at the beginning of the industrialization of flexible thin-film transistor (TFT) backplanes. The two important research directions for the TFTs are (i) processability on flexible substrates and (ii) sufficient field-effect mobilities of electrons and holes to support complementary metal insulator semiconductor operation. The most important group of TFT capable semiconductors are the several modifications of silicon films: amorphous, nanocrystalline and microcrystalline. We summarize their TFT properties and their compatibility with foil substrate materials.

Keywords: Transistors; Flexible substrates; Thin films

1. Introduction

The commercial success of active-matrix liquid-crystal displays (AM-LCDs) has stimulated considerable research on thin-film transistors (TFTs), which function as the pixel switches in AM-LCDs. TFT channels can be made of silicon, small-molecule or polymer organics, and a few near-ionic compound semiconductors like CdSe. Among these alternatives silicon enjoys a considerable advantage because it draws from a vast technology base [1], and because amorphous silicon TFTs are the current industrial standard. The a-Si:H TFTs are used primarily as pixel switches, but are explored for current sources [2], on-pixel amplifiers [3], and peripheral driver circuits [4,5]. The complementary circuits required for low-power operation are out of reach of a-Si:H because its electron mobility is low and its hole mobility is insufficient for p channel operation. Nanocrystalline (nc) and microcrystalline (μc) silicon, with their higher field-effect mobilities, considerably expand the range of application of silicon TFTs. nc- and μc-Si are capable of p and n channel and thus of complementary metal insulator semiconductor (CMOS) operation. When used for peripheral driver circuits, they can enable high-level on-glass integration. High-level integration raises yield and reduces cost. nc- and μc-Si TFTs also are capable of driving high-current loads such as organic light emitting diodes (OLEDs).

The next frontier of the flat panel display industry, flexible and conformal displays, extends the motivation for exploring CMOS and high-current capable Si TFTs to their fabrication on flexible foil substrates. Flexible displays are attractive because flexibility is associated with light weight and ruggedness. These are desirable features for portable applications today, and even more so for the large-area displays, e-textiles and mechatronic materials of tomorrow.

2. Silicon for thin-film transistors

The two important research directions for TFTs are high mobility and flexible substrates. All TFT applications benefit from a high ‘on’ current, which is proportional to carrier mobility. Simple switches and on-pixel circuits (e.g. preamplifiers) can be implemented with n channel TFTs. Monolithic integration with peripheral circuits and reduction of power consumption need also p channel TFTs. Because of their particular contact configuration OLEDs also benefit from p channel TFT current sources. The need for high mobility makes the grain size of silicon films take on overriding importance, regardless of the substrate material on which the silicon is deposited. In consequence the correlation between mobility/grain size and process temperature dominates
the research on channel materials for silicon TFTs. By imposing a maximum process temperature of \( \sim 600 \, ^\circ C \), glass substrates have forced the invention of low-temperature processes for the crystallization of precursor layers and for device fabrication. By tolerating temperatures of close to \( 1000 \, ^\circ C \), steel substrates permit the adoption of many processes used by the integrated circuit industry. In contrast, the low-temperature stability of organic polymer (‘plastic’) substrates demands a broad revision of TFT materials, device geometry, and processes. a-Si TFTs may be brought to plastic by careful adaptation of the established 250–350 \( ^\circ C \) processes to the temperatures of 150 \( ^\circ C \) or less tolerated by plastics. With their top gate geometry, SiO\(_2\) dielectric, and reduced tolerance to series resistances, high-mobility TFTs made from directly deposited nc-Si or from laser crystallized \( \mu \)c-Si pose much greater challenges to fabrication on plastic. Making the ancillary materials, including a stable gate dielectric and highly conducting contacts at temperatures of \( \sim 100 \, ^\circ C \) may turn out to be more demanding on the fabrication of silicon TFT CMOS on plastic substrates than the preparation of the channel material itself.

The modifications of silicon available for TFTs, as well as approximate regimes of carrier mobility and device type, are shown in Fig. 1, where grain size serves as the running parameter.

TFT grade silicon can be made on foil substrates in three ways: (1) deposition of a precursor film followed by crystallization; (2) direct deposition of the channel semiconductor; (3) physical transfer of separately fabricated circuits. Table 1 lists the three grades of thin-film silicon that are available for the fabrication of TFT backplanes on foil substrates [1].

Amorphous silicon backplanes can be made at the standard process temperature of 250–350 \( ^\circ C \) on steel [2,6] and at \( \sim 100–150 \, ^\circ C \) on plastic [7–14] foil substrates. Nanocrystalline silicon TFTs [15–20] are made at the same low temperatures as a-Si, and can be made with p or n channels. Thus they are capable of CMOS [18], but their device and process technology is immature.

<table>
<thead>
<tr>
<th>Attribute</th>
<th>a-Si:H</th>
<th>nc-Si:H</th>
<th>( \mu )c-Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard deposition ( T ) (( ^\circ C ))</td>
<td>250</td>
<td>250</td>
<td>150 (precursor)</td>
</tr>
<tr>
<td>Highest ( T ) process/material (( ^\circ C ))</td>
<td>350</td>
<td>280</td>
<td>Laser</td>
</tr>
<tr>
<td>Lowest reported process ( T ) (( ^\circ C ))</td>
<td>SiN(_2)</td>
<td>n(^+), p(^+)</td>
<td>( \mu )c-Si</td>
</tr>
<tr>
<td>Electron mobility (( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} ))</td>
<td>110</td>
<td>150</td>
<td>Laser</td>
</tr>
<tr>
<td>Hole ( \mu ) (( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} ))</td>
<td>0.5–1</td>
<td>40</td>
<td>300</td>
</tr>
<tr>
<td>Conductivity (( \text{S} \text{cm}^{-1} ))</td>
<td>( \sim 0.01 )</td>
<td>0.2</td>
<td>50</td>
</tr>
<tr>
<td>Growth rate (( \text{nm} \text{s}^{-1} ))</td>
<td>( 10^{-11} )</td>
<td>( 10^{-1}–10^{-2} )</td>
<td>( 10^{-6} )</td>
</tr>
<tr>
<td>Gate and source/drain geometry</td>
<td>Bottom</td>
<td>Top</td>
<td>Top</td>
</tr>
<tr>
<td></td>
<td>Staggered</td>
<td>Coplanar or staggered</td>
<td>Coplanar</td>
</tr>
<tr>
<td>Gate insulator</td>
<td>SiN(_2)</td>
<td>SiO(_2)</td>
<td>SiO(_2)</td>
</tr>
</tbody>
</table>
Micro (or poly) crystalline silicon provides CMOS with the highest mobilities but requires high-temperature processing [21,22]. Furnace processing is acceptable for steel substrates. Laser crystallization for steel [23,24] and plastic [25] substrates has been demonstrated.

In view of the early stage of silicon TFT technology on foil substrates, and of the still uncertain future of organic and CdSe TFT technologies, considerable opportunities exist for establishing proprietary positions in TFT backplanes.

3. Foil substrates

Table 2 presents a chart of compatibility of silicon with the main groups of substrate materials. Because steel foil can be processed up to 1000 °C, all conceivable silicon TFT fabrication can be carried out on it, from a-Si:H to μc-Si, like on quartz glass. However, steel is opaque and couples in a large parasitic capacitance. Plastic foils can be transparent and even clear, but may be processed up to only 100 or 200 °C. Plastic substrates present many new challenges, which have been recognized only in part.

Nearly arbitrary foil thicknesses can be chosen, with a-Si:H TFTs having been fabricated on stainless steel foils as thin as 3 μm [26]. We have found 25-μm thick stainless steel foil and 50-μm thick polyimide foil convenient to work with.

4. Direct deposition of silicon on plastic

The direct deposition of device-grade silicon onto plastic brings up many substrate issues. Desirable are thermal and chemical stability, high softening or glass transition temperature, low coefficients of thermal and humidity expansion, low shrinkage during circuit fabrication, low solubility for water, low permeability by water and oxygen, good film adhesion, low chemical and mechanical inhomogeneity, and low surface roughness [13,14]. The roughness of Kapton E does not seem to impair TFT operation. We select plastic substrates primarily by (i) high thermal stability, (ii) low coefficient of thermal expansion, and (iii) film adhesion. The first layer to go down is critical as it provides adhesion, planarizes, passivates the substrate against process chemicals, and encapsulates against degassing and contamination. Our standard combination of plastic substrate and encapsulant are the polyimide Kapton and a film of silicon nitride as shown in the schematic cross-section of Fig. 2 [13]. Deposition of both a-Si:H and nc-Si:H by plasma-enhanced chemical vapor deposition (PE-CVD) is compatible with plastic substrates, because it can be adapted to \( T = 150 \) °C [19].

5. Amorphous silicon

PE-CVD of a-Si:H at \( T = 250–300 \) °C is a well-characterized baseline process and provides reproducible material. The advantage of PE-CVD for the deposition of device-grade silicon at 150 °C is that it requires only an extension instead of a new deposition technique. This advantage is demonstrated by the field-effect mobilities measured in a-Si:H (\( \mu_a \approx 0.5 \) cm² V⁻¹ s⁻¹) and in nc-Si:H (\( \mu_a \approx 40 \) cm² V⁻¹ s⁻¹ and \( \mu_p \approx 0.2 \) cm² V⁻¹ s⁻¹) deposited at 150 °C [19,20].

Lower-temperature processing requires the re-optimization of all higher-temperature steps. It is known that the quality of the amorphous silicon (a-Si:H) and silicon nitride (SiNₓ) deposited by PE-CVD deteriorates with decreasing deposition temperature. To overcome this problem the source gases are diluted with hydrogen to ensure that the electronic properties of a-Si:H and SiNₓ layers are comparable to those of a-Si:H/SiNₓ grown at the optimum temperature of 250–350 °C. When a device process is brought from high to low temperature, the most critical re-optimization is that of the highest-temperature process and material. In the a-Si:H TFT that is the SiNₓ gate dielectric. Device quality SiNₓ gate dielectric deposited at the standard temperatures of 300–350 °C usually is slightly nitrogen rich. The threshold voltage of the TFTs is lowest when the refractive index of the SiNₓ layer lies in the range of 1.85–1.90. The

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Table 2
Compatibility of directly deposited silicon channels with substrate materials

<table>
<thead>
<tr>
<th>Substrate material and ( T ) limit</th>
<th>Plastic</th>
<th>Glass</th>
<th>Steel</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFT use ( \leq 150 ) °C</td>
<td>( \leq 600 ) °C</td>
<td>( \leq 1000 ) °C</td>
<td></td>
</tr>
<tr>
<td>Preferred for cell switch (n channel)</td>
<td>a-Si:H</td>
<td>a-Si:H</td>
<td>a-Si:H</td>
</tr>
<tr>
<td>Preferred for peripheral circuits</td>
<td>nc-Si:H</td>
<td>μc-Si or nc-Si:H</td>
<td>μc-Si or nc-Si:H</td>
</tr>
<tr>
<td>(n and p channel)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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Fig. 3. Fabrication of nc-Si TFTs for plastic substrates. The nc-Si is grown in two steps to achieve a combination of high field-effect mobility with low TFT ‘off’ current. From Ref. 20.

index of refraction is related to the stoichiometry of the film, being larger for silicon-rich films. Our optimized 150 °C film has a growth rate of 1.5 Å s⁻¹, index of refraction at the wavelength of 632.8 nm n=1.80, dielectric constant ε=7.46, dielectric breakdown field > 3.4 MV cm⁻¹, Si/N ratio of 0.67, and H content of ~2×10⁻²² cm⁻³.

We fabricated arrays of a-Si:H TFTs on 51-μm thick Kapton E (Fig. 2) at the maximum process temperature of 150 °C. First, the polyimide substrate is coated on both sides with a 0.5-μm thick layer of SiNₓ. The TFTs have a staggered bottom gate geometry with the channel passivated by SiNₓ. All TFTs have the following structure: ~100-nm thick Ti/Cr layer as gate electrode, ~360 nm of gate SiNₓ as gate dielectric, ~100 nm of undoped a-Si:H as channel material, 180 nm of passivating SiNₓ, ~50 nm of (n⁺) a-Si:H, and ~100-nm thick Al for the source–drain contacts. The stress is optimized in all TFT layers to make the substrate come out flat after fabrication. The transistors were annealed after fabrication. Complete a-Si:H TFT backplanes have been made using this process [14].

6. Nanocrystalline silicon

c-Si:H TFT fabrication needs considerably more research than that of 150 °C a-Si:H TFTs. The structural evolution of nc-Si, from amorphous close to the substrate to increasingly granular as the film grows thick, has two consequences. One is a rise in the carrier mobilities in the top layer of the film. The electron field-effect mobility grows from that in a-Si:H to ~40 cm² V⁻¹ s⁻¹ and the hole mobility to ~0.2 cm² V⁻¹ s⁻¹ in fully connected nc-Si layers (the maximum mobility values are likely to go up with progress in device fabrication). The rise in mobility with film thickness reflects the change in the dominating mechanism, from trapping and re-emission out of bandgap states to emission over electrostatic barriers at grain boundaries. The structure of nc-Si explains why top gate TFTs of nc-Si exhibit much higher field-effect mobilities than bottom gate TFTs. A second consequence of the a-Si:H → nc-Si evolution is the electrical activation in nc-Si of (unwanted) impurities that are inactive in a-Si:H. As is already known from solar cell research, the electrical conductivity of nominally undoped nc-Si can be quite high. While the conductivity of intrinsic crystalline Si is ~10⁻⁵ S cm⁻¹, that of not intentionally doped nc-Si may reach 10⁻² S cm⁻¹, and can be brought to values as low as 10⁻⁷ S cm⁻¹. Because the ‘off’ current of TFTs is set by the conductance of the channel layer, care must be taken to keep the thickness-averaged electrical conductivity of the channel layer low, and still grow a top layer with high field-effect mobilities. This combination ensures low ‘off’ current and high ‘on’ current, and can be obtained by careful adjustment of nc-Si growth conditions and layer thickness, which may be as low as 50 nm [27] or as high as 300 nm. A typical fabrication sequence that includes the deposition of a nc-Si nucleation layer is shown in Fig. 3. The approach to developing the nc-Si structure (direct or pre-nucleation), the location of source/drain contacts (in-plane or staggered), efficient source/drain doping (particularly p⁺), the type of gate dielectric (SiO₂ or SiNₓ), and techniques for post-process annealing, are not settled however. All TFT technologies for plastic (silicon, organics, CdSe) share the need for a high-quality gate dielectric made at ultra-low temperature. A promising direction is growing the silicon dioxide under hydrogen free conditions. The gate dielectric will remain at the focus of TFT research for some time to come, regardless of the type of channel semiconductor.
7. Microcrystalline silicon

The furnace crystallization of a-Si precursor films to microcrystalline silicon films for TFTs is an established technology. Laser crystallization on glass substrates also has entered industrial production. When the fabrication of poly-Si films is done on steel foil substrates, it is a simple extension of the crystallization on glass but with greater process latitude. Laser crystallization of a-Si on plastic substrates and the subsequent fabrication of TFTs are among the experimentally most demanding directions in TFT research. μc-Si TFTs, including μc-Si TFTs on steel foil [28,29], warrant a separate discussion.

8. Outlook

Silicon films are leading candidates for flexible and conformal TFT backplanes. nc-Si and μc-Si both are capable of CMOS operation, with nc-Si probably more amenable to fabrication on plastic foil substrates. The ultra-low temperature TFT process steps, in particular, for the doped source/drain layers and the gate dielectric, are posing considerable challenges, and may require new experimental approaches. Likewise, TFT geometries are not settled. Because large-area electronics is certain to grow to a new industry, making the required TFT backplanes offer the opportunity for challenging and sustained research.

Acknowledgments

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References