Pentacene Organic Thin-Film Transistors for Circuit and Display Applications

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Abstract—We have fabricated organic thin-film transistors (TFT’s) using the small-molecule polycyclic aromatic hydrocarbon pentacene as the active material. Devices were fabricated on glass substrates using low-temperature ion-beam deposited silicon dioxide as the gate dielectric, ion-beam deposited palladium for the source and drain contacts, and vacuum-evaporated pentacene to form the active layer. Excellent electrical characteristics were obtained, including carrier mobility as large as 0.6 cm²/V-s, on/off current ratio as large as 10⁶, and subthreshold slope as low as 0.7 V/dec, all record values for organic transistors fabricated on nonsingle-crystal substrates.

I. INTRODUCTION

Thin film transistors (TFT’s) using organic semiconductors as the active material are of interest for a number of applications. Used as pixel-access devices in active-matrix displays, organic TFT’s could complement liquid-crystal light valves or organic light emitting diodes (OLED’s) to allow inexpensive display fabrication on flexible, rugged, light-weight polymeric substrates. Used as switching devices for logic gates and memory arrays, organic transistors could permit the fabrication of very low cost integrated circuits on flexible, large-area substrates for applications like smart cards, smart price and inventory tags, and large-area sensor arrays [2], [3].

The performance of organic thin-film transistors (TFT’s) has improved dramatically over the last twelve years [4]–[8], and optimized organic TFT’s now show electrical characteristics similar to those obtained with hydrogenated amorphous silicon (a-Si:H) devices. For example, carrier field-effect mobilities larger than 1 cm²/V-s have been obtained in pentacene organic TFT’s [9]. In addition to a large carrier mobility, a large on/off current ratio is required for TFT’s to be useful as pixel-addressing devices in active-matrix displays. Small TFT subthreshold slope and near-zero threshold voltage are also important to reduce the power consumption of an integrated circuit or display. Finally, to address organic light emitters in all-organic emissive displays, TFT’s must be able to drive fairly large drain currents.

We have fabricated organic TFT’s using the small-molecule polycyclic aromatic hydrocarbon pentacene as the active material. Pentacene TFT’s have been fabricated previously in our laboratory and have shown excellent electrical characteristics, including field-effect mobility as large as 1.5 cm²/V-s, on/off current ratio larger than 10⁶, and subthreshold slope as low as 1.6 V/dec [9]. For simplicity, these early devices used a single-crystal silicon wafer as the substrate and gate electrode, with thermally grown silicon dioxide serving as the gate insulator. To allow TFT integration into circuits or displays, selective gate electrodes and a gate insulator that can be deposited at temperatures compatible with the substrate are required. Low deposition temperatures are of particular concern if devices are to be fabricated on light-weight, flexible polymeric substrates. In this work, silicon dioxide deposited by reactive ion-beam sputtering at a substrate temperature of 80 °C was used as the gate dielectric, and pentacene TFT’s with excellent electrical characteristics were obtained.

II. DEVICE FABRICATION

All transistors were fabricated on borosilicate glass (Corning 7059) using the device structure shown in Fig. 1. Nickel was used for the gate electrodes since it shows excellent adhesion to the substrate and to the gate dielectric layer. Silicon dioxide was deposited to form the gate dielectric layer. Palladium was used for the source and drain contacts, since its large work function leads to improved carrier injection into the organic material. To form the active TFT layer, pentacene was thermally evaporated in vacuum at a pressure near 10⁻⁵ Pa with a deposition rate near 1 Å/s. During the pentacene deposition, the substrate was held at 60 °C to improve molecular ordering in the pentacene film, which leads to larger carrier mobility and better device characteristics [10].

Molecular ordering also benefits from a smooth substrate. This is illustrated in Fig. 2(a) which shows an atomic force microscopy (AFM) image of a pentacene film deposited onto the smooth surface of an oxidized silicon wafer. The thermally grown silicon dioxide has a peak-to-valley roughness of 8 Å and an RMS roughness of 1 Å, and the deposited pentacene...
Fig. 2. Atomic force microscopy (AFM) images of pentacene films deposited onto (a) thermally grown silicon dioxide, (b) thermally evaporated palladium, (c) ion-beam sputtered palladium, and (d) ion-beam sputtered silicon dioxide. The pentacene layer has an average thickness of 400 Å.

The film shows good molecular ordering with large, micron-sized grains. For comparison, Fig. 2(b) shows an AFM image of a pentacene film deposited onto the significantly rougher surface of evaporated palladium. The evaporated palladium film has a peak-to-valley roughness of 48 Å and an RMS roughness of 5.4 Å, and the deposited pentacene film shows very little ordering.

To obtain a smooth gate dielectric and smooth source/drain contacts for our pentacene TFT’s, the nickel gate electrodes, the silicon dioxide gate dielectric layer, and the palladium source/drain contacts were all prepared by ion-beam sputtering. We have found that ion-beam sputtered palladium and silicon dioxide films have exceptionally smooth surfaces, leading to improved molecular ordering in the deposited pentacene layer. Fig. 2(c) shows an AFM image of pentacene deposited onto ion-beam sputtered palladium. The ion-beam sputtered palladium has a peak-to-valley roughness of 11 Å and an RMS roughness of 1.3 Å, and the deposited pentacene film appears well ordered, with terraced, micron-sized grains. Ion-beam deposited SiO₂ films are quite smooth as well, with a peak-to-valley roughness of 20 Å and an RMS roughness of 2 Å. Fig. 2(d) shows that when pentacene is deposited onto the smooth surface of our ion-beam sputtered SiO₂ gate dielectric layer, an active TFT layer with excellent molecular ordering is obtained.

Silicon dioxide gate dielectric layers were prepared in an Oxford ion-beam deposition system by sputtering from a single-crystal silicon target in a partial pressure of oxygen. Prior to each deposition, the vacuum chamber was evacuated to a background pressure below 10⁻⁴ Pa. The process pressure
was 0.1 Pa, with an oxygen partial pressure of 0.075 Pa and an argon partial pressure of 0.025 Pa. To reduce the mechanical film stress often observed in sputtered dielectric films, substrates were held at a temperature of 80 °C during deposition. The properties of the deposited oxide films were evaluated by ellipsometry, atomic force microscopy, capacitance–voltage \((C–V)\) measurements, current–voltage \((I–V)\) measurements, and thermally assisted gate bias stress.

Using ellipsometry, a refractive index near 1.4 was measured for ion-beam deposited SiO\(_2\) films, similar to the refractive index of thermally grown silicon dioxide. To evaluate the electrical properties of our ion-beam deposited silicon dioxide films, MOS capacitors were fabricated by sputtering SiO\(_2\) onto lightly-doped single-crystal silicon substrates and evaporating aluminum contacts through a shadow mask. Prior to the dielectric deposition, the silicon substrates underwent a standard cleaning procedure using NH\(_4\)OH : H\(_2\)O : H\(_2\)O, HCl : H\(_2\)O : H\(_2\)O, and HF : H\(_2\)O solutions.

Fig. 3 shows the high-frequency (100 kHz) \(C–V\) characteristics of a 630 Å thick ion-beam deposited SiO\(_2\) film on single-crystal silicon. The graph indicates that the flatband voltage shifts by about 6 V upon thermal treatment at 150 °C without gate bias stress. When the capacitor is stressed at 5 MV/cm and 150 °C for several hours, the flatband voltage shifts by about 6 V with a positive gate potential, and by about 2 V with a negative gate potential. Thus, the total flatband voltage shift during thermally assisted gate bias stress is 8 V, indicating an oxide charge density of \(3 \times 10^{12} \text{ cm}^{-2}\). Although this is two or three orders of magnitude larger compared with high-quality thermally grown silicon dioxide, the charge density is sufficiently low for the purpose of fabricating organic TFT’s. The properties of the deposited oxide films can be further improved by annealing at elevated temperature. Fig. 4 shows how the inversion characteristics measured at low frequency (10 kHz) under strong illumination improve after a 30 min/500 °C anneal in forming gas.

Ion-beam deposited SiO\(_2\) films also have large electrical resistivity near \(2 \times 10^{13} \Omega\)-cm. Dielectric breakdown occurs when the electric field exceeds 8 MV/cm, somewhat lower than the breakdown field of thermally grown silicon dioxide films.

Among the challenges in fabricating organic TFT’s based on small-molecule materials like pentacene is patterning of the organic active layer. Even though these materials are often not attacked in a bulk sense when exposed to the solvents commonly used in photolithographic processes, their electrical characteristics tend to degrade significantly. If the active TFT layer cannot be patterned, current leakage between circuit or display elements can be a significant problem, unless the threshold voltage can be controlled so that the active layer is normally nonconducting.

Although pentacene is an excellent insulator, with resistivity around \(10^{14} \Omega\)-cm, evaporated pentacene films have a tendency to form a carrier accumulation channel at the substrate interface, and a positive gate voltage is often necessary to deplete the channel. As a result, current leakage through an unpatterened active layer can be significant [11]. To reduce the leakage between individual TFT’s, we have employed a Corbino transistor layout where the source electrode forms a closed ring around the active TFT area, with the drain electrode located in the center. For a discrete device this allows a patterned gate to control the entire current path from source to drain electrode. Fig. 5 shows a photograph and the schematic layout of a Corbino-type pentacene TFT with a gate length of 5 \(\mu\)m and a gate width of 500 \(\mu\)m.

### III. DEVICE CHARACTERISTICS

Figs. 6 and 7 show the electrical characteristics of a Corbino-type pentacene TFT with a gate length of 60 \(\mu\)m, a gate width of 600 \(\mu\)m, and a gate dielectric thickness of 1600 Å. The saturation field-effect mobility of this device is 0.6 cm\(^2\)/V-s, to our knowledge the largest carrier mobility reported for organic transistors fabricated on a substrate other than single-crystal silicon. The on/off current ratio for this device is \(10^6\), and the off-current is near the noise level of the test setup used, indicating low leakage due to the Corbino layout of the device. Devices with an open electrode
Fig. 5. Photograph and schematic layout of a Corbino-type pentacene TFT with a gate length of 5 μm and a gate width of 500 μm.

Fig. 6. Electrical output characteristics of a Corbino-type pentacene TFT with a gate length of 60 μm, a gate width of 600 μm, and a gate dielectric thickness of 1600 Å.

Fig. 7. Electrical transfer characteristics of a Corbino-type pentacene TFT with a gate length of 60 μm, a gate width of 600 μm, and a gate dielectric thickness of 1600 Å.

Fig. 8. Electrical transfer characteristics of a Corbino-type pentacene TFT with a gate length of 10 μm, a gate width of 1000 μm, and a gate dielectric thickness of 1600 Å.

Low power consumption is an essential prerequisite for many potential organic TFT applications, and devices with near-zero threshold voltage and low subthreshold slope are desirable. The device shown in Figs. 6 and 7 shows excellent turn-on characteristics with a threshold voltage of ~4 V and a subthreshold slope of 1.0 volt/dec. Unfortunately, we are thus far unable to reliably control these characteristics. For example, Fig. 8 shows the electrical transfer characteristics of a pentacene TFT fabricated under similar conditions as the device in Figs. 6 and 7, but using a different pentacene deposition run. The device in Fig. 8 has a gate length of 10 μm, a gate width of 1000 μm, and a gate dielectric thickness of 1600 Å. The subthreshold slope is 0.7 V/dec, to our knowledge the lowest subthreshold slope for organic TFT’s fabricated on a nonsingle-crystal substrate, and close to the lowest subthreshold slope reported for any organic TFT [12], [13]. In addition, the device has an on/off current ratio...
near $10^8$. However, the threshold voltage is +40 V, and the carrier field-effect mobility is only 0.2 cm$^2$/V·s.

For organic TFT’s to be useful for all-organic, active-matrix emissive flat panel displays, they must be able to drive fairly large currents in order to produce bright emission from organic light-emitting diodes (LED’s). Fig. 9 shows that even modest-sized pentacene TFT’s can drive several milliamperes of drain current. This device has a gate length of 10 $\mu$m, a gate width of 1000 $\mu$m, and a gate dielectric thickness of 1600 Å (not the same device as the one shown in Fig. 8). The transistor has a footprint area of about $10^{-3}$ cm$^2$ and produces a drain current of 50 $\mu$A (0.05 $\mu$A/$\mu$m) at about 20 V, 1 mA (1 $\mu$A/$\mu$m) at about 50 V, and close to 3 mA (3 $\mu$A/$\mu$m) at 100 V. These currents are substantially larger than those required to drive an organic LED pixel. For a typical organic LED with a pixel area of about 10$^{-4}$ cm$^2$, a brightness of about 10$^2$ cd/m$^2$, and an external efficiency near 1%, the expected drive current is on the order of 10 $\mu$A [14], [15]. Even using the large layout rules of the transistor in Fig. 9 this would require only about $10^{-6}$ cm$^2$ footprint area (0.1% of the pixel area) for an organic TFT operated at 50 V, or about $10^{-4}$ cm$^2$ footprint area (10% of the pixel area) for an organic TFT operated at 20 V.

IV. CONCLUSION

We have demonstrated organic TFT’s on glass substrates using the small-molecule hydrocarbon pentacene as the active material and low-temperature ion-beam deposited silicon dioxide as the gate dielectric. TFT’s with excellent electrical characteristics were obtained, including carrier field-effect mobility of 0.6 cm$^2$/V·s, on/off current ratio near $10^8$, sub-threshold slope as low as 0.7 V/dec, and drain currents of several microamps per micron. These results increase the likelihood that organic TFT’s will find application in low-cost, large-area electronic and optoelectronic applications.

REFERENCES


Jonathan A. Nichols received the B.A. degree in physics from Edinboro University, Edinboro, PA, and the B.S. degree in materials science and engineering from the Pennsylvania State University, University Park, in 1998, where he is currently pursuing the M.S. degree in materials engineering at the Center for Thin Film Devices. His research focuses on the processing and material characterization of organic thin-film transistors.

Thomas N. Jackson (S'75–M'80) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1975, 1976, and 1980, respectively.

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