

Localization of Gate Bias Induced Threshold Voltage Degradation in a-Si:H TFTs

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Abstract—This letter describes a method to identify the channel region of hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) in which threshold voltage (V_{th}) degradation occurs. The TFTs are subjected to gate bias stress under different operating conditions. Asymmetry in the measured TFT drain current in the forward direction (same source and drain during stress and measurement) and reverse direction (interchanging the source and drain terminals) shows localization of the gate-voltage dependent V_{th} shift mechanism. Based on the observations, a charge-based expression for V_{th} shift is derived.

Index Terms—Amorphous silicon thin film transistors (a-Si:H TFTs), circuit simulation, display technology, spice, threshold voltage degradation.

I. INTRODUCTION

AMORPHOUS silicon thin film transistors (a-Si:H TFTs) suffer from prolonged gate bias stress V_{th} shift (ΔV_{th}). In general, two mechanisms are considered responsible for V_{th} instability in a-Si:H TFTs [1]: First, charge injection into the gate dielectric increases the fixed charge in the silicon nitride (a-SiN_x) layer. Second, dangling bond defect states are created in the a-Si:H channel region. The defect states in a-Si:H TFTs are located within the gate insulator (a-SiN_x layer), at the silicon/insulator interface or within the aSi:H conducting channel [2], [3]. Generally, when modeling ΔV_{th} , these are lumped together and the net V_{th} shift is expressed as

$$\Delta V_{th} = \frac{\Delta V_{th}^e - \Delta V_{th}^h}{2} = q \cdot \frac{\Delta N_D}{C_{ox}}. \quad (1)$$

Here, ΔN_D is the density of created defect states, ΔV_{th}^e is the threshold voltage shift from electrons, ΔV_{th}^h is the threshold voltage shift from holes, C_{ox} is the gate capacitance and q is the electronic charge. This letter describes the experiment

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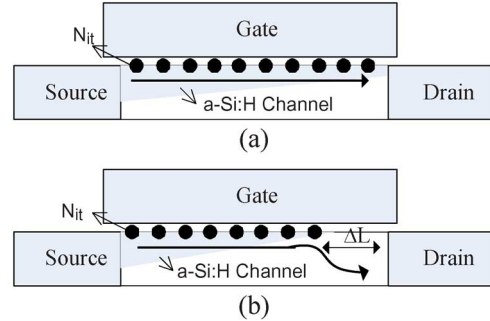


Fig. 1. Schematic representation of the stress conditions and degradation localization. N_{it} is the density of interface defect states (dots) formation is limited to the extent of current flow (solid line) at the surface (a) and (b). (a) Linear mode stress affects channel length L . (b) Saturation mode stress extent limited to $L - \Delta L$.

with which the threshold voltage shift ΔV_{th} is shown to be constrained to the a-Si:H to SiN_x gate dielectric interface and to vary with bias conditions during both stress and measurement. The a-Si:H TFTs are subjected to varying gate bias stress and the current–voltage characteristics are measured under different operating conditions, e.g., in linear and saturation. Specifically, by controlling the transistor operating region, e.g., linear or saturation, and interchanging the source and drain after stress, a different apparent ΔV_{th} is measured.

II. EXPERIMENT

It is well known in bulk-silicon MOSFETs that hot-electron degradation occurs only at the drain where hot electrons are injected [4], [5]. When bulk MOSFETs are biased with the same drain and source (the “forward” configuration) as during hot-electron stress, the linear mode current is strongly affected, but I_{DSAT} is not [6]. When the source and drain are reversed (“reverse” configuration) the MOSFET I_{DS} is degraded for all V_{DS} . Consequently, reversing the source and drain during measurement indicates the location of the hot-electron degradation mechanism—as carriers are forced away from the Si-SiO₂ interface in saturation, the trapped oxide charge at the drain has no effect. At the MOSFET source the impact is maximized.

Here, the same experiment is applied to a-Si:H TFTs to determine if the gate voltage induced ΔV_{th} mechanism is similarly localized in the channel. The concept behind this experiment is illustrated in Fig. 1, with the interface defects

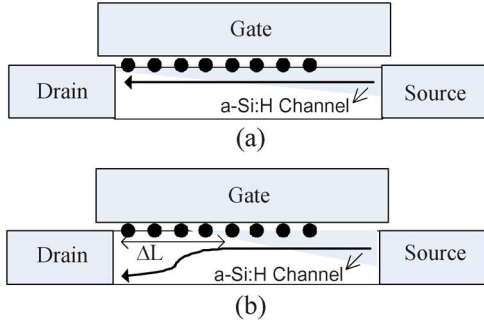


Fig. 2. With source and drain interchanged (reverse measurement) after saturation mode stress, the current flow (solid line) is predominantly below the surface (a), the effect of interface defect states is reduced, producing an increased I_{DSAT} as V_{DS} increases (b). (a) Reverse linear I_{DS} sees all of V_{th} . (b) Reverse saturation I_{DS} increases with V_{DS} screening the damage at pinch-off ($L - \Delta L$).

between the a-Si:H channel and SiN_x gate are represented by the black dots. When the TFT is exposed to a gate voltage at low V_{DS} (linear mode stress) in the forward configuration, the ΔV_{th} mechanism is distributed throughout the channel extent [Fig. 1(a)], resulting in maximum V_{th} degradation. Whereas when exposed to the same gate voltage at a higher V_{DS} (saturation mode stress), the ΔV_{th} mechanism is limited to $L - \Delta L$ [Fig. 1(b)]. The mobile carriers (current flow) responsible for the a-Si:H bond-breaking, which results in V_{th} degradation, occurs at the surface until the pinch off point. This results in a limited extent to the degradation during saturation mode stress. This point is modulated toward the source during saturation mode stress as V_{DS} increases, and the stress induced traps are localized toward the source. Therefore, drain current in the saturation operating region after applying a saturation mode stress should show less ΔV_{th} (higher I_{DS}) when measurement is made in the reversed configuration [Fig. 2(b)]. The TFT in the linear operating region (after saturation mode stress), sees the whole extent of the damage ($L - \Delta L$) in the forward and reverse configurations [Fig. 2(a)]. Hence, reversing the source and drain maximizes current flow in the unaffected region. Since the TFT in the linear mode results in increased interface defects distributed throughout the extent of the channel (L), drain current measured in the linear or saturation operating conditions is significantly reduced. Reversing the source and drain (after linear mode stress) has no effect and reverse I_{DS} tracks the drain current behavior from the forward configuration [Fig. 1(a)].

The next section validates this proposed theory through measured data obtained by stressing the a-Si:H TFTs and measuring in both configurations. The a-Si:H TFTs used in this experiment are fabricated with a low temperature, 175 °C process compatible with flexible transparent substrates. The TFTs have an inverted staggered structure, a molybdenum gate and silicon nitride gate dielectric. The a-Si:H TFTs were subjected to a gate bias stress of 20 V with $V_{DS} = 0$ V (linear mode stress) and $V_{DS} = 20$ V (saturation mode stress) at logarithmically spaced time intervals of 10, 20, 50, 100, 1000, 2000, 5000, 10000 and 20000 s. During each stress interval the I_{DS} - V_{DS} characteristics were measured in the forward and reverse configurations. V_{DS} was varied from 0 to 20 V with $V_{GS} = 20$ V.

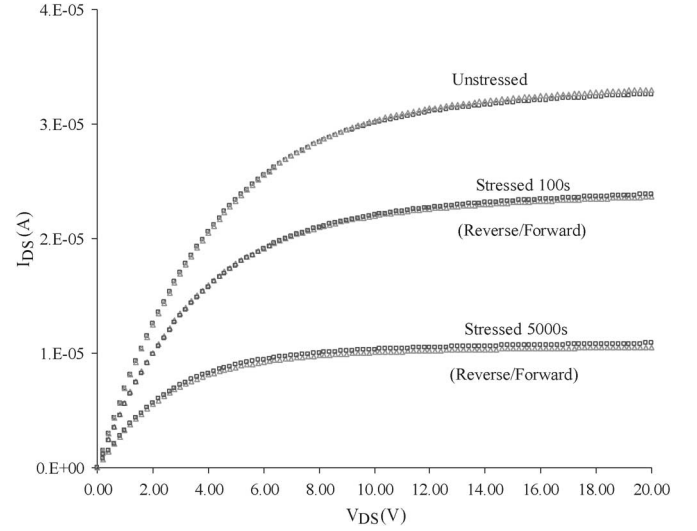


Fig. 3. I_{DS} - V_{DS} characteristics and the change in I_{DS} of a-Si:H TFT pre- and poststress with $V_{GS} = 20$ V and $V_{DS} = 0$ V (linear mode), measured in the forward and reverse configurations. Linear mode stress results in almost identical I_{DS} - V_{DS} characteristics with a constant slope ($\Delta V_{DS}/\Delta I_{DS}$) in the saturation region for both forward and reverse configurations.

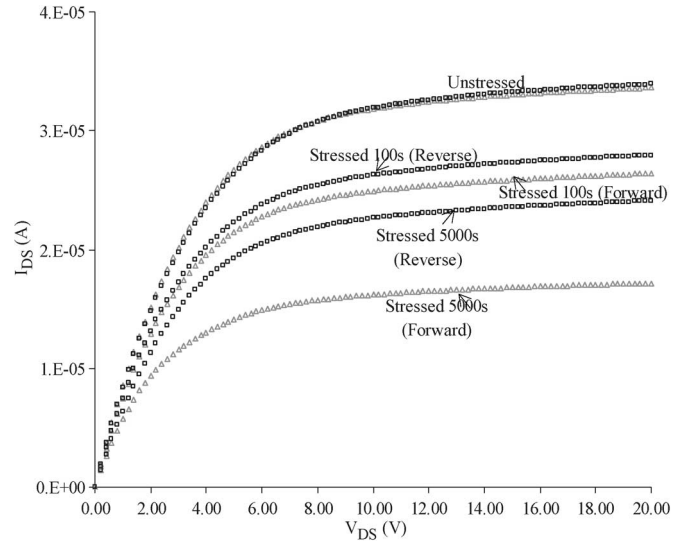


Fig. 4. I_{DS} - V_{DS} characteristics of a-Si:H TFT and the change in I_{DS} pre and poststress with $V_{GS} = 20$ V and $V_{DS} = 20$ V (saturation mode), measured in the forward and reverse configurations. Saturation mode stress results in higher I_{DS} in reverse configurations depicting less V_{th} degradation at the source end of the channel.

A Keithley 4200 C parametric analyzer was used for all measurements. The unstressed a-Si:H TFTs used have $V_{th} = 3$ V and a large subthreshold slope = 0.5 V/decade, which results in a low $V_{DS,sat}$ [7].

III. OBSERVATION

The I_{DS} , versus V_{DS} in both pre- and poststress conditions, comprise Figs. 3 and 4. Referring to Fig. 3, the linear mode stress with $V_{GS} = 20$ V and $V_{DS} = 0$ results in essentially identical I_{DS} - V_{DS} characteristics for the poststress case in both forward and reverse configuration measurements. I_{DS} degradation

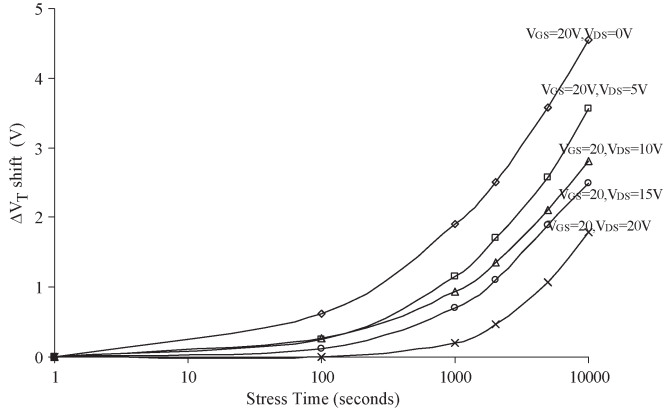


Fig. 5. ΔV_{th} versus stress time of a $108 \mu\text{m}/9 \mu\text{m}$ n-channel TFT stressed with $V_{GS} = 20 \text{ V}$ and $V_{DS} = 0, 5, 10, 15$ and 20 V , respectively.

is greater when the transistor is stressed in linear mode as expected (Fig. 3). The saturation mode stress ($V_{GS} = 20 \text{ V}$ and $V_{DS} = 20 \text{ V}$) shows less I_{DS} degradation when V_{DS} increases in the reverse configuration as theorized (see Fig. 4). Assuming that all defect states (N_{it}) created at the silicon/insulator interface are charged, the percentage degradation of linear drain current ($I_{DS,lin}$) (after a saturation mode stress) is expressed as

$$\frac{\Delta I_D}{I_{D,lin}} = K \cdot \frac{L - \Delta L}{L} \cdot N_{it} \quad (2)$$

where K is a constant related to the effective vertical electric field. Hence, (2) clearly shows that degradation reduces as V_{DS} increases and biases the TFTs further into saturation. The effect is mild, since the transistors have long channels and the $\Delta L/L$ in saturation is not a large value. Higher V_{DS} moves the pinch off point toward the transistor source and produces a decrease in excess carriers, affecting ΔV_{th} (refer to Fig. 5) and consistent with previously reported results [8]. Consequently, the reverse drain-source conductance ($g_{DS} = \Delta I_{DS,sat}/\Delta V_{DS}$) computed from the I_{DS} - V_{DS} characteristics (Fig. 4) shows a 20% increase, indicating weaker saturation.

The measurements indicate that V_{th} degradation is localized at the gate to a-Si:H channel interface region and further, that the mechanism is localized in the channel. Carrier flow is at the surface until the pinch off point. Consequently, essentially normal poststress saturation current magnitude is observed for all V_{DS} in the forward direction. Reversing the source and drain maximizes current flow in the unaffected region and allows the pinch-off point to sweep across traps that create the V_{th} degradation. The source to channel barrier appears unaffected by the ΔV_{th} mechanism since the drain current in the linear operating region after the linear mode or saturation mode stress is less affected in reverse measurement configuration (refer linear region of Figs. 3 and 4). Based

on these observations, the expression of V_{th} shift from (1) is modified as

$$\Delta V_{th} = q \cdot \frac{\Delta \bar{N}_{it}}{C_{ox}}, \quad \text{where } \Delta \bar{N}_{it} = \frac{1}{L} \int_0^{L-\Delta L} \Delta N_{it}(y) \cdot dy. \quad (3)$$

Here, ΔN_{it} is the change in the density of defect states in the silicon/insulator interface and $L - \Delta L$ is the effective channel length.

IV. CONCLUSION

Gate voltage stress measurements of low fabrication temperature a-Si:H TFTs indicate that V_{th} degradation is localized at the SiN_x gate a-Si:H channel interface. The measurements in forward (as stressed) and reverse (source and drain interchanged from the stress condition) also demonstrate that reduced ΔV_{th} occurs at the drain end, where electric fields drive the carriers away from the surface after the channel “pinch-off” point. As the device is biased further into saturation, defect creation occurs over a smaller area, which is always at the source side of the pinch-off point. These measurements are consistent with the ΔV_{th} mechanism requiring carriers at the interface, as suggested in [9].

Differing forward and reverse configuration currents are manifested in better poststress performance of a-Si:H TFT circuits with bidirectional current flow such as pass-transistors. However, the effect is less important than the operating mode of the transistor, i.e., linear or saturation, during gate voltage stress.

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