Enhancement of TFT Performance by Low Temperature Oxygen Annealing

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Abstract

An improvement in the electrical characteristics of TFT’s is evident when the active silicon layer is given a low temperature oxygen anneal prior to the deposition of the gate dielectric. The devices were fabricated using a self-aligned polysilicon gate process on Corning 1737 glass substrates and the maximum processing temperature was 620°C. The TFT’s exhibit an increase in carrier mobility, from 24.1 cm²/Vsec to 31.6 cm²/Vsec, and a reduction in threshold voltage from 12.7 V to 9.2 V after a 50 hour anneal.

1. Introduction

Polysilicon Thin Film Transistors (TFT’s) have vast potential in a wide range of applications including, flat panel displays, large area electronics and 3D integrated circuits [1-3]. The high field effect mobilities of polysilicon TFT’s compared with conventional amorphous silicon devices make them more suitable for driver and signal conditioning circuitry on the periphery of the display panel [4]. The quality of the active polysilicon layer prior to gate dielectric deposition plays an important role in the resulting TFT performance. The deposition technique and the crystallisation method determine the structure and the grain size of the active silicon layer. Laser recrystallisation methods can provide layers with high mobilities and excellent electrical characteristics, although this process is costly and suffers from a low throughput [5]. A more recent method of “touch” polishing the active layer is also proving useful at improving device performance [6]. In this case any inherent roughness in the layer after deposition is reduced by the polishing pad. Other methods which have been investigated include a CF₄ plasma clean of the substrate, prior to the deposition of the polysilicon layer and this resulted in larger grain sizes of the film [7]. This paper discusses the effect of a low temperature oxygen anneal of the active silicon layer prior to the dielectric deposition and the subsequent effect upon TFT device performance.
2. Experimental Procedure
A low temperature process for the fabrication of self-aligned n-channel TFT’s on Corning 1737 glass substrates has been developed. A cross-section of a device fabricated by this process is shown in Figure 1.

Prior to the device fabrication process, the glass is annealed at the maximum process temperature of 620°C to achieve a compaction rate of <0.5µm/hour. A diffusion barrier is deposited on the glass substrate, which is a combination of a PECVD silicon nitride film and an APCVD silicon dioxide layer. This prevents any impurities from the glass substrate from reaching the active silicon layer. The formation of the active polysilicon is by solid phase crystallisation of a previously deposited amorphous silicon layer by a low temperature anneal at 590°C for 72 hours. The thickness of this layer is approximately 0.2µm. The grain size of these layers, determined by Atomic Force Microscopy, was found to be 0.15µm±5%. Prior to dielectric deposition the active polysilicon layer receives an anneal at 600°C in an oxygen ambient with flowrate of 3slm. For the purposes of this investigation wafers A, B and C were given an oxygen anneal treatments for durations of 0, 1 and 50 hours respectively. This anneal results in the growth of a thin high quality silicon dioxide film improving the active layer-gate dielectric interface. The thickness of the dielectric was increased to 100nm by deposition of a silicon dioxide layer in an APCVD reactor at 440°C. This layer is subsequently densified in a nitrogen ambient for 15 hours at 600°C. A deposited polysilicon layer is used as the gate electrode to the device and the gate, source and drain are doped by ion implantation. An APCVD silicon dioxide layer is used to passivate the device. The devices are completed by opening contacts in the passivation layer and forming contacts to the device by sputtering aluminium. Finally the devices receive a N₂/H₂ sintering anneal at 450°C. This process does not use a hydrogenation step.

3. Results and Discussion
Figure 2 shows the transfer characteristics ($I_{ds}$ vs $V_{gs}$; $V_{ds}=15V$) for n-channel TFT’s with $W/L=100\mu m/20\mu m$ for three different oxygen anneals: A) no anneal, B) 1 hour anneal and C) 50 hour anneal. After a one hour anneal in oxygen a slight increase in carrier mobility and reduction in threshold voltage is observed. However, when the oxygen anneal time is increased to 50 hours there is a significant improvement in mobility, from $24.1\text{cm}^2/V\text{sec}$ to $31.6\text{cm}^2/V\text{sec}$, and threshold voltage from $12.7\text{V}$ to $9.2\text{V}$. A reduction in the sub-threshold slope was also found after the oxygen anneal. The improvement in the measured device parameters is due to the growth of a high quality thin silicon dioxide film during the oxygen anneal. The thickness of the silicon dioxide layer grown on a single crystal test wafer in a 50 hour 600°C oxygen anneal was measured by a Nanometrics 210UV to be approximately 12nm. The measured electrical characteristics of the devices fabricated in the process described above are summarised in Table 1.

<table>
<thead>
<tr>
<th>Wafer ID</th>
<th>O$_2$ Anneal (hours)</th>
<th>Mobility (cm$^2$/Vsec)</th>
<th>Threshold Voltage (V)</th>
<th>Sub-threshold slope (V/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>24.1</td>
<td>12.7</td>
<td>1.84</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>28.1</td>
<td>11.75</td>
<td>1.7</td>
</tr>
<tr>
<td>C</td>
<td>50</td>
<td>31.6</td>
<td>9.2</td>
<td>1.3</td>
</tr>
</tbody>
</table>

Table 1: The effect of Oxygen anneal on TFT Performance

4. Conclusions
It has been shown that an improvement in TFT performance can be achieved by annealing the active silicon layer in an oxygen ambient prior to deposition of the gate dielectric. This anneal results in the growth of a thin high quality SiO$_2$ film improving the interface between the active silicon layer and the dielectric. The carrier mobility increased from 24.1cm$^2$/Vsec to 31.6cm$^2$/Vsec, and threshold voltage was reduced from 12.7V to 9.2V after a 50 hour oxygen anneal.

5. References


