CMOS Fabricated Micromechanical Structures

Polysilicon microstructures
  - microbridges

Oxide microstructures
  - pyramidal pits
  - microbridge
  - cantilever beam
  - membrane
Polysilicon Microbridge (I)

Fabrication process:

1. SiO$_2$ layer is initially deposited on a silicon substrate and pattern lithographically. This sacrificial oxide layer and its thickness determines the spacing of the microbridge from the substrate.

2. Polysilicon (microbridge material) of the required thickness is then deposited and patterned.

3. CVD-1 oxide is used to define the contact area between polysilicon and metal.

4. Metal and CVD-2 oxide are deposited and patterned. CVD-2 oxide serves as a protection for the metal layer.

5. Isotropic etching of oxide is performed to released the polysilicon microbridge.

- **Steps 1-4 are standard CMOS processes.**
  The on-chip IC circuits can be integrated with polysilicon microbridge structures.

- **Step 5 isotropic etching is a post processing to form the polysilicon microbridge.**
  The circuits can be protected from etchant by PR.

Drawbacks of the 1st Polysilicon Micro Bridge

- The thickness of the polysilicon is limited by the polysilicon process given in the CMOS sequence.

- The spacing between the microbridge and the substrate is given by the thickness of the field oxide.

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Fig. 5. Polysilicon microbridge fabrication.
**Polysilicon Microbridge (II)**

**Fabrication process:**

1. Two active areas are defined and field oxidation SiO$_2$ is formed by thermal oxidation on a silicon substrate outside the active areas.

2. Polysilicon (microbridge material) strip is placed across these two active areas.

3. A thin gate oxide is beneath the polysilicon in the active areas with a thick field oxide beneath elsewhere.

4. Following the standard CMOS processing sequence, layers of CVD-1 oxide, metal and passivation (CVD-2 oxide) is processed to after the deposition of polysilicon.

5. CVD-1 and CVD-2 oxides can be removed during the CMOS processes by placing CCP, CCA, Via, or COG above the location of polysilicon microbridge.

6. The contact openings must be oversized to permit the isotropic etchant of oxide to removed the field oxides underneath of the polysilicon microbridge.
* Thermal SiO$_2$: BOE (buffered oxide etches) 49%HF + NH$_4$F + H$_2$O

* Vapox (vapor deposited oxide): CVD SiO$_2$ passivation film usually deposited over the aluminum metallization pattern. Since BOE attacks the aluminum, the prefer etchant for this layer is acetic acid (CH$_3$COOH) and ammonium fluoride (NH$_4$F) => Selectivity
Apertures on Polysilicon Bridge

Apertures (etching holes) is designed to reduce the etching time of a larger polysilicon bridge.
Oxide Masks for Pyramidal Pits

KOH or EDP anisotropic etching of (100)-wafers

- (100)-oriented silicon wafers are normally used in CMOS.
- In order to form a pyramidal pit in (100) silicon, a square opening has to be made in the oxide mask.
- The sides of the oxide mask opening has to be either parallel or perpendicular to the (110) edge of the silicon crystal.
Effect of Misalignment on \{100\} Substrate

If the silicon is etched long enough, any arbitrary shape will result in a rectangular pit in the silicon and the arbitrary shape is perfectly inscribed in the rectangle.
Possible Combinations of Oxide Microstructure by CMOS Processing

- field oxide and two CVD oxides films
- field oxide and CVD oxides sandwiching a polysilicon
- field oxide and CVD oxides sandwiching a aluminum metal
Oxide Microbridge

- Active area (CAA), Contact to Active (CCA), Vias (CVA) and Overglass (COG) are placed one above the other in the areas where the silicon substrate has to be exposed.

- The diagonal oxide layer defined by the layout can not aligned to the (110) edge of the silicon wafer. This will ensure the anisotropic etchant to undercut the diagonal oxide layer to the form the microbridge.
Oxide Cantilever Beam

The undercut effect is exploited to make oxide cantilever beams.
Oxide Membrane Structures
XeF₂ Etch for Post-Processing CMOS

- **Xenon Diflouride Etching:**
XeF₂ is a non-plasma, isotropic dry etch process for silicon.

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2\text{XeF}_2 + \text{Si} \rightarrow 2\text{Xe} + \text{SiF}_4
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- Xenon Difluoride provides very high selectivitiy for alluminum, silicon dioxide, silicon nitride and photoresist. These properties makes it an extremely useful etchant for postprocessing CMOIS integrate circuits.
- Typical etching rates 1~ 3 µm/min.
- The etched surfaces produced are rough. (granular structure 10µm and smaller).
- Exthermic reaction which may affect some structures (1 W/cm² of etch area).
CMOS Electrothermal Microactuator

(a) Device Well Contact-Cut Via-Cut and Pad-Opening

(b) Sandswiched Polysilicon Heater Element

DEFLECTION (µm)

INPUT POWER (mW)

Plastic

Elastic

DEFLECTION (µm)

FREQUENCY (Hz)

Oscillating region