Chapter 9. Device Fabrication

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9.2 The silicon process

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9.4 Device assembly
9.1 Introduction

• Three layers are bonded together to form a robust sandwich structure by adhesive layer, fusion bonding or anodic bonding.

• An adhesive layer can be used to glue the two parts together, however, because the gap between the mass and the encapsulation is very small, the glue layer thickness and the variation therein are relatively large, making this method not very suitable.

• Silicon fusion bonding is used to bond two silicon wafers by increasing the temperature up to 1100°C. Because the aluminum interconnection is only able to withstand temperatures up to 450°C. This method is not suitable when using electronic circuits on the same chip.

• Anodic bonding bonds the silicon and glass wafer by applying high voltage across the wafers at 200-300°C. This technique is fully fabrication compatible with the standard bipolar process.
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9.2 The silicon process

- Standard double-side polished 4” p-type (100)-oriented silicon wafers.
- The following steps are part of bipolar silicon process:
  (a) Grow 4μm thick n-type epi-layer => beam suspension and bipolar electronic circuits.
  For isolation of the micro-electronic device, a P⁺ Deep P (DP) diffusion is included. This P⁺ region is also used as the contact pads for the center electrode (the whole seismic mass).
  (b) 1200A SiO₂ and a 3000A LPCVD-Si₃N₄ layer is used for masking the wafer during KOH etching. To prevent this layer from being damaged during subsequent processing steps, it is covered with a 2000A thick low-stress LPCVD poly-Si.
  (c) On the front of the wafer, SiO₂ is removed, P⁺ (WP) diffusion is implemented to generate the single-plate center electrode and SiO₂ is deposited again.
  (d) Contact holes are opened and a 6000A thick aluminum/silicon layer is deposited for interconnect.
  (e) Extra SiO₂ on the beams is removed to reduce the stress. Patterning and window plasma etching of Si₃N₄/poly-Si/SiO₂ layer at the back of the wafer for KOH-etching.
9.2.1 Anisotropic etching

Anisotropic etching of silicon in KOH

- 33 weight % KOH at 86°C => 1.7 µm/min
- Electrochemically-controlled etch-stop (ECE) technique for membrane thickness control.
9.2.2 Corner Compensation

Fig. 4-4  Convex corner undercutting and the resulting angles $\alpha$ and $\beta$ between the undercutting planes at the surface. Variables 'a' and 'b' denote the direction of the undercutting and need to be determined.

$$\cos \alpha = \frac{r_{l_1} \cdot r_{l_2}}{|r_{l_1}| |r_{l_2}|}, \quad (4-1)$$

where $r_{l_1}$ and $r_{l_2}$ denote the directional vectors of $l_1$ and $l_2$ (ref. to undercut directions $<a \pm b' 0>$ and $<\pm b a 0>$ in Figure 4-4), so that the angles are given:

$$\alpha = \arccos\left(\frac{a^2 - b^2}{a^2 + b^2}\right), \quad \beta = \arccos\left(\frac{2ab}{a^2 + b^2}\right) \quad (4-2)$$
Table 4-1. *angles between the cross-sectional lines of the undercutting planes and the (100)-plane.*

<table>
<thead>
<tr>
<th>undercutting direction</th>
<th>$r_{l_1}, r_{l_2}$</th>
<th>$\alpha$</th>
<th>$\beta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$&lt;210&gt;$</td>
<td>$(\pm 1, \pm 2, 0), (\pm 2, \pm 1, 0)$</td>
<td>143°</td>
<td>53°</td>
</tr>
<tr>
<td>$&lt;310&gt;$</td>
<td>$(\pm 1, \pm 3, 0), (\pm 3, \pm 1, 0)$</td>
<td>126°</td>
<td>37°</td>
</tr>
<tr>
<td>$&lt;410&gt;$</td>
<td>$(\pm 1, \pm 4, 0), (\pm 4, \pm 1, 0)$</td>
<td>152°</td>
<td>62°</td>
</tr>
</tbody>
</table>
Experimental Test

Fig. 4-5  Influence of the undercutting on the convex corner, (a) mask design with desired structure and (b) SEM-photograph of the resulting corner.
Fig. 4-6  SEM-photograph taken directly above the convex corner to measure the angle between the undercutting planes.
(110)-oriented corner compensation structures

Fig. 4-9 Mask layout showing the (110)-oriented corner compensation structures, (a) using beams and (b) using a combination of beams and squares.

Fig. 4-10 Etching of a silicon mass in 33 wt. % aqueous KOH at 86 °C, using (110)-oriented corner compensation beams.

Fig. 4-11 Etching of a silicon mass in 33 wt. % aqueous KOH at 86 °C, using (110)-oriented corner compensation squares.

Fig. 4-12 SEM-photograph showing the convex corner when using (110)-oriented corner compensation structures.
(100)-oriented corner compensation structures

This velocity is related to the etch-rate of the \( \{411\} \)-planes \( \dot{R}/411 \) due to the inclination of this plane with respect to the (001)-plane. The angle between the \( \{411\} \)-plane and the \( \{410\} \)-plane is determined by (ref. Eq. (4-1)):

\[
\varphi = \angle(\{411\}, \{410\}) = \arccos\left(\frac{\sqrt{17}}{18}\right),
\]

so that the cross-sectional line oriented in the \(<410>\)-direction moves with a velocity \( v_{410} = R411/\cos\varphi = R\{411\}\sqrt{17}/18 \).

Due to the angle \( \alpha \) between the \(<410>\)-direction and the \(<100>\)-direction, which is given by \( \alpha = \arccos(4/\sqrt{17}) \), the travel distance of the \( \{411\} \)-plane in the \(<410>\)-direction is given by:

\[
d_1 + d_2 = \frac{B}{2\cos\alpha} + L_1\sin\alpha
\]

so that with \( L = L_1 + L_2 + L_3 \) and \( L_2 = B/2\tan\alpha, L_3 = B/2 \), the following etch time is found, at which the \( \{411\} \)-planes reach the convex corner of the mass:

\[
t_{\{411\}} = \frac{d_1 + d_2}{R\{411\}\sqrt{17}/18} = \frac{(L + 3B/2)}{\sqrt{17}R\{411\}}
\]

The etch time required for the \( \{100\} \)-plane to reach the convex corner is simply given by:

\[
t_{\{100\}} = \frac{B/2}{R\{100\}}
\]

where \( R\{100\} \) denotes the etch-rate of the \( \{100\} \)-planes.

**Beam length \( L \):**

\[
L \geq B \frac{3}{2} \left( \frac{R\{411\}}{R\{100\}} \sqrt{2} - 1 \right)
\]
Fig. 4-15  Realized seismic mass, using the (100)-oriented corner compensation structure.
Fig. 4-16 Etching of (100)-oriented corner compensation structures in aqueous KOH with resulting convex corner.
Membrane Quality

Fig. 4-17 Photograph taken from the bottom of the silicon wafer after etching, showing (a) the ridges on the membrane due to the corner compensation structure and (b) a close-up view of the membrane.
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9.3.1 Anodic bonding

Fig. 4-18 Schematic view of the three-layer sandwich structure.

Fig. 4-19 Schematic view of anodic bonding of glass on silicon

Fig. 4-20 Typical bond curve showing the peak in the current.

Fig. 4-21 Thermal expansion properties of Pyrex #7740 glass and single crystal silicon [4.11].
9.3.2 Press-on contacts

Fig. 4-22 Deformation of the glass during bonding due to the interconnect pattern on the silicon and glass wafer.

Fig. 4-23 Shallow recess in the glass for improved bonding of the silicon-to-glass. In areas where aluminum is present on the silicon as well as on the glass an electrical contact is made.
Resistance of press-on contacts

Fig. 4-24 Test structure for measuring the resistance of the press-on contact.

Fig. 4-25 Measured contact resistance for several sizes of the press-on contact.

From this figure the following contact resistance can be evaluated:

$$R_{\text{press-on}} = \frac{590}{w_{\text{contact}}} \text{ [}\Omega\text{]}.$$  (4-8)
9.3.3 Etching of glass

Etchant: HF or BOE

Mask: Poly-Si or Photoresist

Step coverage:

First, the thicker the aluminum layer, the better the step coverage. However, by increasing the thickness of the aluminum layer, the gap needs to be deeper to maintain the gap between the mass and the encapsulation, because the effective gap is between the mass and the electrode. For this reason, the thickness of the aluminum electrode layer was limited to 0.6 μm, similar to the aluminum thickness on the silicon wafer, so that the required etch-depth is 4.6 μm in order to obtain a gap of 4 μm. Also, sputtered aluminum gives a better step coverage than evaporated aluminum. For this reason, sputtered aluminum was used.

Second, the steeper the slope of the profile, the worse the step coverage of the aluminum across the edge of the recess will be. Therefore, a large undercut ratio is desired, as shown in Figure 4-26 (the undercut ratio is defined as the ratio of the lateral underetching of the mask \( d_{\text{lateral}} \) and the vertical etch-depth \( d_{\text{vertical}} \)).

\[
\text{Undercut ratio} = \frac{d_{\text{lateral}}}{d_{\text{vertical}}}
\]

Fig. 4-26 Influence of the etch-profile on the step coverage of the aluminum. (left) undercut ratio = 1 is bad for the step coverage and (right) undercut ratio > 1 is good for the step coverage.
Push edges:
- the edges facing the center of the wafer.
- The photoresist is pushed against the edges. => thicker

Pull edges:
- The photoresist is pulled away from the edges. => thinner
Polysilicon masking layer

Mask: Poly-Si

A 2000 Å thick LPCVD polysilicon masking layer is deposited at a temperature of 560 °C, with a gas flow of 45 standard cubic centimeter per minute (sccm) SiH₄ at 150 mTorr. After deposition of the Poly-Si layer, this layer is patterned using a 1.2 μm thick photo-resist (HPR 504). Etching is

Etchant: HF

Polysilicon masking layer is not attacked by the HF-solution, so that very deep recesses can be fabricated.

Table 4-2. Etch-rate [μm/min] of Pyrex #7740 glass in HF-solutions for several concentrations and temperatures.

<table>
<thead>
<tr>
<th>Concentration HF in H₂O</th>
<th>Temperature 23 °C</th>
<th>40 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 %</td>
<td>0.5</td>
<td>1.6</td>
</tr>
<tr>
<td>20 %</td>
<td>1.2</td>
<td>3.3</td>
</tr>
<tr>
<td>40 %</td>
<td>4.6</td>
<td>-</td>
</tr>
</tbody>
</table>
Step coverage:

Fig. 4-28 *SEM-photo of the recess edge fabricated with a poly-silicon masking layer using HF as etchant, showing (a) an overview and (b) a close-up of the overhanging tip.*

The edges of the recesses fabricated in this way are very sharp and reveal an overhanging edge, the length of which is approximately 10% of the etch-depth, as shown in the SEM-photo of Figure 4-28. Due to this overhanging edge, the step coverage when using aluminum is very poor. A long HF-dip after removal of the poly-Si mask reduces the overhanging tip-length. However, step coverage still remains poor, because the **undercutting ratio** using this masking layer is approximately 1, thus revealing a sharp corner at the recess edge. Therefore, recesses which require a step coverage of
Wet stripping of polysilicon masking layer:

An additional problem when using poly-Si as masking layer, is that during stripping of the mask, either dry or wet, the recess deepens. When using a wet stripping procedure of the 2000 Å-thick poly-Si mask (in a solution containing HNO₃, HF and H₂O), the increase in depth is approximately 1 μm. Also, the non-uniformity of the recesses is increased. Prior to the stripping of the mask, the non-uniformity of the recess depth over the complete wafer is ±2.0 %, whereas after removal of the poly-Si mask, the non-uniformity is ±2.5 %.
Photoresist masking layer

Mask: photoresist

When using photo-resist as masking layer, the stripping is performed, after the recesses are etched, by using acetone. In that case, the recesses do not deepen, because the glass is not attacked by the acetone.

The main problem when using the photo-resist masking layer, however, is the adhesion of this layer to the Pyrex wafers. Even when using the adhesion promoter HMDS (HexaMethylDiSilazane), the photo-resist layer peels-off in a HF-solution after only 2-3 minutes.

Etchant: BHF

The solution was found in using a Buffered HydroFluoric acid (BHF) solution with a ratio of HF:NH₄F = 1:7 as the etchant. The etch-rate of the Pyrex #7740 glass in this solution was found to be 0.025 μm/min at 21°C, thus requiring an etch-time of 40 minutes to obtain the shallow-recess of depth 1 μm and an etch-time of 185 minutes to obtain the deep-recess of depth 4.6 μm. A 1.2 μm thick HPR 504 layer is used to fabricate the shallow recess and a 2 μm thick HPR 504 layer is used to fabricate the deep recess. The recess depth is mainly limited by the adhesion of the photo-resist to the Pyrex wafer, but a depth of 5 μm is easily obtainable.
Step coverage:

Due to the poor adhesion of the photo-resist, an undercut ratio of 25–30 has been measured, using a Tencor Instruments Alpha-step 200 surface profilometer. Figure 4-30 shows the profile of a shallow recess containing an aluminum lead for the press-on contact and Figure 4-31 shows the measured profile of a deep recess containing an aluminum lead. Due to the large undercut ratio, the step-coverage of the recess edge by the aluminum layer can be very good (ref. Figure 4-26). This was confirmed by an experiment with a 10 μm wide aluminum lead passing a 5 μm deep recess. None of the measured leads failed the conductivity test. The measured non-uniformity over the complete wafer is ±2.0 %, which is less than the non-uniformity when using the poly-Si masking layer.
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After the etch is performed, the bottom encapsulation is anodically bonded to the silicon wafer. After the bonding is performed, the device is heavily damped, due to the small air-gap below the seismic mass. At this point the membrane is RIE-etched (using SF₆) to define the flexible beam suspension. If the membrane is etched prior to bonding, the damping is very poor, because damping in that case is only realized by internal damping of the silicon material and many devices would not survive the subsequent handling steps.
Directions of the Beam (Review)

- Both Young’s modulus and Poisson ratio depend on the directions of crystal.
- \(<110>\)-direction is stiffer than \(<100>\)-direction. Poisson ration in \(<110>\)-direction is much smaller than in the \(<100>\)-direction. Therefore, the influence of the aspect ratio on the correct factor \(\alpha_{wb/lb}\) will be much less.
- \(<110>\)-oriented beams are preferred because they don’t have to be placed at the corners of the seismic mass.

Table 2-1. Mechanical properties of silicon beams

<table>
<thead>
<tr>
<th>direction of beam</th>
<th>E [10^{11} \text{ N m}^{-2}]</th>
<th>v</th>
<th>max. error [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(&lt;100&gt;)-direction</td>
<td>1.300</td>
<td>0.2785</td>
<td>8.4</td>
</tr>
<tr>
<td>(&lt;110&gt;)-direction</td>
<td>1.690</td>
<td>0.0625</td>
<td>0.4</td>
</tr>
</tbody>
</table>

Fig. 2-11 Two commonly-used orientations for beams in accelerometers: \(<110>\)-oriented beams (left) and \(<100>\)-oriented beams (right).
Optimal geometry (Review 2.1.6)

• Because the lateral sensitivity depends on the location of the beams, there is an optimal geometry which suffers the least from lateral accelerations.
• The optimal geometry should be far away from the center of the mass.
• Since the corners of the mass are attacked during etching, the beams are placed at a certain distance from the corner of the seismic mass.
• Therefore, <110>-oriented beams are preferred. There are several possibilities of placing these <110>-oriented beams.

- The smallest cross-axis sensitivity in all directions is obtained by structure III and IV. Since structure III is not symmetric, an acceleration in the x or y-direction will cause the mass to rotate around the z-axis. => Optimal geometry is structure IV.
This process sequence thus ensures a low yield loss due to break-out. Figure 4-32 shows the resulting two-layer structure after the RIE-etch of the membrane. A close-up view of a device is shown in Figure 4-33.
The next step involves the bonding of the top encapsulation to the silicon wafer. In order to contact the bondpads, which are located on the silicon wafer, the top encapsulation is cut-in 200 μm prior to bonding using a dicing saw. The remaining 300 μm is cut after the bond is complete to reveal the bondpads, as shown schematically in Figure 4-34.
Fig. 4-36 Photograph of the completed three-layer sandwich structure.