Progress in epitaxial deposition on low-cost substrates for thin-film crystalline silicon solar cells at IMEC

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Abstract

In recent years, research on epitaxial growth for photovoltaics became more important due to the increasing interest in thin-film silicon solar cells. Two significant challenges need to be resolved before this technique can become a competitive industrial alternative to the current dominating technology of bulk silicon solar cells: (i) the availability of a high-throughput and cost-effective epitaxial CVD reactor and (ii) efficiencies approaching those of bulk Si solar cells.

In this paper, two CVD systems are studied: an AP-CVD commercial reactor, as a reference system, and an experimental LP-CVD system for optimization of a low-cost semi-industrial process. For low growth rates, an LP-CVD process is realized with a defect density around $5 \times 10^{13}$ defects/cm$^2$, comparable with the layers grown in the commercial reactor with a growth rate of 3.9 $\mu$m/min. First solar cells, grown in the LP-CVD reactor show an efficiency of 8.2% on mono-crystalline samples. Cells on various low-cost substrates, grown in the reference reactor, show efficiencies between 12% and 13% with IMEC’s industrial screen-printing process.

The short-circuit current of epitaxial cells is limited to 28 mA/cm$^2$ (typically 5 mA/cm$^2$ less than for bulk Si cells). Therefore, the thin epitaxial cell concept requires optimal light trapping, increasing the optical path length. Experiments show that a porous silicon (PS) intermediate layer as an internal reflector can fulfill this role adequately, giving an internal reflectance up to 80%. However, the effectiveness of this reflector depends on its influence on the quality of the epi-layer. Measurements show a lower-quality epi-layer for samples with a PS intermediate layer, but indicate that further optimization of the pre-deposition bake could lead to a compromise between current gain by internal reflectance and losses caused by the increased defect density.

1. Introduction

Thin-film silicon solar cells grown on low-cost highly doped substrates by high-temperature CVD have a high potential for low production costs because of the reduced quantity of high-purity silicon. Furthermore, epitaxial cells have the same cell structure as conventional bulk solar cells. Therefore, besides the actual epi-deposition, only minor changes need to be made to the current industrial production process and the main effort should be focused on the research on high-throughput and cost-effective epitaxial CVD systems [1,2]. At IMEC, experiments are conducted on an experimental batch-type low-pressure CVD system and a commercial CVD reactor from ASM, serving as a reference system. Even with a high-throughput system, the CVD process will represent the dominating cost component in an epitaxial thin-film solar cell production process. Epitaxial cells can only be competitive when the epi-layer is of good epitaxial quality and limited in thickness. The first requirement is heavily influenced by pre-deposition treatments (Section 2) and growth parameters (Sections 3 and 4) and will be evaluated for both CVD reactors. The second requirement, a limited thickness of the active layer, obliges us to use light trapping mechanisms to enhance the optical thickness of the thin active layer. In Section 5, an internal reflector consisting of porous silicon (PS) layers is introduced to fulfill this role.
2. Pre-deposition treatments

To grow high-quality epitaxial films on low-cost silicon substrates, proper pre-deposition treatment is crucial. First the saw-damage of the low-cost silicon substrates should be removed and afterwards, the roughness of the surface should be minimized, ideally resulting in a mirror-polished substrate. Initially, this polishing was done with a double wet etching process [3]. Recently, IMEC developed a single etching solution to obtain a ‘polished’ low-cost silicon substrate with a surface roughness around 100 nm. The solution consists of an isotropic etching solution based on HF, HNO₃ and acetic acid as a wetting agent with an average etch rate around 1 µm/min for the first 10 min of etching, depending on the doping concentration and the substrate type.

Secondly, a full RCA clean is applied to the wafers to remove all remaining organic and metal contaminations. This step concludes with an HF dip to remove the native oxide. For the final cleaning, necessary for good crystallographic quality of the epitaxial layer, the wafers are heated in situ in ultra pure H₂ at deposition temperature to reduce the native surface oxides and to diffuse other surface impurities to the bulk of the silicon substrate.

3. Results obtained with a commercial single-wafer ASM reactor

Our AP-CVD reactor is a commercial Epsilon2000 single-wafer reactor from ASM, which is used for microelectronics. As a precursor trichlorosilane (TCS) is used diluted with hydrogen (H₂) and diborane (B₂H₆) is added to dope the epitaxial layers to the required doping level of 1 × 10¹⁷ at/cm³. Our reference process is performed at 1130 °C at atmospheric pressure, with a growth rate of 3.9 µm/min. The average defect density (determined with a preferential wet chemical etching based on HF/Cr₂O₇⁻²) of 20-µm thick layers on highly doped mono-crystalline Cz wafers, grown with this reference process, is 5 × 10³ defects/cm². Recent cell results on different types of highly doped low-cost substrates are presented in Table 1. All solar cells are obtained with IMEC’s industrial screen-printing process, mainly consisting of the following steps:

- epitaxial growth of a 20-µm thick active layer with the reference process,
- plasma texturing (removing 1–2 µm of the epi-layer),
- emitter formation by POCl₃ diffusion and removal of the glass,
- SiNx deposition as an anti-reflection coating,
- screen printing of the contacts,
- firing of the contacts through the nitride layer,
- dicing of the edges and tabbing of the busbar.

Efficiencies between 12% and 13% are achieved for large area (10 x 10 cm²) cells on highly doped upgraded metallurgical grade (UMG-Si), off-spec and reclaim substrates. More details about the cell process and the solar cell results can be found in Refs. [4,5].

4. Results obtained with an experimental LP-CVD batch-type reactor

The LP-CVD reactor is an upgraded PEO603 furnace from ATV, illustrated in Fig. 1. The system operates at 1000 °C and pressures around 5 mbar. Silane (SiH₄) is available as precursor gas, B₂H₆ as doping gas, both diluted in H₂. Up to 20 wafers (12.5 cm x 12.5 cm), are placed vertically inside an insert tube, parallel to the gas injector. A more detailed description of the experimental LP-CVD reactor and its processing possibilities can be found in Refs. [6,7]. For growth rates between 20 and 50 nm/min, a defect density of around 5 × 10⁵ defects/cm² is obtained, comparable with the layers grown in the commercial reactor with the reference process. Processes with higher growth rate (up to 150 nm/min), result in a defect density in the order of 1 × 10⁶ defects/cm² (Fig. 2).

Solar cell results obtained on epitaxial layers grown in this system with the screen-printing cell process as described above, are presented in Table 2. The highest efficiency on mono-crystalline silicon is 8.2% for a 20-µm thick epitaxial layer. On UMG multi-crystalline silicon, thin epitaxial layers of 4–5 µm are deposited with a growth rate of 85 nm/min. The corresponding cells reach a maximum Voc of 571 mV, which proves the good quality of the epitaxial layer and indicates the potential for higher current densities if thicker epitaxial layers (20 µm) are grown. It should be mentioned that the solar cells processes were not optimized for the thickness of a 725 µm thick

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Table 1

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Epi-layer (µm)</th>
<th>Size (cm²)</th>
<th>Jsc (mA/cm²)</th>
<th>Voc (mV)</th>
<th>FF (%)</th>
<th>Eff (%)</th>
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<tr>
<td>Off-spec</td>
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<td>605</td>
<td>76.8</td>
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<tr>
<td>Reclalm</td>
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<td>96</td>
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<td>618</td>
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<td>12.8</td>
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<tr>
<td>UMG-Si</td>
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<td>26.4</td>
<td>604</td>
<td>76.6</td>
<td>12.2</td>
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</table>

Fig. 1. Schematic drawing of the batch type LP-CVD reactor.
5. Porous silicon as intermediate layer

Compared with typical short-circuit currents of industrial multi-crystalline solar cells (around 32–34 mA/cm²), the short-circuit current of epitaxial cells is limited to 28 mA/cm². Therefore, the thin epitaxial cell concept requires a certain light-trapping mechanism to increase the optical thickness of the active layer and as a result of that, an increase in the short-circuit current of the cell should be possible.

Experiments show that a PS intermediate stack, sandwiched between the substrate and the epi-layer, with alternating layers of 55% and 22.5% porosity, can act as such an internal reflector. For a stack of 15 layers, an internal reflectance of 80% is achieved [5]. However, to fulfill its role adequately in a solar cell device, not only the optical requirements should be fulfilled, but the surface of the PS stack should also serve as a good template for high-temperature epitaxial growth.

During the H₂-bake before deposition, the columnar structure of the PS layer can rearrange into large voids (Fig. 3), depending on the annealing conditions and the PS stack. At very high temperatures and in a H₂ environment reorganization of the PS layers occurs in such a way that the top surface of the PS layer gets smooth due to the closing of the pores at the surface of the PS layer. This smoothening results in a reduction of the RMS surface roughness by a factor of four [8], which is a desirable effect for the deposition of high-quality epitaxial layers.

Detailed studies have to be made to optimize the best annealing conditions before epitaxial growth and to minimize the defect density of the epitaxial layer. So far, experiments have indicated that the lowest defect densities could be obtained by annealing in pure H₂, at 1130 °C, at atmospheric pressure for 30 min or longer. It is clear that H₂ atmosphere during the bake is crucial, as it is responsible for evaporation of oxides and therefore enhancement of the material transport by changing the activation energy for surface diffusion [9]. Although H₂ environment is an important condition for pore closure at the surface, the limited diffusion length of H₂ makes the rearrangement of the multiple PS layers only possible to a depth of 7 μm (Fig. 4).

To evaluate the influence of the number of layers in the stack on the defect density in the epi-layer, 3 different PS stacks are made with resp. 2, 8 and 15 layers. After annealing in H₂ at 1000 °C for 30 min at reduced pressure and growth of a 5 μm thick epitaxial layer, a small increase in defect density with increasing amount of layers in the PS

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**Table 2**

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Epi-layer (μm)</th>
<th>Size (cm²)</th>
<th>Jsc (mA/cm²)</th>
<th>Voc (mV)</th>
<th>FF (%)</th>
<th>Eff (%)</th>
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<td>Mono-Si</td>
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<td>27.3</td>
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<td>UMG-Si</td>
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<td>571</td>
<td>65</td>
<td>4.26</td>
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</table>

*As a comparison, the solar cells parameters of an epitaxial cell on mono-crystalline silicon, grown in the reference system is given.

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**Fig. 2.** Influence of the growth rate on the defect density in the LP-CVD batch reactor.

**Fig. 3.** (a) Transmission electron microscope (TEM) picture of a PS stack before annealing, (b) scanning electron microscope (SEM) picture of a PS stack after a high-temperature anneal.

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**Fig. 4.** (a) Transmission electron microscope (TEM) picture of a PS stack before annealing, (b) scanning electron microscope (SEM) picture of a PS stack after a high-temperature anneal.
stack can be observed: defect densities of resp. $3.1 \times 10^7$, $3.2 \times 10^7$, $1.8 \times 10^8$ defects/cm$^2$ are measured. Besides the atmosphere, experiments have shown that the temperature in combination with pressure has a large influence on the defect density of the epitaxial layer. When a similar 15-layer stack is annealed at atmospheric pressure for 30 min at 1130°C, the defect density is decreased drastically to values between $10^3$ and $10^4$ defects/cm$^2$. Epitaxial layers with defect densities up to $10^4$ defects/cm$^2$ are suited for solar cell processing and therefore, the concept of a PS stack as an internal reflector for solar cell devices is feasible.

6. Conclusion

Recent progress in epitaxial growth for an experimental batch-type LP-CVD reactor is reported, with a maximum efficiency of 8.2% for a 20μm epitaxial cell on monocrystalline silicon. Furthermore, an overview of the recent results in a commercial CVD reactor demonstrating solar cells with efficiency between 12% and 13%, demonstrate the need for a light-trapping mechanism. It is demonstrated that PS intermediate layers have the potential to fulfill this role when optimal annealing and growth conditions for the epitaxial layer are used. The influences of pressure, annealing gas and temperature, and the amount of PS layers on the defect density of epitaxial layer on top of a PS stacks are discussed. Defect densities lower that $1 \times 10^4$ defects/cm$^2$ can be obtained when annealing is done under atmospheric pressure for 30 min at 1130°C.

Acknowledgements

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References