WIRELESS TRANSMISSION OF POWER AND DATA TO IMPLANTS

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***Abstract* — This paper describes an RF-link system suitable for coupling to an implant. The wireless coupling minimizes the risk of infection and improves the patient health level. Data and power are transmitted by means of an RF low-coupling transformer. Binary FSK modulation is used in the forward link (from outside to implanted prosthesis) and DBPSK is used in the backward link (implanted prosthesis to outside). Experimental results concerning an intracortical prosthesis derived prototype are presented, and important concerns regarding the magnetic coupling and data synchronization are addressed.**

I. INTRODUCTION

Nowadays a great effort is being done in developing neurological stimulators by means of integrated implants. This is particularly relevant in muscular stimulation for limbs or heart diseases [1]-[5] and in cortical stimulation for blind people [6]-[9]. The classic techniques make use of wired links between the unit placed outside the body and that inside the body [6], [9]. However, this technique has a high risk of infection and is considerably uncomfortable for the patient. In order to improve these drawbacks, wireless solutions are presently being under development. Also, in most applications, the need of long time functioning requires the implant to be powered by the outside, in order to avoid unnecessary surgery for batteries replacement. Nevertheless, wireless solutions present many challenges because power and data have to be satisfactorily transmitted to the inside unit, in spite of the significant coupling losses. In what concerns the inside unit power requirements, they depend on many issues, as for instance the electrode stimulation power requirements, the internal control unit, the chosen technology, etc. Usually, for the case of cortical neuroprosthesis, a few miliwatts are sufficient. Also, a duplex transmission is desirable in order to have some information on the inside unit status. In this paper, an RF-link system suitable for coupling to an implant is presented. The general architecture is explained, the main problems found in the wireless coupling are discussed and experimental results concerning an intracortical prosthesis derived prototype are presented. The system uses binary FSK for the forward link (from outside to inside body) and DBPSK for the backward link (inside to outside body, for maintenance purposes). The wireless connection is accomplished by means of a low magnetic coupling transformer.

In Section II the overall system architecture is presented. In Section III the outside unit is presented and explained. In Section IV the coupling transformer along with the coupling main problems are addressed. In Section V the inside body unit is presented, including the clock, data and power recovery. Experimental results are presented in these sections. Conclusions are addressed in Section VI.

II. SYSTEM ARCHITECTURE

The block diagram of the RF link system is shown in Fig. 1. The system is divided in two parts: the primary system, located outside the human body and the secondary system designed to be placed inside the human body. Two radio frequency (RF) data links connect these systems: a forward link which transmits data from the primary to the secondary system and a backward link which operates in the reverse direction. For the intracortical prosthesis prototype half-duplex mode was adopted. The forward link transmits a power/data signal using binary FSK (Frequency Shift Keying) modulation. After demodulation and frame disassembly, useful data is forwarded to the electrodes stimulator. The secondary system power and master clock are derived from the forward link signal. In the opposite direction DBPSK (Differential Binary Phase Shift Keying) is used for data modulation.

The coupling between the primary and the secondary system is accomplished by means of an RF low coupling transformer.

The following specifications were adopted:

- 1 MHz frequency carrier for the forward link.
- 125 kHz frequency carrier for the backward link.
- Transmission rate up to 100 kbps for the forward link.
- Transmission rate of 15.625 kbps in the backward link.

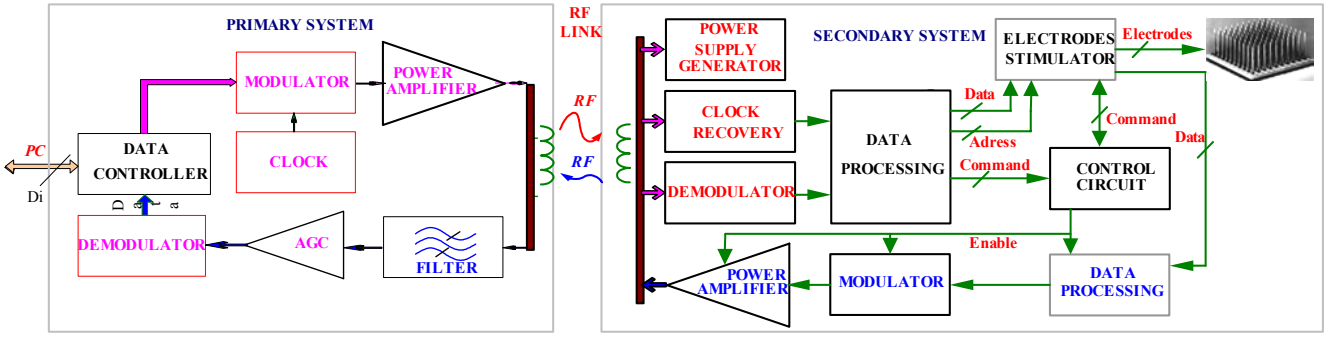

Fig. 1. Architecture of the intracortical prosthesis RF link system.

This work was supported by EC RTD program QLK6-CT-2001-00279.

III. PRIMARY SYSTEM

The primary system emitter (forward link) is represented in Fig. 2. The emitter includes an FSK modulator and a signal amplifier. The FSK modulator is implemented by means of a counter driven by an oscillator at 16 MHz (clock signal). According to the transmitted data bits, 0 or 1, the counter divides the clock signal by 16 or 15, respectively. In this way, modulated data at 1 MHz and at 1.067 MHz frequency is generated. This signal feeds a class E switching-mode tuned power amplifier, configuration that was chosen to optimise the efficiency at the emitter [10]-[12].

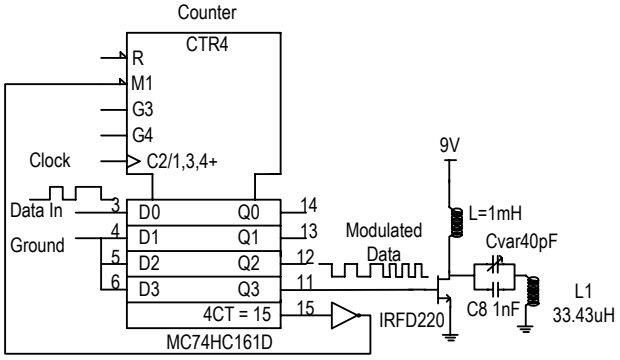

Fig. 2. Primary system emitter.

Fig. 3 illustrates the transmission of the data signal at the class E tuned power amplifier output and at the transformer circuitry output (points A and B of Fig. 7, respectively). As one can see, the very weak magnetic coupling of the transformer produces an important attenuation. However, the signal delivered to the secondary system still allows correct power and data recovery.

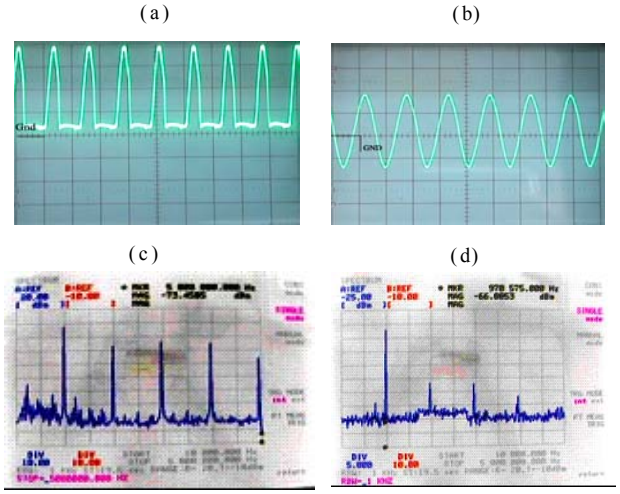

Fig 3. Transmitted signal. (a) Signal before the transformer; (b) Signal after the transformer; (c) Signal spectrum before the transformer; (d) Signal spectrum after the transformer. Intercoil distance of 1 cm.

IV. THE TRANSFORMER

The transformer is of major importance in the RF link. Its performance has a strong influence on the overall functioning of the secondary system. Also, the transformer design must allow the system functioning for different intercoil distances and for different media. In order to analyse the transformer behaviour, the classical equivalent circuit shown in Fig. 4 was used for simulation purposes.

The corresponding parameters were obtained from the real measurements over both the primary and secondary. The loss capacitances C_{p1} and C_{p2} were neglectful. So, when operating at the series resonant frequency, the equivalent circuit can be simplified.

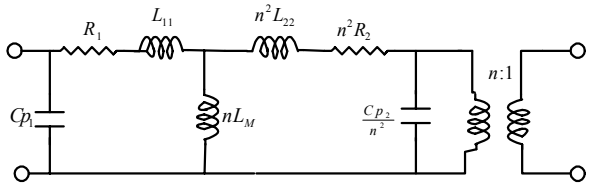

Fig. 4. Transformer equivalent circuit, seen at the primary.

The simulation results presented next were obtained with the PSPICE simulation program. Figs. 5 and 6 illustrate the frequency response of the transformer for different loads and different magnetic coupling (different intercoil distances). The varying load frequency response was obtained for an intercoil distance of 0.5 cm (k=0.3). This study aimed at the analysis of the channel frequency response with a variable load. The load value would be around the expected value for the secondary system power consumption (50 miliwatts). In both cases there is degradation in power transfer between primary and secondary, which is not significant to the load resistor values considered. In the first case, degradation happens for lower load resistance, and in the second case, for increased distance.

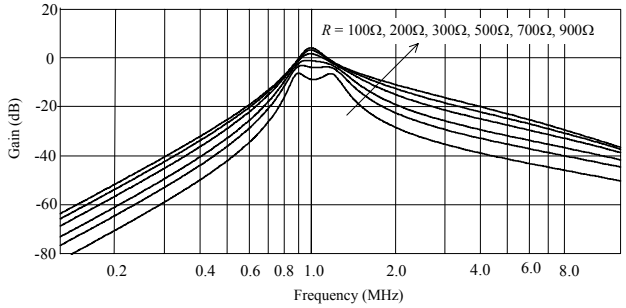

Fig. 5. Transformer amplitude response with varying load and k = 0.3 (RL = 100 Ω, 200 Ω, 300 Ω, 500 Ω, 700 Ω, 900Ω).

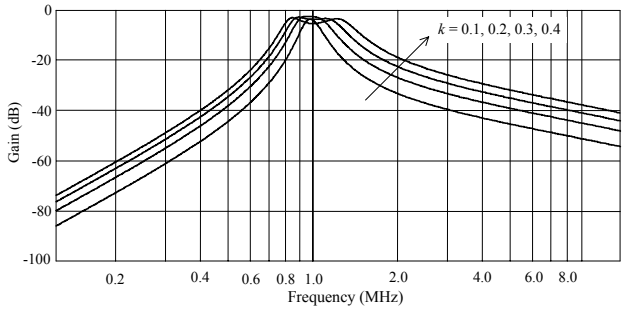

Fig. 6. Transformer amplitude response with a load RL= 200Ω and varying coupling factor (k= 0.1, 0.2, 0.3 and 0.4).

The experimental results concerning the transformer confirmed the theoretical results with the single exception of the bandwidth centre frequency. This is explained by the fact that the transformer equivalent model used in literature considers high magnetic coupling factors (parameter k with value near 1) and does not take into account the distributed

capacitance and skin effect. In fact, this is not the case here, where the absence of an iron core makes it impossible to have a strong magnetic coupling (the measured coupling factor was 0.3). So, a better model of the real transformer can be seen in Fig. 7, where each coil is modeled by a series of RLC elementary units. It is to note that the transformer exhibits a distributed parameter behavior (the distributed elements are represented in dashed line).

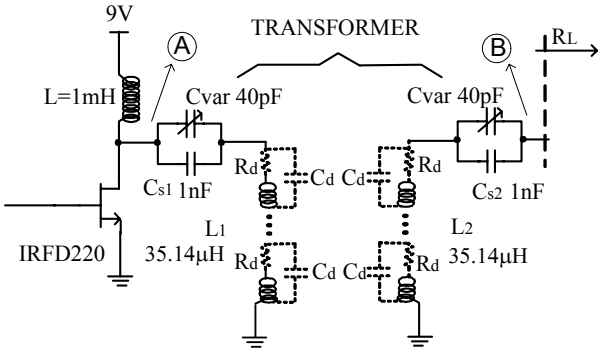

Fig. 7. Low magnetic coupling transformer model.

Fig. 8 illustrates the experimental amplitude response of the transformer for different intercoil distances. The transformer pass band is centered at 1 MHz, as desired.

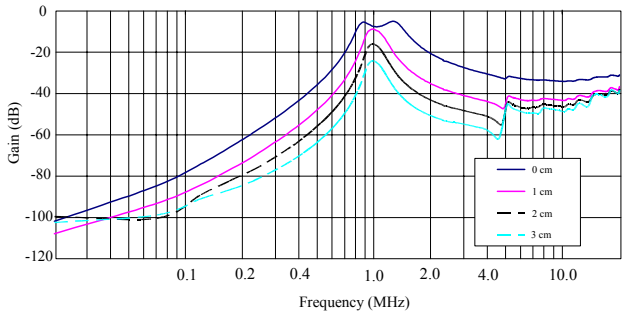

Fig. 8. Transformer amplitude characteristics for 0, 1, 2 and 3 cm intercoil distance.

V. SECONDARY SYSTEM

The receiver architecture is depicted in Fig. 1. The power supply generator is comprised of a half-wave rectifier, protection circuits and series regulator. It is able to recover the required receiver power (stabilized 5 VDC) from the received signal with 35% power efficiency at an intercoil distance of 1cm. The binary FSK demodulator is built around a PLL (Phase Locked Loop) circuit and a comparator, and provides a stream of received data at a bit rate of 100 kbps. This bit stream is fed to a data processing unit, which performs bit and frame synchronization and frame disassembly. Formatted data is then forwarded to the electrodes stimulator circuitry. A reverse link used for monitoring tasks, electrode calibration and impedance measurement is established from the secondary to the primary system at a lower data rate of 15.625 kbps, using DBPSK modulation. This modulation format was chosen because the transmitter is very simple and requires very low power. The clock recovery task is accomplished in the CLOCK RECOVERY block (Fig. 1) by means of a narrow-band PLL designed to produce a reference 1MHz clock from the received signal. The task performed by the bit synchronizer is of fundamental importance to establish a proper time reference in the receiver. The positive-going transitions in this reference clock should accurately signal the optimum instants to sample and detect the received data bits. Fig. 9 shows the part of the receiver interacting with the bit synchronizer.

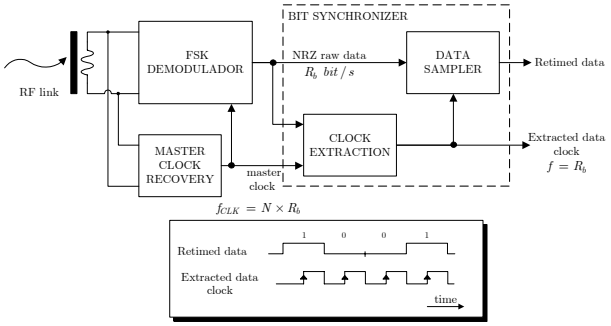

Fig. 9. Data clock recovery and bit synchronizer.

The signal received from the primary system is used to produce the system master clock, with frequency $f_{CLK} = \frac{1}{T_{CLK}} = N \times R_b$ where $R_b = \frac{1}{T_b} = 100$ kbit/s is the raw bit-rate and $N = 10$ (corresponding to a RF carrier frequency of 1MHz). The following point is worth noting: since the master clock is derived from the transmitted signal and is used to demodulate the data, it follows that the data stream is frequency synchronized (i.e., frequency-locked) with the master clock; a data clock could therefore be obtained by suitable division (by a factor N) of f_{CLK}. This is because there is no frequency offset between transmitter and receiver. Although this is true, the (lead or lag) *phase difference* between the positive-going clock transitions and the optimum time epoch for sampling the data — which is the middle time of each bit — is *unknown*. The purpose of the bit synchronizer is thus to provide a stable reference clock with positive-going transitions signaling the middle of each bit (see the time diagram in Fig. 9). Nevertheless, the bit synchronizer which has been developed is also able to track small frequency offsets, with acceptable performance. As can be seen in Fig. 9, the bit synchronizer has a novel feedforward structure; this feature avoids the annoying loop behavior known as *hang-up*, typical in feedback synchronizer operation, which manifests itself as an unacceptably long synchronizer acquisition period, compromising receiver operation. In summary, the bit synchronizer developed has the following desirable properties: 1) in the absence of frequency offset between transmitter and receiver (as it is the case in this application) the recovered clock is *jitter-free* (no dynamic phase error), 2) it has a feedforward structure that avoids the *hang-up* disabling phenomenon and finally, 3) it is easily implemented with simple digital logic. The working principle of the bit synchronizer is best understood with the aid of the waveforms depicted in Fig. 10.

Suppose we have a binary counter being driven with the master clock frequency f_{CLK}; then, it will advance N states within each bit period. If, at time t_0, the counter is in state i then, at time $t_0 + \frac{T_b}{2}$, it will have advanced $\frac{T_b}{2T_{CLK}} = \frac{f_{CLK}}{2R_b} = \frac{N}{2}$ and will be in state $i + \frac{N}{2}$ (on

average); this is the time epoch at which the recovered clock should have a positive transition, marking the middle of the data bit.

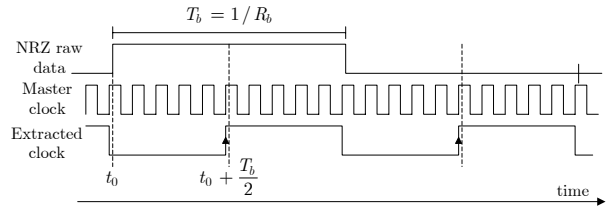

Fig. 10. Bit synchronizer waveforms.

This reasoning justifies the block diagram represented in Fig. 11: the positive-going transition on the data signal (Non-Return to Zero, NRZ random data signal) latches the counter state i, at reference time t_0, and marks the start of a bit. When the counter reaches the state $S = i + \frac{N}{2}$, then $S + \frac{N}{2} \bmod N = (i + N) \bmod N = i$ and the comparator will signal this event to the final processing block, which in turn samples the raw data and produces a clock pulse synchronized with the master clock.

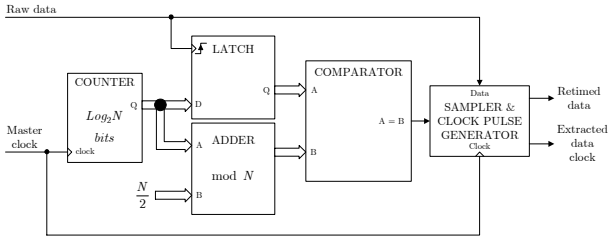

Fig. 11. New feedforward bit synchronizer block diagram.

The synchronizer has been tested using a random NRZ binary data signal as the raw data input and an unsynchronized master clock with no frequency offset.

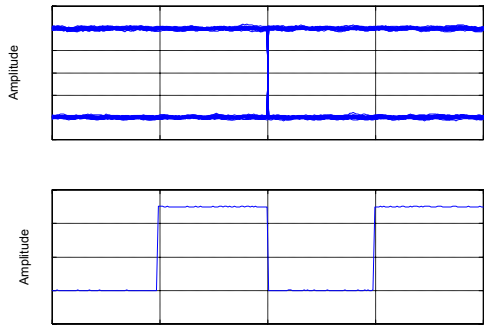

Fig. 12. Bit synchronizer performance with 10 samples per bit and a master clock frequency with no frequency offset.

The resulting eye-pattern diagrams for both the data signal and the recovered data clock are presented in Fig. 12. In the absence of frequency offset, the recovered data clock exhibits no jitter and the positive-going transitions, occurring at $t = \pm 0.5T_b$, accurately mark the optimum sampling instants, at half the bit duration. When the master clock has a small frequency offset, the recovered clock will still be synchronized to the incoming NRZ data stream but will exhibit some amount of phase noise or jitter. Because only $N = 10$ clock periods are available in each bit duration (10 samples/bit), the synchronizer has an inherent phase error of $\pm\frac{T_b}{2N} = \pm\frac{T_b}{20}$, so the positive-going transitions will occur in a $\frac{T_b}{10}$-duration interval around the desired epochs $t = \pm 0.5T_b$. Nevertheless, because high amounts of noise and intersymbol interference are not expected in this system (i.e., operation is with a wide open raw data eye diagram), the synchronizer performance will be acceptable even in the presence of a small frequency offset.

VI. CONCLUSIONS

In this paper the design of an RF link system for an intracortical neuroprosthesis was presented. The system uses FSK modulation which provides better immunity to noise and to the severe amplitude fluctuations due to the transformer weak coupling. Because of its high efficiency, a class E tuned power amplifier was selected to transmit at 100 kbps over a 1 MHz carrier. The transmitted information signal is also used to provide the power for the secondary system (50 miliwatts, inside the patient body) with an average efficiency of 35 % for a 1cm intercoil distance. A new bit synchronizer has been designed. It has a feedforward structure which avoids the *hang-up* phenomenon typical in feedback synchronizers which leads to unacceptably long synchronization acquisition time. The system operates with satisfactory power, data and clock recovery for intercoil distances up to 2 cm. Based on this system, a VLSI chip is currently under development.

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