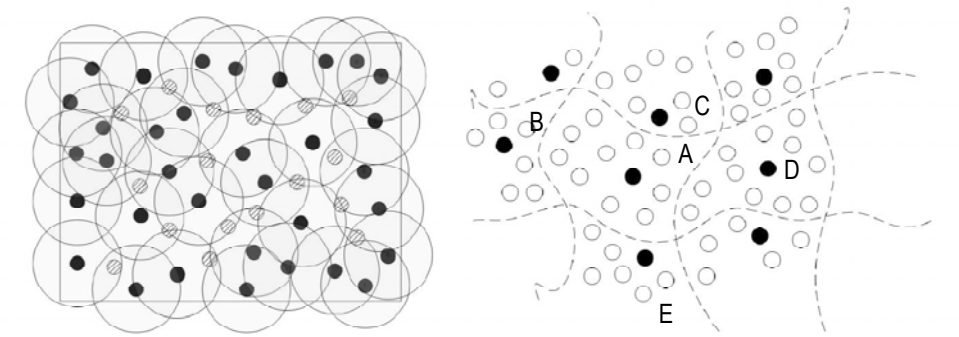
# *Wireless Interfaces*

The Wireless Interfaces Thrust undertakes basic and applied research in wireless interfaces for environmental and biomedical sensor devices. The thrust is exploring CMOS and RF MEMS circuits, miniature antennas, and sensor networking. Full systems incorporating these components are being developed and demonstrated. The wireless thrust is developing wireless interfaces to neural probes, cochlear implants, and other biomedical devices such as arterial stent monitors. The thrust is exploring techniques for moderate range, moderate rate, wireless communication to environmental sensors. Wireless circuits and systems based on RF MEMS and nanometer CMOS are being researched. The demonstration of low-power CMOS transceivers for the Zigbee 2.4GHz sensor network standard is a medium term goal. Other applications and approaches including RFID, and low-power super-regenerative receivers are also being considered. The performance of RF MEMS devices is now close to that of off-chip quartz and SAW components. RF MEMS harnesses the high-$Q$ of micromechanical devices, and this technology promises dramatic improvements in power efficiency of RF circuits. The Wireless Interface Thrust is also exploring circuit and process techniques that will permit the integration of RF MEMS and CMOS wireless circuits. A long-term goal is the integration of RF MEMS, power-efficient CMOS RF, and CMOS baseband circuitry, as well as digital signal processing and miniature antennas in a signal package.

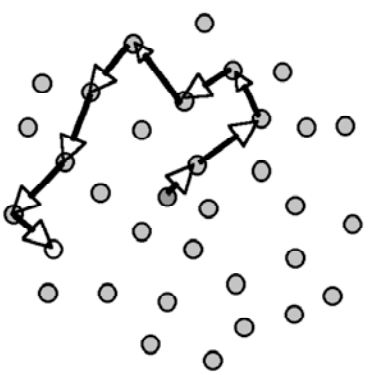
# *Energy-Efficient Networking Mechanisms for Environmental Monitoring Wireless Sensors*

Chih-fan Hsin and Mingyan Liu



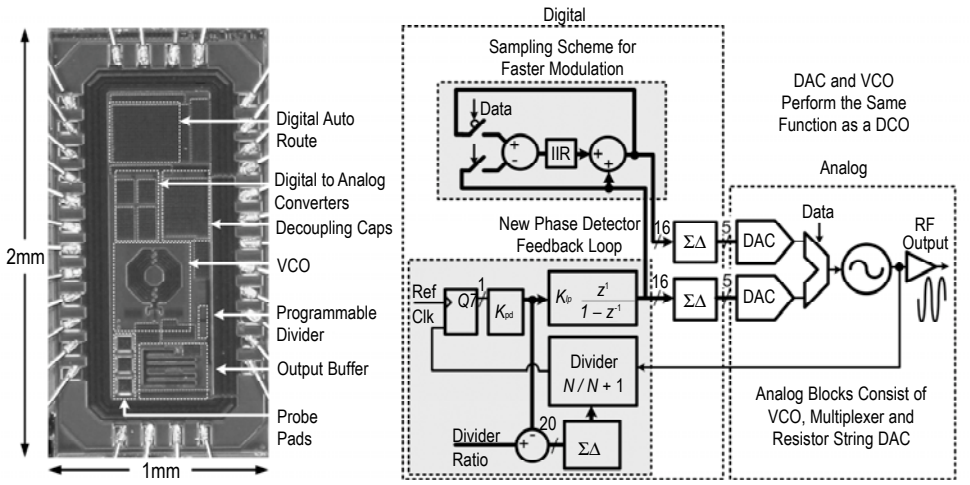

*Left – Illustrations of using low duty-cycled wireless sensors to provide network surveillance and monitoring coverage, Right – and the partial clustering method to provide network connectivity with most of the sensors sleeping.*

The goal of this project is to advance the understanding of the implications of networking a large number of such devices to perform various environmental monitoring and surveillance tasks. In the first part of this project, we have completed the development of a distributed self-monitoring mechanism for wireless sensor networks used in monitoring and surveillance. This scheme combines active and passive monitoring and adopts a two-phase timer concept. It achieves a much lower, false-alarm probability than a typical timeout-based scheme while maintaining the same level of responsiveness. As a second part of this project, we have studied the performance degradation caused by duty-cycling sensors, in terms of network coverage and connectivity. We also developed distributed algorithms by which a sensor can schedule its on and off periods while maintaining network coverage and connectivity (one such algorithm, *partial clustering*, is shown in the figure above). In the third part of this project, we have investigated energy-efficient routing protocols in such a network. We studied two types of random routing (or packet forwarding) strategies: random direction forwarding and random walk-based forwarding (shown on the right). We analyzed their performance in terms of forwarding delays. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.



# *Low-Power Transmitter for Sensor Networks*

Mark A. Ferriss and Michael P. Flynn



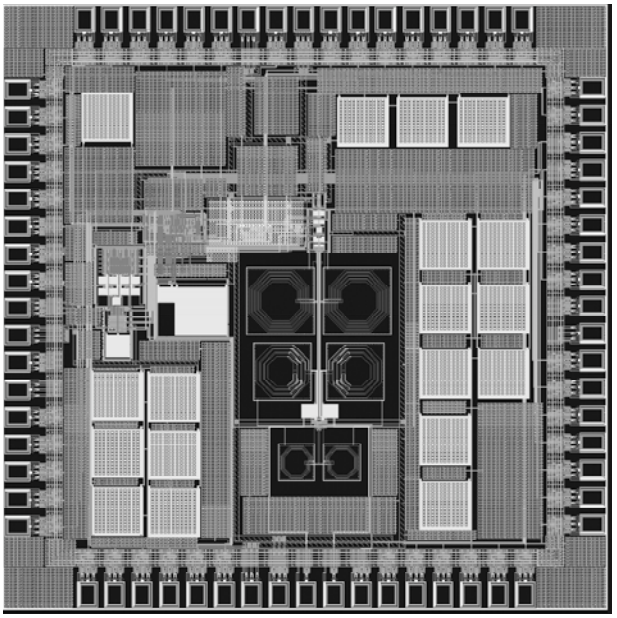

*Die photo and block diagram of the transmitter.*

The aim of this research is to develop a new architecture for a wireless transmitter with an emphasis in performing much of the analog functions, which are typically required in the digital domain.

The proposed transmitter architecture performs direct modulation by varying a phase-locked loop (PLL) divide ratio. We developed a synthesizer that utilizes a novel, all-digital phase detector in place of the conventional analog-intensive phase detector, charge pump and loop filter blocks. In addition, the design uses a digital dual-modulation scheme that alleviates the tradeoff between loop bandwidth and switching speed. These techniques were developed as part of a prototype 14mW, 2.2GHz, MSK transmitter with a transmission rate of 927.5kbit/s. Silicon testing and tape-out of a prototype transmitter was carried out in 2006, with the results to be published in ISSCC 2007. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# A Low-Power CMOS Receiver

Jia-Yi Chen and Michael P. Flynn



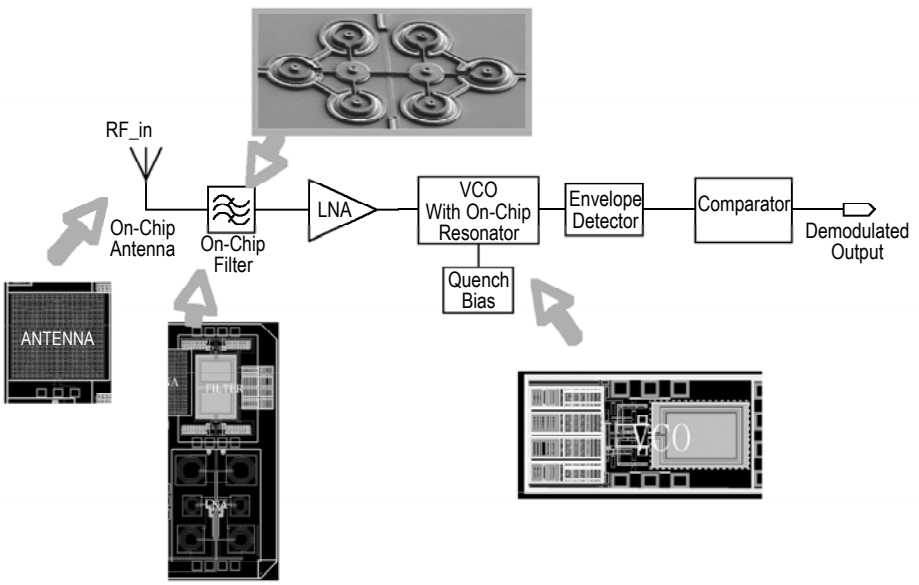
*2.4GHz low-power, super-regenerative CMOS radio in 0.13μm CMOS.*

Wireless communication has experienced exponential growth due to the need for connectivity and data exchange. Most communication systems focus on the quality of service issues such as high-data-rate and wide coverage area. However, there are applications such as implantable neuroprosthetic devices, robotics, and home automation with completely different characteristics. These only require short communication range and low-data-rates, but power consumption must be very low to support long lifetime, and the radios must be very small.

A fully integrated, auto-calibrated, super-regenerative receiver was presented at the 2006 International Solid State Circuits Conference. Consuming only 2.8mW, this receiver has a record low-energy-consumption per received bit. The receiver occupies less than 1mm$^2$ and has a measured sensitivity of -90dBm. This project is supported in part by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *A Fully Integrated CMOS Receiver*

Dan Shi and Michael P. Flynn



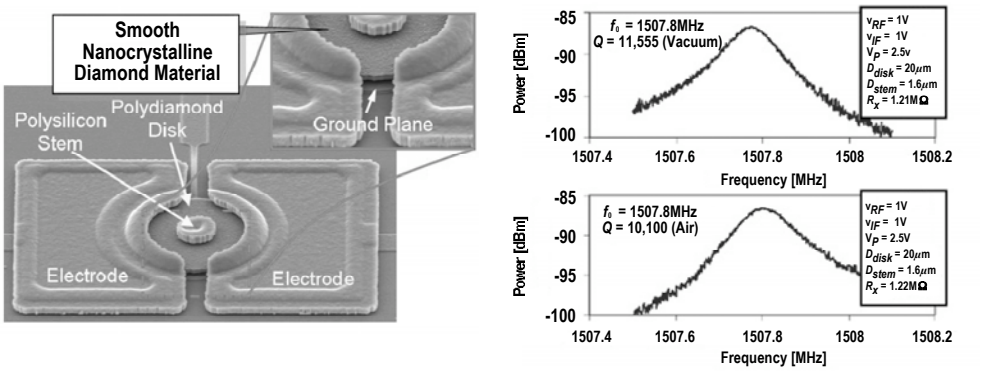

*Fully integrated CMOS radio in 0.13μm CMOS.*

The rapidly growing wireless communication market is creating a growing demand for radio frequency (RF) transceivers. To minimize the size and cost, more and more RF bands and standards, or even the entire transceivers, have been integrated into one chip. This project focuses on developing a wireless solution which is highly integrated with on-chip passive components and that is small size and requires very low power. This is for applications which need short range, low-data-rate, but a long lifetime. These include wireless devices used in implantable neuroprosthetic devices, environmental wireless sensors, etc.

Several prototype components including a 5GHz VCO with on-chip resonator and 5GHz bandpass filter, were designed and fabricated. The VCO achieves a measured phase noise of -117dBc/Hz at a 1MHz offset. Tape-out of a prototype receiver is planned for 2007. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *Low-Power UHF Micromechanical Voltage-Controlled Oscillator (VCO)*

Jing Wang and Clark T.-C. Nguyen

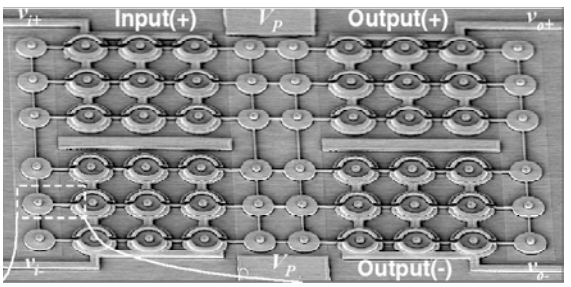



*A SEM (left) and measured frequency responses (right) of a 1.51GHz CVD diamond micromechanical disk resonator with Q's >10,000 in both air and vacuum.*

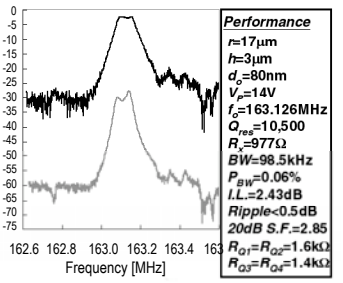
This project aims to demonstrate a voltage-controlled oscillator utilizing a tunable, UHF, micromechanical resonator, or switchable bank of such resonators, as its high-*Q* frequency-setting element. Due to the sheer *Q* of its resonator tank elements and the removal of the need for phase-locking to a lower frequency reference, such an oscillator should be capable of achieving low phase noise while consuming very little power compared to present-day synthesizers. En route to demonstrating a complete oscillator, a micromechanical resonator capable of operating at GHz frequencies while retaining *Q*'s on the order of 10,000 is needed. Pursuant to further extending frequency and *Q* of the subject radial contour mode disk resonator, CVD polycrystalline diamond material with the highest to date acoustic velocity among surface-micromachinable materials has been utilized as the structural material along with polysilicon self-aligned stem. Using this technique, the first CVD nanocrystalline diamond micromechanical disk resonator with material-mismatched stem has been demonstrated at a record frequency of 1.51GHz with an impressive *Q* of 11,555, which is more than 4.5 times higher than demonstrated in a previous 1.156GHz polysilicon disk resonator, and which achieves a frequency-*Q* product of $1.74 \times 10^{13}$ that now exceeds the $1 \times 10^{13}$ of some of the best quartz crystals. Custom integrated circuit design to achieve a VCO based on these resonators is already underway. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *UHF Micromechanical Transmit Filters*

Sheng-Shian Li and Clark T.-C. Nguyen




*Left – The SEM of a polysilicon fabricated differential micromechanical disk-array filter.*



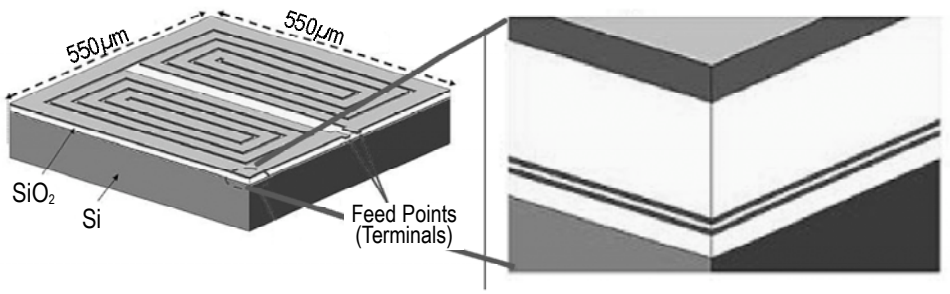

*Right – Measured frequency characteristic for a differential micromechanical disk-array filter.*

Although capable of unprecedented on-chip frequency shaping, the micromechanical filters demonstrated to date have had difficulty processing high-power signals, such as those commonly seen in the transmit path of wireless communication devices. This project aims to realize micromechanical filters at GHz frequencies capable of handling power levels typically seen in the transmit path of wireless communication devices. One of the more promising techniques under investigation is the use of large arrays of small resonators that can distribute the power load over several devices. With this in mind, a medium-scale integrated (MSI) vibrating micromechanical filter (cf., left figure) circuit that comprises 128 radial-mode disk and mechanical link elements to achieve low motional resistance while suppressing unwanted modes and feedthrough signals has been demonstrated with a 0.06%-bandwidth insertion loss less than 2.5dB at 163MHz. The ability to attain an insertion loss this small *for such a tiny percent bandwidth on-chip* is unprecedented and is made possible here by the availability of $Q$'s >10,000 provided by capacitively transduced resonators. By realizing the most complex hierarchical mechanical circuit to date, the 163MHz filter of this work achieves an insertion loss of 2.43dB for 0.06% bandwidth and a 20dB shape factor of 2.85, all with a constituent resonator motional resistance $R^x$ of only 977Ω. All aspects of this filter's response are predictable via ANSYS and SPICE-based mechanical and electrical models, respectively, instilling a confidence in our models that now paves the way for larger array filters at higher frequency. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# A Miniature High-Impedance Antenna

Wonbin Hong and Kamal Sarabandi

This project entails the design and demonstration of miniaturized antennas with the possibility of achieving complete integration with the RF front end, and ultimately achieving a single-chip wireless system. The antennas need to be placed above ground plane which limits their radiation efficiency and reduces the bandwidths. Reducing the size, increasing the bandwidth, and improving the efficiency of the antenna in the presence of the ground plane are problems that will be addressed.



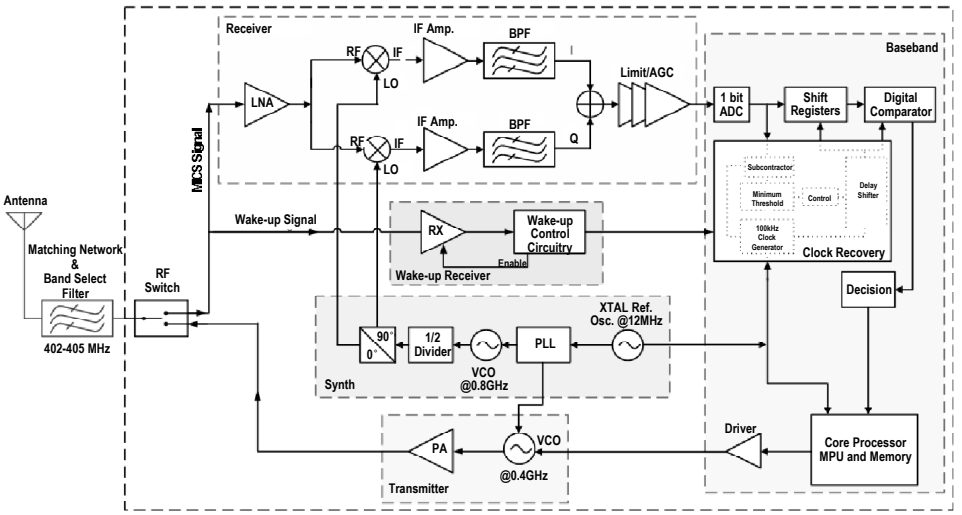

*Miniaturized 9GHz slot antenna fabricated using 0.13μm CMOS process. Left – Expanded view of the wafer corner showing two parallel ground planes each 0.6μm thick separated by 0.6μm (M4 and M5).*

This project has three main phases: first, to design a miniaturized antenna without a ground plane and with a fairly high efficiency to conserve as much power as possible; second, enhancing the bandwidth of the miniaturized antenna and increasing the input impedance of the antenna so that it can be matched to a very high impedance; and finally, the radiation efficiency of the antenna in the presence of a ground plane must be enhanced. The first task is fulfilled knowing that by a virtual enforcement of the required boundary condition at the end of a slot antenna, the area occupied by the resonant antenna can be reduced. Furthermore, loading the antenna with distributed inductors also reduces the antenna size. Combining these two techniques results in a highly miniaturized slot antenna. Different bandwidth enhancement techniques that increase the BW while maintaining the size have also been demonstrated.

Miniaturization of the antenna will be achieved via alternative slot antenna geometries, for which the antenna impedance can be varied (and matched to any RF input) by attaching the RF front-end circuit at the proper slot location. Design and fabrication of an on-chip antenna using 0.13$\mu$m CMOS process was demonstrated. This project is supported by the Engineering Research Centers program of the National Science Foundation under NSF Award Number EEC-9986866.

# *Low-Power MICS Transceiver*

James D. Griggs, Huseyin Savci, Zheng Wang, Ping Yin,
and Numan S. Dogan

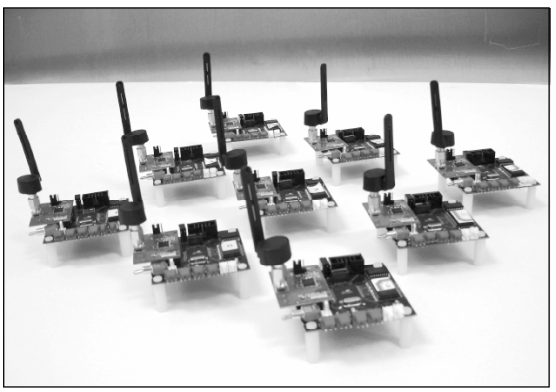



*Ultra-low-power MICS transceiver.*

The Medical Implant Communications Service (MICS) is an ultra-low-power, unlicensed, mobile radio service for transmitting data in support of diagnostic or therapeutic functions associated with implanted medical devices. U.S. Federal Communications Commission (FCC) allocated a 402–405MHz frequency band for MICS operations on a shared, secondary basis in 1999. A MICS transceiver is being designed and implemented using IBM's 0.18$\mu$m RF CMOS process with reduced supply voltage (1V). Single-ended LNA with source degeneration inductor and cascode transistor is used for its low-power dissipation and ease of interfacing to an antenna. LNA provides 15dB gain, 0.9dB noise figure, -19.5dBm 1-dB compression point, and -5.3dBm IIP3 while dissipating 0.5mW power from 1-V supply. The N- and P-MOS cross-coupled pair LC VCO with current-limiting resistors is chosen among all other topologies because of its performance for low-power dissipation. The VCO operating at 800MHz followed by a divide-by-two is the best choice for quadrature signal generation at 400MHz, achieving 177$\mu$W for the VCO and 25$\mu$W for the divider. Phase Noise at 1MHz offset is -127.3dBc/Hz. Peak-to-peak voltage is 940mV. Figure of Merit of the VCO is -186dB. Ultra-low-power designs are sensitive to process, temperature, and supply voltage variations. Dynamic body biasing is used to substantially reduce the sensitivity to process and supply voltage variations. By using conventional CMOS technology and ultra-low-power designs, we are achieving circuit performances that are comparable to RF circuits employing MEMS-based resonators. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *Narada: Low-Cost Wireless Sensors for Monitoring and Control Applications*

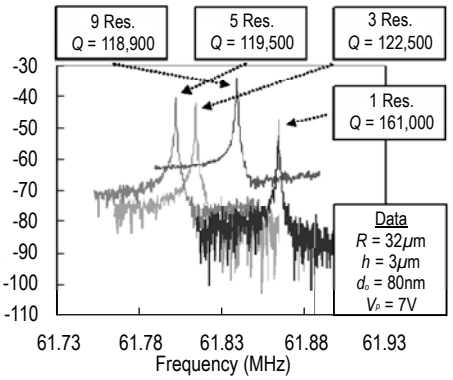
Andrew Swartz, Andrew T. Zimmerman, Arman Kizilkale, and Jerome P. Lynch



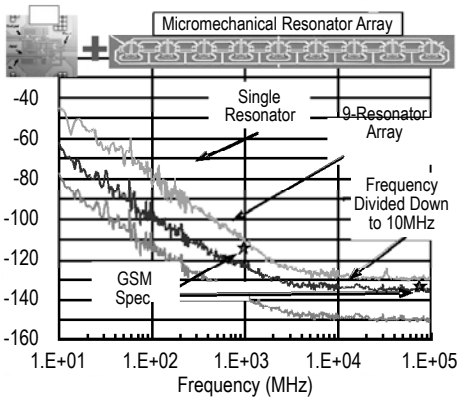
A new wireless sensor platform, termed Narada, has been developed by the WIMS ERC reseachers for a variety of monitoring and control applications. Designed from commercial off-the-shelf components, Narada offers multichannel sensor and actuator interfaces. The internal 16-bit analog-to-digital converter can simultaneously collect sensor data from four channels at rates as high as 100kHz. A two-channel, 12-bit digital-to-analog converter provides the wireless sensor with the capability to output voltage signals from 0V to 4V to actuators. The low-power, 8-bit Atmel ATmega128 microcontroller has been selected as the wireless sensor's computational core. To facilitate interoperability with commercial wireless sensor nodes (e.g., Crossbow Motes) using the IEEE 802.15.4 wireless sensor protocol stack, the Chipcon CC2420 wireless transceiver is integrated with the Narada node. A multithread operating system featuring a complete implementation of the IEEE 802.15.4 physical and medium access control protocol layers has been embedded in the wireless sensor core. To validate the functionality of Narada, a multinode wireless sensor network has been installed in a variety of engineered systems. For example, wireless monitoring systems based on the Narada wireless sensor has been installed in the Geumdang Bridge (Korea), Voigt Bridge (California), Grove Street Bridge (Michigan), and Gi-Lu Suspension Bridge (Taiwan), to monitor bridge behavior to traffic and wind loads. To validate the closed-loop control performance of the wireless sensor platform, a multinode wireless sensor network was installed in a test building in which adjustable dampers were used to mitigate structural responses during earthquake loadings. This is the first ever full-scale implementation of a wireless structural control system applied to civil engineering structures for seismic protection. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *Micromechanical Resonator Reference Oscillator*

Yu-Wei Lin and Clark T.-C. Nguyen




*Left – Measured frequency characteristic for a fabricated wine-glass disk resonator array, showing Q's > 110,000 even in large arrays.*

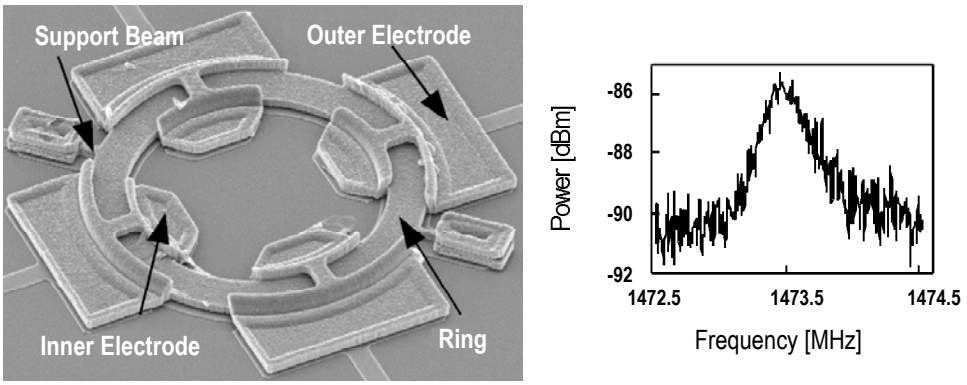



*Right – Phase noise density versus carrier offset frequency plot for the oscillator using various resonator combinations, showing that GSM phase noise spec. is satisfied.*

This project aims to demonstrate a high-*Q*, low-phase noise micromechanical resonator oscillator for use as an on-chip reference oscillator in wireless transceivers. The particular oscillator will utilize a micromechanical resonator specifically designed to handle sufficient power levels so as to allow it to achieve adequate far-from-carrier phase noise in an oscillator circuit. Consistent with this, recent work has focused on an array-composite wine-glass disk micromechanical resonator. A reduction in phase noise by 13dB has been obtained over a previous 6MHz surface-micromachined micromechanical resonator oscillator by replacing the single resonator normally used in such oscillators with a mechanically coupled array of them to effectively raise the power-handling ability of the frequency selective tank. Specifically, a mechanically coupled array of nine 60MHz wine-glass disk resonators (figure at left) embedded in a positive feedback loop with a custom-designed, single-stage, zero-phase-shift sustaining amplifier achieves a phase noise of -123dBc/Hz at 1kHz offset and -136dBc/Hz at far-from-carrier-offsets (figure at right). When divided down to 10MHz, this effectively corresponds to -138dBc/Hz at 1kHz offset and -151dBc/Hz at far-from-carrier-offset, which represent 13dB and 4dB improvements over recently published work on surface-micromachined resonator oscillators, and also now beat stringent GSM phase noise requirements by 8dB and 1dB, respectively. This project is supported by the Defense Advanced Research Projects Agency (DARPA) under Grant No. F30602 01-1-0573.

# *UHF Micromechanical Receive Filters*

Yuan Xie and Clark T.-C. Nguyen

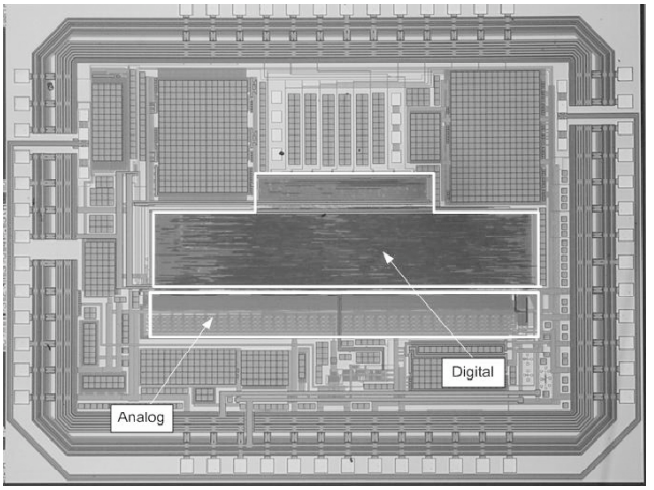



*SEM of a 426MHz extensional wine-glass mode polysilicon micromechanical ring resonator, and measured frequency spectrum for a 1.47GHz version of this resonator.*

This project investigates methods for achieving high-$Q$ $\mu$mechanical resonators and filters that operate at UHF frequencies. Bandpass filters for band or channel selection in wireless transceivers are of particular interest, and these are achieved by interlinking mechanically vibrating components in networks that realize the desired bandpass transfer functions. With $Q$'s in the thousands, or even tens of thousands, mechanical resonators are very well suited to this application, and should be able to achieve insertion losses less than 1dB for very small percent bandwidth filters. To date, a ring resonator structure (above figure) using a unique extensional wine-glass mode shape that combines aspects of previous radial and wine-glass disks, and a radial annular ring, has been demonstrated at a frequency of 1.47GHz with a $Q$ of 2300. Due to its larger electrode-to-resonator overlap area, this device also achieves a motional resistance six times lower than posted by previous radial-mode disks in the same frequency range, making it particularly suitable for use in front-end RF filters, for which direct connection to the antenna is desired. Work on filter design using this resonator is now underway, as are efforts to further raise the $Q$ of this device to values above 10,000 (for RF channel-selection applications). In the meantime, methods for suppressing spurious modes, which are more troublesome for this ring resonator than for previous disks, have also been under investigation. This work is supported by the Defense Advanced Research Projects Agency (DARPA) under Grant No. F30602-01-1-0573.

# *Digitally-Corrected, Nyquist-Rate, Analog-to-Digital Converters*

Ivan T. Bogue and Michael P. Flynn



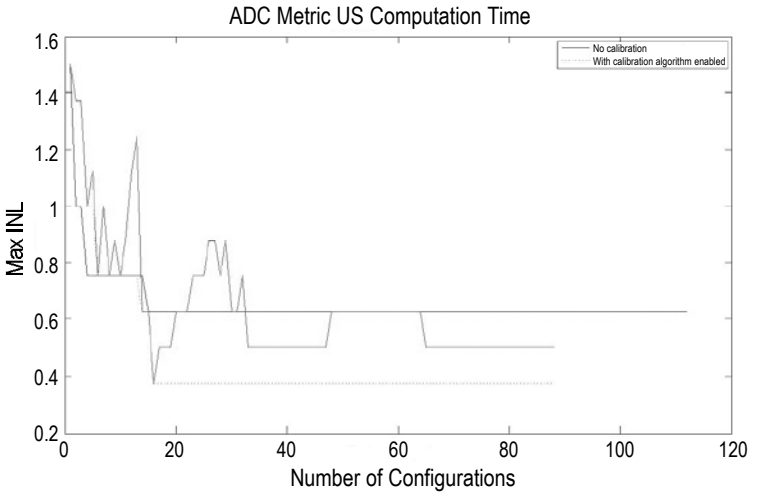

*8-bit digital CMOS folding ADC.*

According to the 2001 International Technology Roadmap for Semiconductors, improved ADC technology is a key factor in the development of present and future applications. The switched-capacitor (SC) pipeline technique is the most popular method of implementing moderate resolution ADCs. However, process scaling is eroding the advantages of CMOS which originally made SC circuits feasible. Good switches and opamps are becoming increasingly difficult to design, and the growing gate leakage of deep submicron MOSFETs is causing difficulty. Traditional ADC schemes do not work well with supply voltages of 1.8V and below.

This work involves the development of digital calibration techniques for Nyquist-rate Analog-to-Digital Converters. These allow the analog circuitry to be greatly simplified. Digital processing is used to compensate for transistor non-idealities and mismatch. Since the link between size and accuracy is broken, the analog circuits can be small, fast, and power efficient. A prototype chip was taped out in TSMC 0.18$\mu$m. The 8-bit folding ADC has no missing codes at a clock-rate of 850MHz. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *Self-Calibrating Moderate Resolution Analog-to-Digital Converters*

Andres A. Tamez and Michael P. Flynn



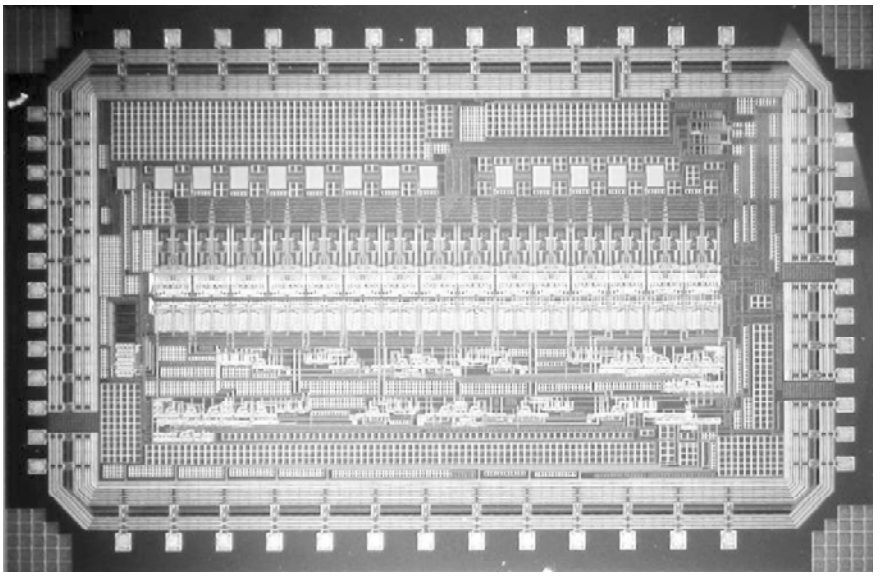

*Comparison of calibrated and non-calibrated capacitor arrays in simulation.*

The accuracy of SAR analog-to-digital converters is deteriorated by mismatch in the DAC capacitor array. Our goal is to identify an optimization algorithm that can be implemented on-chip to calibrate the capacitor array to yield the best ADC performance. The optimization algorithm is modeled in MATLAB to determine the effects of different algorithm parameters. Monte Carlo simulations are used to measure the effectiveness of the algorithm and compare the performance of both the calibrated and unmodified ADC's. The algorithm will be implemented with the help of a calibration engine, a SRAM array, and calibration logic. The graph above shows a Monte Carlo simulation of 100 10-bit capacitor arrays.

Moderate resolution low-power ADCs are required for digitization of sensor outputs and for digitizing baseband signals in the wireless transceiver. The SAR ADC architecture is a good candidate for digitizing wireless IF or baseband signals. This work complements the work on CMOS transceivers and on ADCs at the WIMS Center. A 10- or 12-bit SAR ADC would be very useful for sampling IF signals in a sensor network wireless receiver. This project is funded by GEM Fellowship, Analog Devices, and supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *Deep Submicron CMOS Flash Analog-to-Digital Converters*

Sunghyun Park and Michael P. Flynn



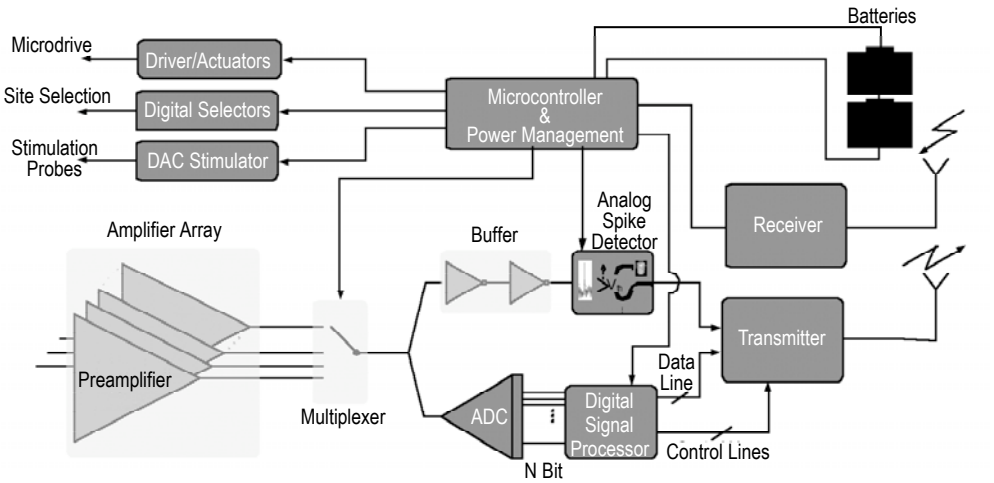
*A 4GS/s 4-bit flash type analog-to-digital converter in 0.18μm CMOS.*

The goal of this project is to develop very fast analog-to-digital conversion techniques for wireless applications. Very fast analog-to-digital converters are required to digitize high-frequency IF radio signals in UWB and 'digital' radio architectures. This work investigates the use of RF techniques in the design of Nyquist-rate ADCs, with multi-GHz sampling rate. A sampling rate of 4GS/s was achieved.

A 4GS/s 4-bit prototype ADC was presented at the 2006 International Solid State Circuits Conference. This ADC implemented in 0.18$\mu$m digital CMOS is one of the fastest ADCs implemented in this technology node. This project was partially funded by Intel, Texas Instruments, Inc., and National Science Foundation.

# *Lightweight Bidirectional Wireless Neural Recording and Control Microsystem*

Amir Borna and Khalil Najafi

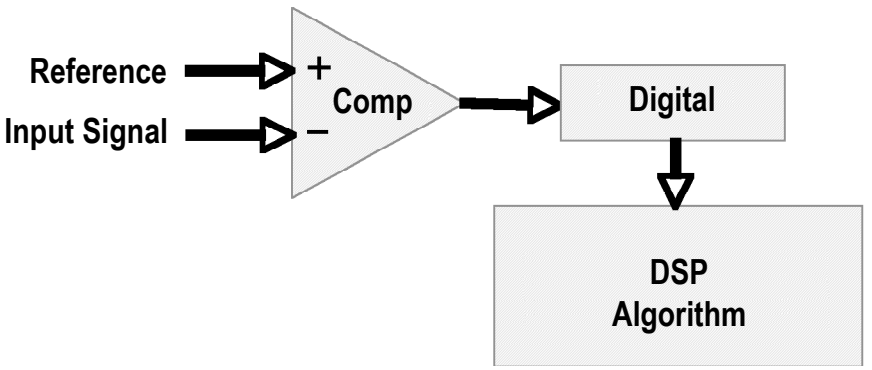



*Architecture of a multichannel, bidirectional wireless biopotential recording microsystem for in-vivo recording of spontaneous neural activity from unrestrained animals.*

Wireless recording of neural activity from biological hosts is important in neurosciences. It is required that neural activity is recorded from an unrestrained animal, and the information is wirelessly transmitted to a remote host. In this project, a low-power, multichannel, standalone, integrated wireless FM system is being developed for a variety of biomedical recording applications. Signals are recorded by micromachined electrodes, amplified, time-division multiplexed, and then modulated onto an FM carrier. The transmitted signal is picked up by an FM receiver, which decodes it and then displays it for future use. Previous versions of the system utilized batteries for operation. Both 4- and 8-channel wireless recording microsystems have been developed, featuring on-chip ac amplification, dc baseline stabilization, time-division-multiplexing, and wireless FM transmission of input biopotentials with frequency contents from 0.1–7kHz while dissipating <2mW from 3V. We have demonstrated wireless *in-vivo* recording of spontaneous neural activities at 96.2MHz from the auditory cortex of an awake marmoset monkey up to 50cm away with signal-to-noise ratios in the range of 8.4 to 9.5dB. This project is supported by the NIH through a subcontract from University of Pennsylvania in collaboration with Professor Marc Schmidt in the Department of Biology.

# *Very-Low-Power Analog-Digital Conversion for Low-Power Wireless Transceivers*

Shahrzad Naraghi and Michael P. Flynn



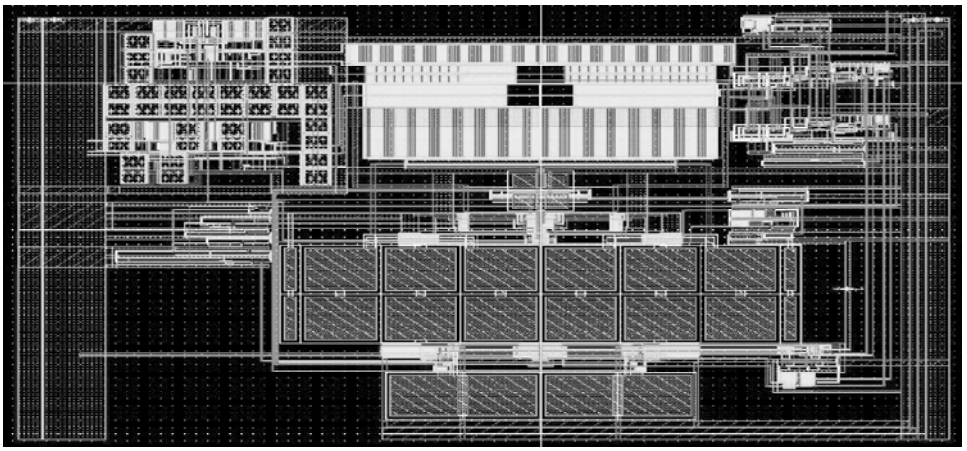

*Block diagram of the ADC.*

Reducing the power consumption and chip area of analog-to-digital converters is a big challenge in today's research since analog-to-digital converters are key building blocks in all communication, sensing, and imaging systems. We are investigating a new very-low-power ADC scheme that helps us in this goal by putting most of the accuracy burden on digital processing, significantly improving energy efficiency and size.

Digital correction and calibration are used extensively in this ADC. Tape-out of a prototype ADC is planned for 2007. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866.

# *Oversampled Analog-to-Digital Converters*

Chun C. Lee and Michael P. Flynn



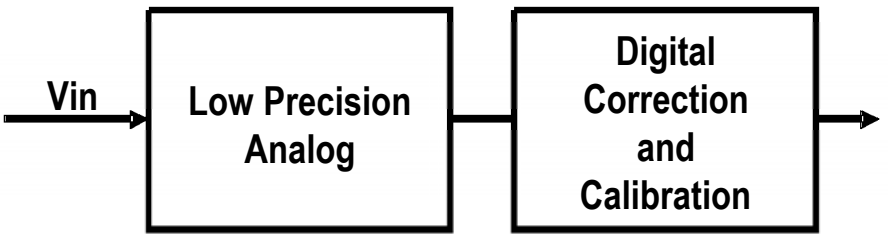
*An Integrator used for oversampling analog signals, designed in modern sub-micron CMOS technology.*

Current state-of-the-art CMOS integrated circuit (IC) processes are ideally suited to implementing digital circuits; but they do not deliver the precision and accuracy required for high-resolution analog design. This is because the transistors have poor analog properties (such as linearity and gain) and the shrinking of the supply voltage makes the matter worse. The Analog-to-Digital Converter (ADC) is a key analog component in most applications. Thus, new techniques need to be developed to design ADCs in these new IC processes. Furthermore, the performance requirements (in terms of resolution, speed, and power) of such ADCs also increase with newer applications.

This work involves the use of oversampling techniques to trade off speed for accuracy in ADCs. Sigma-delta (or oversampling) ADCs have been used traditionally for low-bandwidth, high-accuracy applications, trading speed for accuracy. This work explores the use of oversampling in high-speed applications. This project is supported by an NSF CAREER grant.

# *End of the CMOS Scaling Roadmap ADCs*

Jorge Pernillo and Michael P. Flynn




*ADC Structure—Digital techniques will allow us to decouple analog accuracy from ADC accuracy. This allows the analog circuitry to be small, fast, and power efficient.*

Our goal is to investigate new approaches to analog-to-digital conversion that are suited for end-of-the-roadmap CMOS, and which also deliver orders-of-magnitude improvements in speed and energy efficiency. We break analog-to-digital conversion down to its essence and simplify the process of analog-to-digital conversion to its most basic form. This allows us to take advantage of the tremendous digital capability of nanometer processes and then implement the analog circuitry in the simplest way.

We propose an ADC structure that is comprised of low-precision comparators aided by digital processing. The architecture incorporates redundancy to cancel mismatch and offset. Tape out of prototype ADC is planned for 2007. This project is supported by an Intel Ph.D. Fellowship.