

Quarterly report
Chronic Microelectrode Recording Array
NIH/NINDS
Period 07/01/06 – 09/30/06

Project: NIH/NINDS **Contract-No.** HHSN265200423621C
Date: 07/01/06-09/30/06

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I. Executive Summary

The overall goal of the contract No. NIH/NINDS HHSN265200423621C is to develop and test (in-vivo) a chronically implantable neural recording array and provide the device to the neuroscience community upon completion of the initial technical development phase for experimental use and evaluation.

The objective of the eighth contract quarter (Q8) as proposed was to:

- a) Continue optimizing the backside (rerouting metallization) to improve adhesion and support more reliable flip-chip bonding.
- b) Develop characterization techniques to optimize the front side metallization for adhesion and mechanical stability.
- c) Design the third version of INI chip.
- d) Continue design, construction, and testing of external interface components (i.e. power supply coil, forward telemetry transmitter, software controls, etc).
- e) Continue flip-chip integration work with addition of surface mount devices (SMDs) and custom made coil spacers to the integrated device.
- f) Continue leakage current, impedance spectroscopy, adhesion and dissolution long term tests of SiC and Parylene encapsulation in buffer solution and subsequent further development of Parylene and SiC coating processes, materials characterization (material composition, electrical and chemical properties).
- g) Conduct leakage current long term tests of the outermost mechanical protection layers of silicone and epotek ®.
- h) Continue to conduct acute *in vivo* tests to investigate the affects of fully integrated UEA implant.

Throughout the eighth quarter, all of the above mentioned objectives were completely accomplished.

II. Activity Summary

Key results for project period (Q 8) (work packages)

- Fabrication of UEA test and hot chips: fabrication of UEAs was continued. The Microsystems Lab is now in a production mode where new wafers are fed into the process every week. Work is in progress for implementing wafer scale processes especially wafer scale etching which is the biggest bottle neck at this point in fabrication.
- Development and fabrication of electronics and communications module: The external interface circuits have been tested. The 3rd version signal processor is being designed with the new knowledge gained after testing INI1 and INI2.
- Development and fabrication of PI/BCB coil: Design of the PI coils has been finalized and fully characterized.
- Flip-chip bonding and assembly: The concept of integrating the fully functional device has been tested and new backside metallization has been tested and finalized.
- Hermetic encapsulation and layer coating: The adhesion between parylene and the device materials has been tested. The leakage current test was performed on the mechanical protection layers.
- In vivo wireless recording: The evaluation of Utah wireless telemetry system by periodic recording of cortical neural activity in anesthetized cats that stated on June 7th 2006, was suspended after 51 days of testing on July 28th 2006 because of the dropping quality of the signals on both, the benchmark Cerebus system and the new wireless system. This cat is alive to date and behaves normally. Histological studies are on going both on the arrays and tissue from previous two implants.

Meetings/presentations during project period (Q 8)

- Telephone conference with IZM. Audit of IZM branch at the U of U by the Fraunhofer and initiatives taken to further increase the collaboration between U of U and Fraunhofer institutes.
- Exchange of emails and personal meeting with GVD Corporation, Cambridge, MA. Test chips were handed for the deposition of PTFE films to study the encapsulation properties of PTFE.
- Individual weekly project meetings of the project teams at the University of Utah as well as the subcontractors; meeting minutes are created in common format by all partners.

Patents (Q 8)

- Further processing of previously submitted invention disclosures. Initiation of patent search on neuroprosthetic devices to identify the profile for further invention disclosures, e.g. for the signal processor and coil design.

Organizational accomplishments (Q 8)

- Rescheduled the electrical and biocompatibility tests on PTFE based thin film layers.
- Implemented protocols for good manufacturing practices and good laboratory procedures (GMP/GLP) in preparation of potential later FDA approval.

III. Research Results and Discussion

III.a. Probe system fabrication

III.a.1 Task 1 Fabrication of ultra thin Utah Electrode Array

Description/Rationale

During the past quarter we have made several further improvements in the array fabrication processes. The wafer scale etching process has been partially characterized. The experiments have been designed and being conducted to compare the adhesion and charge injection properties of iridium oxide deposited by three different techniques.

Experimental Results

Waferscale Etching: A stirring system and a wafer holder have been designed and built for etching the array-columns on a wafer scale. As seen in Figure 1 the wafer is placed in a recessed Teflon holder over an O-Ring that protects the back-side of the wafer from the etchant. The holder is attached to a clock motor for stirring. The geometries of the electrodes that were etched conventionally and on a wafer scale were compared. The non uniformity of electrodes in nine 10×10 arrays that were conventionally etched was compared with that of arrays from a wafer scale etching, Figure 3. The initial results show comparable non uniformity in the electrodes.

Front Side Metallization: Traditionally, to reduce the impedance of the electrodes, Iridium metal is sputtered and then electrochemically activated to form iridium oxide. Activation time for an array is about 72 hours. Alternative iridium oxide deposition methods are considered to reduce the process time. Electrodeposition is one way to deposit iridium oxide directly on the electrodes. As a proof of concept, iridium oxide was electrodeposited on the tip of a platinum wire. 50 nm thick iridium oxide layer was deposited on the tip of a platinum wire of diameter 10 um in 4 minutes. Charge injection capacity was calculated from Figure 4 to be 0.29 mC/cm².



Figure 1: Picture of etching holder for wafer scale etching

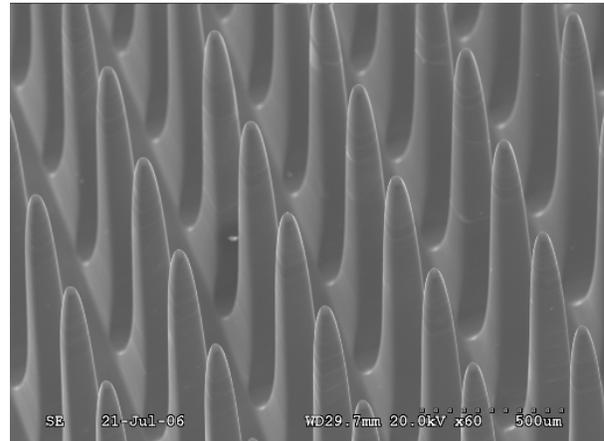


Figure 2: SEM micrograph of the electrodes etched by wafer scale etching process

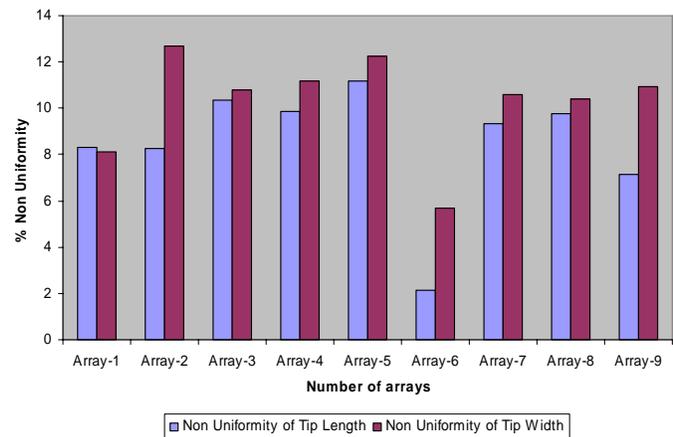
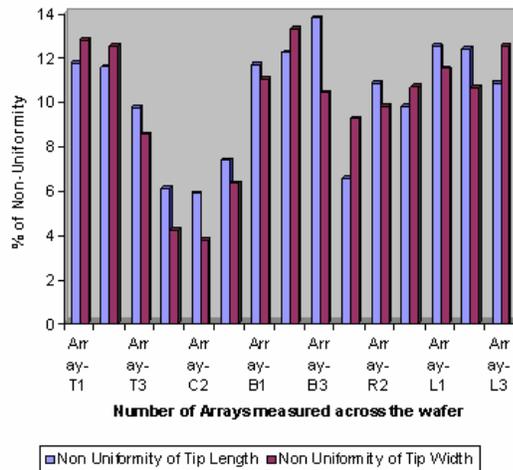


Figure 3: Non uniformity in the geometry of electrodes etched conventionally (left) and on wafer scale (right).

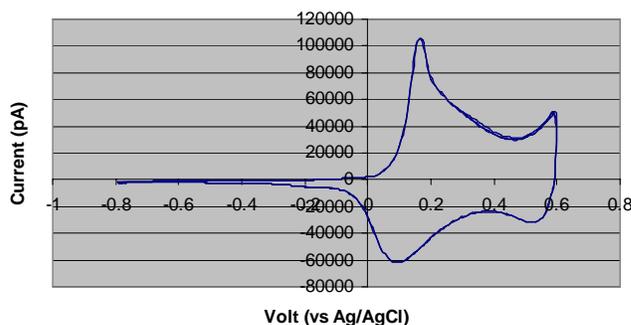


Figure 4: Cyclic voltammogram of iridium oxide deposited on the tip of a pt wire

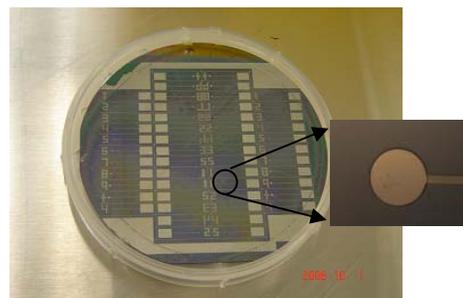


Figure 5: Test chips on a diced wafer

To characterize and compare the electrical and mechanical properties of iridium oxide deposited by various methods, test chips with a circular pad are designed and fabricated, Figure 5. Diameter of the circular pads varies from 50 μm to 1000 μm . This is to study the variation in charge injection capacity

with the surface area. Oxide deposited on the circular pads will be tested by cyclic voltametry and adhesion tests.

Future Plan for Next Two (2) Quarters

About 50 arrays that are backside diced and polished will be sent to IZM for backside metallization. Wafer scale etching process will be further characterized and optimized. Experiments will be conducted to determine the best iridium oxide deposition technique for the array geometry

III.a.2 Task 2: Development and fabrication of electronics and communications module

Description/Rationale

The electronics/communication module will be a single CMOS integrated circuit mounted on the back of the microelectrode array. Three surface-mount capacitors mounted near the chip to provide capacitance values not achievable on chip are planned. The electronics module will amplify and process neural signals, transmit this data out of the body on an RF carrier, and receive power and command data from the power coil via a transcutaneous magnetic link.

Chip Redesign Through X-FAB Semiconductor

Based on the testing results generated from our second integrated circuit (Integrated Neural Interface chip version 2.0, or INI2), we have started designing an improved chip to be sent for fabrication during the next quarter. The new design, designated INI3, will be fabricated through X-FAB Semiconductor instead of MOSIS/AMIS. The first two chips were designed using MOSIS/AMIS, but this option only allows us to get 40 pre-diced chips per fabrication run. Switching to X-FAB requires a complete re-layout and re-simulation of the chip, but for the same price as MOSIS/AMIS, X-FAB will deliver six complete 6-inch wafers containing hundreds of chips each. This will allow us to move to wafer-scale production for INIP assembly, and it also gives us many more chips for benchtop tests. We plan to use I2A Technologies to dice one or two of the wafers into bare die and package a subset of thesis in standard plastic, surface-mount packages for PCB assembly.

While the previous MOSIS/AMIS design was fabricated in a 0.6- μm CMOS technology, the X-FAB process is a 0.6- μm BiCMOS technology, meaning bipolar transistors can be fabricated along since CMOS transistors. This will allow us to design a much more efficient voltage regulator for the chip. The X-FAB process also includes a “thick metal” option, with a top metal layer having a resistance approximately five times lower than that in the MOSIS/AMIS process. This will allow us to build on-chip inductors with higher quality factors (Q), which should lower the power requirements for our FSK wireless data transmitter that had previously consumed approximately 40% of the overall system power.

Power/Command Transmitter

We previously designed and built a Class E power transmitter to drive a 2-cm coil that powers the INI chip and sends configuration commands through ASK (Amplitude Shift Keying) modulation (see Figure 6). We are now optimizing the design of the transmitter coil. We have designed and built two 24-turn “pancake” coils for improved magnetic coupling to the internal coil (see Figure 7). We built one coil using standard 22AWG (American Wire Gauge) enamel-coated magnet wire and the other using #175/48AWG litz wire. The litz wire consists of 175 individually-insulated strands of ultra-thin 48AWG wire twisted together. This arrangement lessens the skin effect, which increases the series resistance of wire at our coil operating frequency of 2.64 MHz. Using an HP 4192A Impedance Analyzer, we measured both coils. The 22AWG coil has an impedance of 15.7 μH and a Q of 81 at 2.64 MHz. The litz wire coil has an impedance of 24.4 μH and a greatly improved Q of 309 at 2.64 MHz. We are currently performing a thorough analysis of inductive power coupling efficiency that will be submitted for publication next quarter.

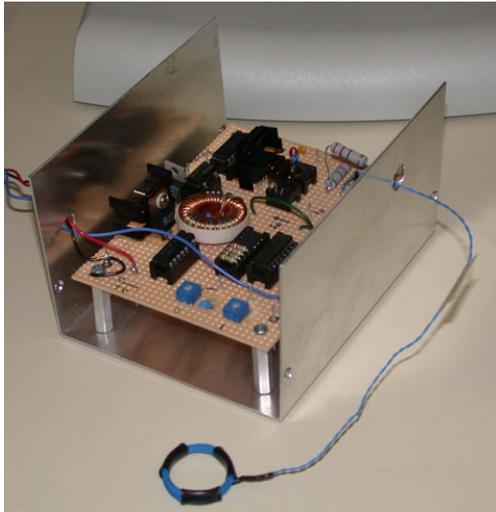


Figure 6: Photo of 2.64-MHz Class E power/command transmitter with 2-cm transmit coil.

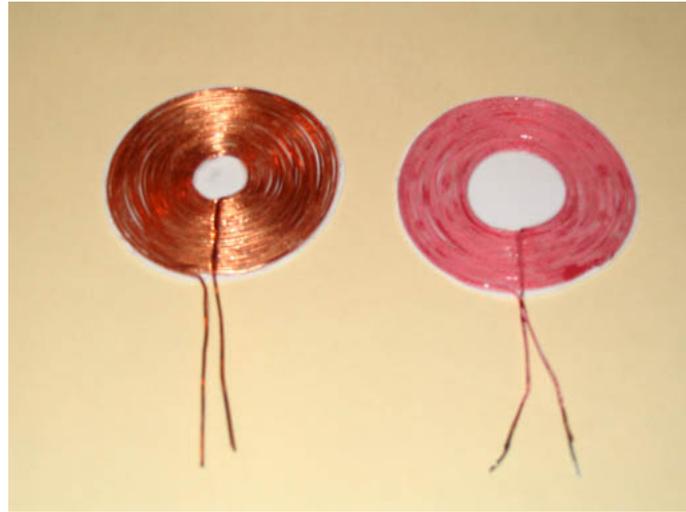


Figure 7: Improved transmit coils built from 22AWG wire (left) and #175/48AWG litz wire (right).

Future Plans for Next Two (2) Quarters

We are beginning design and simulation of the third-generator INI3 chip in the X-FAB 0.6- μm BiCMOS process. We will also be optimizing the power coils introduced above, and adapt them to work with the INI3 system. We will continue to improve the external interfaces to interact with the packaged, coated INI devices.

III.a.3 Task 3: Development and fabrication of PI coils

Description/Rationale

Coils on PI are manufactured and tested. The two layer coil with two 51-turn coils and 20 μm width as well as 15 μm spacing was selected for the assembly of the package.

Future Plans for Next Two (2) Quarters

Fully assembled functional modules will be built and powered using the PI based coils.

III.a.4 Task 4: Flip-chip bonding and assembly

Description/Rationale

The single chip AuSn bumping is finished. A new Ti/Pt/Au metallization was characterized for the bondability. Assembly tests were performed using these arrays.

Experimental Results

Au/Sn electroplating: 10 new substrates were laser machined for the AuSn electroplating of 20 functional single chips. Finally 18 functional AuSn bumped chips were provided for the assembly.

Ti/Pt/Au Metallization / Assembly: The wafer which was Ti/Pt/Au metallized at MSF, Germany, was send to the University of Utah for further processing. 9 singulated dies with glass trenches but without etched Si pins were investigated at FhG-IZM for adhesion of the under-bump-metallization (UBM). During incoming inspection scratches on the surface, damaged Au layers on the IC bonding pads as well as pads without via opening were detected. Si dummy ICs with AuSn bumps were reflow soldered applying the developed bonding process with a maximum temperature of 340°C. Shear tests were performed to get information about the shear strength and the shear mode. A mean shear force of about 2700cN was measured and three different shear modes were detected: ball shear (fracture within the bump), cratering

(damage of the UEArray) and pad lift on IC side. Figure 8 shows an array after IC shear testing. Besides AuSn reflow soldering SnCu bonding of SMD components was carried out and the interconnection was tested by shear testing. Figure 9 depicts the SMD pads of the array after shear testing and the shear mode cratering and ball shear was found. Both, the AuSn as well as the SnCu tests indicated a good adhesion on the pad metallization on the array.

In addition, cross sectioning of the array with and without bonded IC was performed (see Figure 10 and Figure 11). The SEM images of the bond pad of the array show a rough surface within the bond pad via.

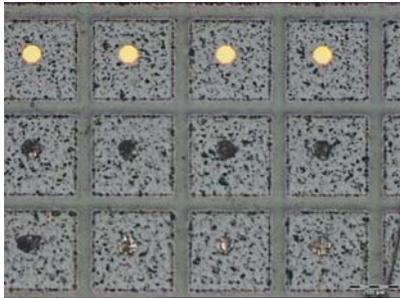


Figure 8: Light microscopy image of an array after shear testing indicating three shear modes: ball lift (on top), cratering (middle) as well as ball shear (bottom without the left bond pad which shows cratering)

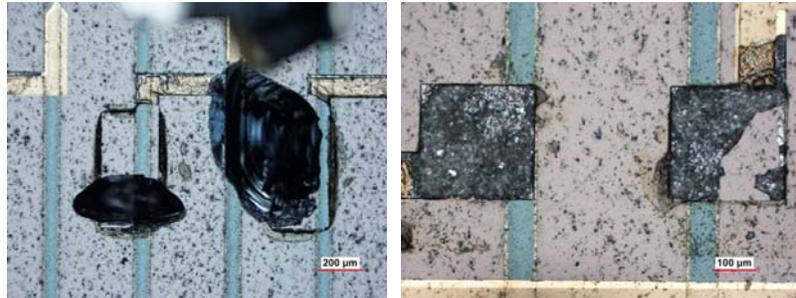


Figure 9: Light microscopy images of the array after shear testing of SnCu reflow soldered SMD components with the shear mode cratering (left) and ball shear (right)

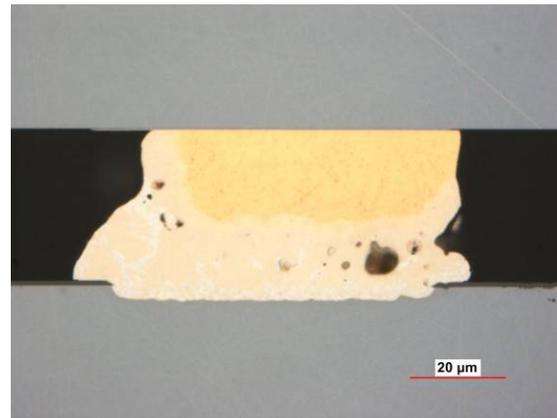
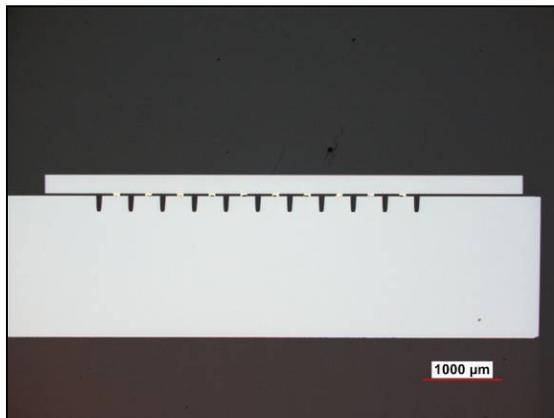


Figure 10: light microscopy images of cross sections of a bonded dummy IC on the array (left: overview, right: detailed picture of an AuSn bump)

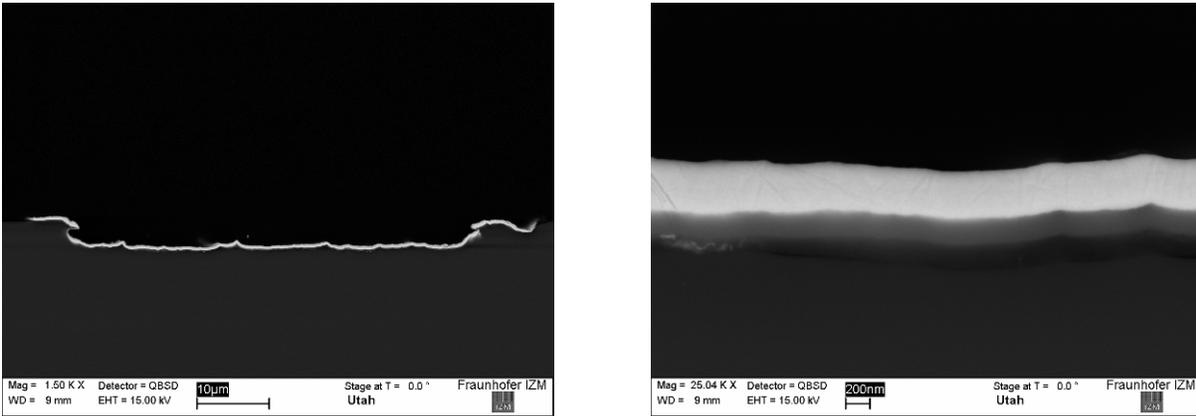


Figure 11: SEM images of the cross section of an array bond pad: left: overview with pad via and Ti/Pt/Au metallization and right: detailed picture of the metallization

Discussion/Interpretation of Results

The Ti/Pt/Au metallization was tested in detail. Compared to previous arrays a good adhesion of the UBM could be detected. The Au/Sn electroplating process for the single chip bumping is finished.

Future Plans for Next Two (2) Quarters

The University of Utah will provide about 50 arrays with pin electrodes and the new metallization. A further optimization of the bonding process of the coil/ferrite on the package will be performed. Finally functional sensor packages will be assembled.

III.a.5 Task 5.1: Hermetic encapsulation and layer coating

Description/Rationale

Various adhesion tests of silicon carbide and Parylene C as well as combinations of both materials were done in the past. The advantage of these layers is their ability to provide good encapsulation properties in physiological fluids. Especially, the required thickness to achieve a closed and pin hole free layer is very low, few 100 nm for silicon carbide and about 3 μm for Parylene C. Different types of medical grade silicones as well as epoxy resins were studied to provide extra mechanical protection. Four materials were tested for their ability to adhere and protect the integrated device: (1) Epo-Tek 310M (Epoxy Technology INC., Billerica, USA), medical approved epoxy resin (two component); (2) MED-1000 (NuSil Technology, Carpinteria, USA), medical approved silicone (one component); (3) MED-6015 (NuSil Technology, Carpinteria, USA), medical approved silicone (two component); (4) Loctite 5248 (Henkel Loctite Europe), medical approved silicone (one component, UV curing).

Experimental Results

Four materials with three different surface modifications were investigated to measure the adhesion quality on Parylene C (Figure 13-Figure 17).

For MED-6015 no significant adhesion was seen. In fact, each sample, without modification, plasma modification and Silane treatment, showed no adhesion and was very easy to peel. Parylene C treated with plasma and Silane before applying of MED-1000 showed measurable adhesion forces of about 2.17 N for plasma modification and 1.71 N for Silane treatment (average values). Epo-Tek 310M showed no relevant adhesion but it was possible to measure the peeling force which was very low between 0.38 N and 0.86 N (average value). Loctite 5248 without modification showed the same behaviour like the other materials and led to no adhesion force results. Plasma surface modification and Silane treatment of the Parylene C surface resulted in a cohesion break of the silicone film (Figure 12).



Figure 12: Loctite 5248 test sample beside peeled sample with cohesion break.

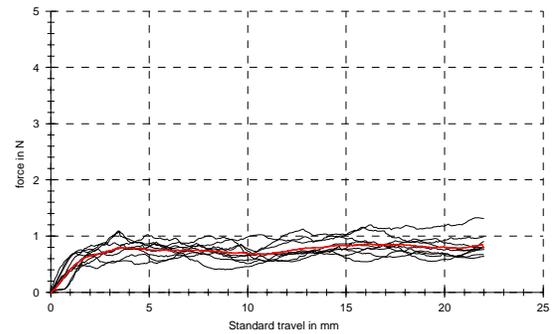


Figure 13: Peel Test result of Epo-Tek 310M (n = 10) with plasma surface modification of Parylene C.

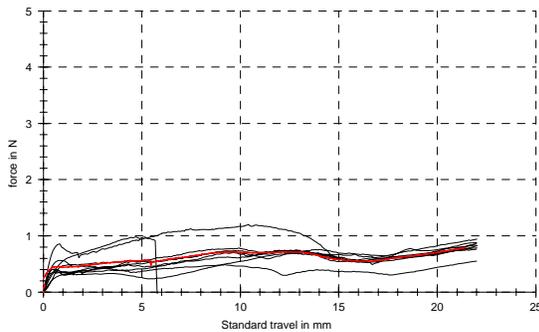


Figure 14: Peel Test result of Epo-Tek 310M (n = 10) with silane surface modification of Parylene C.

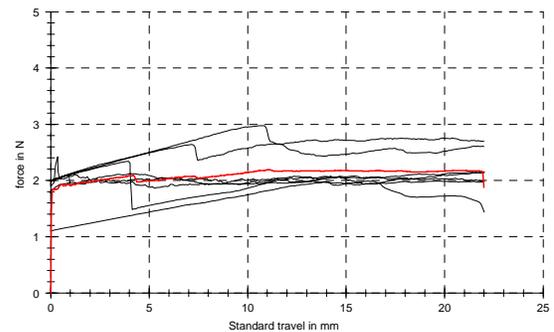


Figure 15: Peel Test result of MED-1000 (n = 7) with plasma surface modification of Parylene C.

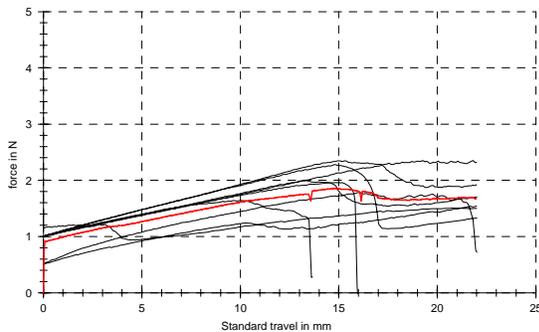


Figure 16: Peel Test result of MED-1000 (n = 9) with silane surface modification of Parylene C.

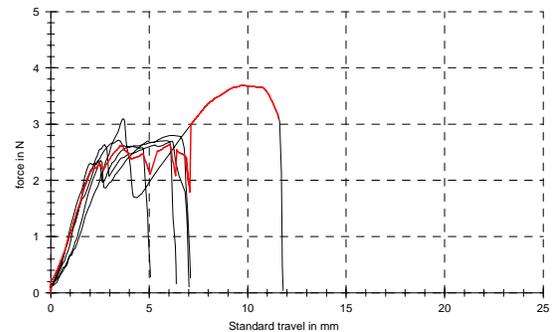


Figure 17: Peel Test result of Loctite 5248 (n = 5) with plasma surface modification of Parylene C – Film breaking.

The peel tests of Parylene C on Si showed a very good adhesion when a combination of plasma activation of the Si surface and a following application of adhesion promoter were used. During the tests the adhesion was always better than the cohesion of the film, although the annealed wafer showed some peeling on the edges of the torn off polymer film.

The adhesion force of Parylene film was higher for the wafer without annealing process (average of 2,89 for non annealed layer and average of 1,8 N for the annealed layer) in contrast to the tensile strength which was much higher for the annealed wafer (average of 51,49 N/mm² for non annealed layer and average of 66,69 N/mm² for the annealed layer).

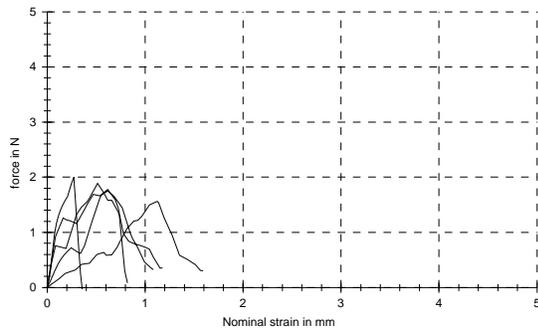


Figure 18: Stress-strain diagram of peeled off Parylene C (annealed) on Si.

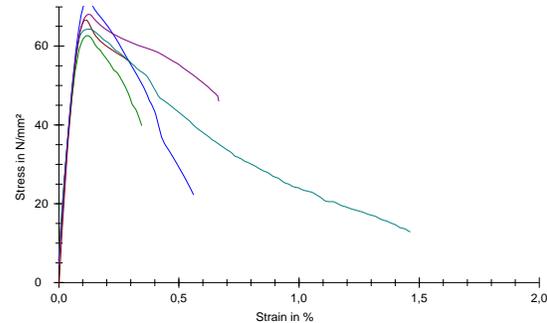


Figure 19: Tensile strength diagram of peeled Parylene C (annealed) sheets.

Discussion/Interpretation of results

The adhesion investigation of the used silicones and the epoxy resin shows the necessity of surface treatment to achieve a relevant adhesion of the used materials on Parylene C. Although, for MED-1000, MED-6015 and Epo-Tek 310M the surface treatments need an improvement. Especially MED-6015 showed no adhesion on the polymer layer. For this material some other plasma gas combinations may achieve better adhesion results in addition to the use of specified adhesion promoter.

The investigations of the last report resulted in lower adhesion values of Parylene C to Si compared with the non annealed wafer in this report. This may be a result of different coating conditions as well as minor difference in surface properties because of non optimized parameters for the first investigated samples. Determining the right balance between the adhesion force and the cohesion force of Parylene C layer requires further investigation of more annealed and non-annealed samples.

Future plans for the next (2) quarters

Investigations of medical grade silicones and epoxy resins as mechanical protection layer on Parylene C as well as Silicon Carbide will be investigated more. Especially the use of different surface treatment applications will be studied. Additional leakage current tests with suited mechanical protection layers will be done to eventually enhance the Silicon carbide / Parylene C encapsulation system.

III.a.5. Task 5.2: Parylene deinsulation

Description/rationale

For an electrode array to be able to record or stimulate, a small active site at the electrode tip needs to be exposed from the encapsulation. Thus, an oxygen plasma etching was used to remove the encapsulation material, Parylene C, from the electrode tip.

After tip deinsulation, the surface morphology of the electrode tips was inspected under SEM. Two plasma etching systems were compared for the etching uniformity study: Oxford Plasmalab80 and March Plasmod, which have anisotropic and isotropic plasma etching characteristic, respectively. For a high selectivity neuron recording or stimulation, the active electrode site needs to be confined in a small geometric area with the corresponding impedance targeting in a range of 200~400 Kohm. Aluminum foil was used as an etching mask for the tip deinsulation etching process. Array tips were poked through the Al foil, and Parylene encapsulation was removed from the exposed tip during oxygen plasma etching.

Experimental results and discussions

Etching system: It was found that on a flat substrate, Parylene can be easily removed using oxygen plasma in either Oxford Plasmalab80 system or March Plasmod, with an etching rate about 0.25~0.3 $\mu\text{m}/\text{min}$. The anisotropic characteristic of Oxford Plasmalab80 is generally preferred for most of the two dimensional wafer etching process; however, it is not suitable for the 3D geometry electrode array etching. As shown in Figure 22 that Parylene was fully removed from the plateau area of the tip, but can not be removed from the side wall of the tip. Further increasing the etching time in Oxford Plasmalab80 system can not compensate for the etching non-uniformity in 3D geometry; furthermore, this system tends to deposit unknown polymeric material on the electrode tip, which deposition was not found in a 2-D substrate etching process.

Therefore, with the 3D geometry, an isotropic etching facility is needed to fully deinsulate the tip of the electrode array. A system with inductive coupling plasma contributing to a higher reactive ion density, and without directional etching characteristic is suitable for the array tip deinsulation. March Plasmod is such a system and was used for the tip deinsulation to compare with Oxford Plasmalab80. The tip deinsulation result using two different systems was shown in Figure 21 and Figure 20, and the smooth surface in Figure 20 indicated a fully deinsulation.

Figure 23 shows an electrode tip exposed to oxygen plasma (rest of the electrode was covered with Al foil) using Oxford Plasmalab80 system, and followed by removing the Parylene from entire array using March Plasmod system. The tip (arrow A in Figure 23) was coated with unknown residue and the rest part of the electrode (arrow B in Figure 23) was cleaned after March Plasmod etching. This result indicated that the residue deposited by the Oxford Plasmalab80 while deinsulating the tip can not be removed even by isotropic oxygen plasma.

Tip exposure: For a high Signal/Noise ratio recording, the tip exposure length was estimated to be in the range of 30~50 μm . Thus, the depth of array tips being poked through Al foil need to be precisely controlled, and current technique needs to be improved to achieve the high repeatability and uniformity of the tip exposure. Al foils with various thicknesses were used to check the minimum tip exposure capability. Preliminary results showed that the thinner foil and shaper tip may be able to achieve small tip exposure requirement (<50 μm). Figure 24 shows that the tip exposure length as small as 25 μm is possible. However, the variation of tip exposure on a single array need to be further investigated in the future.

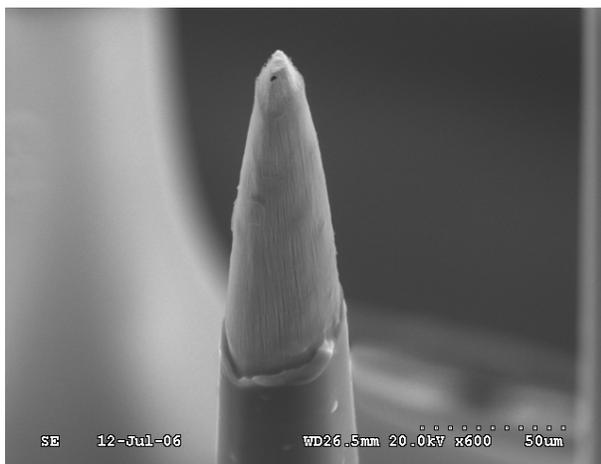


Figure 21: Electrode tip deinsulated using anisotropic plasma etching system—Oxford Plasmalab80. The tip was not cleaned even extending the etching time to double.

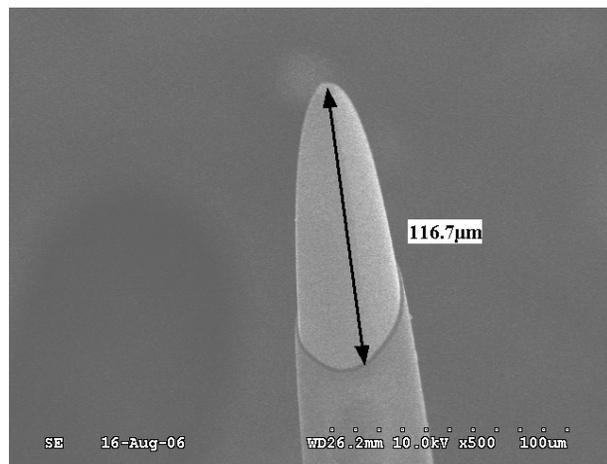


Figure 20: Electrode tip deinsulated using isotropic plasma etching system—March Plasmod

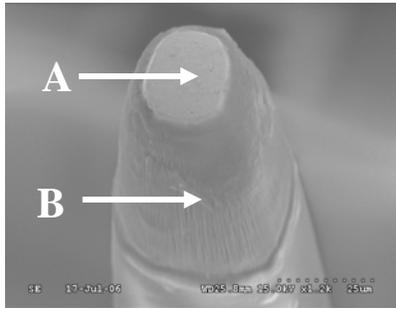


Figure 22: Anisotropic etching characteristic of Oxford Plasmalab80. The top Plateau area (A) was clear, but the side wall of the tip (B) remained coated.

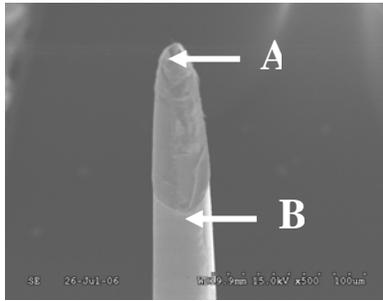


Figure 23: Residue deposited on the tip (A) during anisotropic etching process can not be removed by isotropic oxygen plasma after formed.

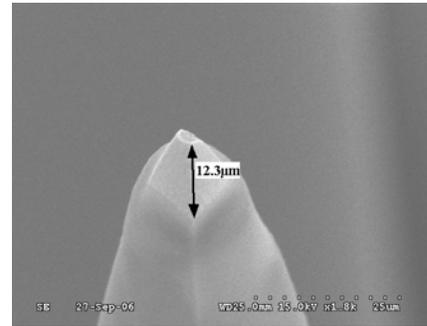


Figure 24: Small tip exposure length using Al foil with 8µm thickness. The exposure length indicated on this figure need to be multiplied by 2 due to the 30° tilt angle under SEM inspection.

Future plans for next two (2) quarters

During the next quarter we plan to investigate new methods to precisely control the tip exposure. In particular we will build a new poking station with precision control and multiple degrees of freedom. PTFE films will be tested for their encapsulation properties. We will conduct impedance spectroscopy, leakage current, adhesion, and dissolution tests on the PTFE films deposited by GVD Corp.

III.b.1. Task 6: Testing and validation of probe systems (in-vitro/in-vivo)

III.b.1.1 Bench testing of interface/electronics

We have completed benchtop testing of the INI1 and INI2 chips in previous quarters. Our tests show basic functionality in all modules. Our voltage regulator successfully converts an ac voltage on a small off-chip coil into a regulated 3.3 VDC on-chip supply. The regulator requires a minimum peak coil voltage of 5.6 V for proper power supply generation. We are currently powering the chip via a 2.64-MHz wireless link in our laboratory. Command data may be sent to the chip by amplitude-modulating the power waveform. We have sent data at a rate of 6.5 kbit/sec, although we have discovered a bug in our data receiver that leads to prohibitively high bit error rates. The source of this bug is now well understood, and this circuit will be corrected in the INI3 chip.

III.b.1.2 In-vivo testing of interface

Description/Rationale

We have evaluated the performance of the Utah wireless telemetry system by periodic recording of cortical neural activity in anesthetized cats. We have implanted Utah Electrode Arrays in or near auditory cortex of a total of three cats, and, as specified in our contract, we have telemetered neurally recorded data twice a week to an external data acquisition system of our own design. We have recorded and transmitted data successfully for about seven and half weeks. The data recorded using the wired system on July 28th was of low quality with low signal to noise ratio. There were no action potentials identified during the regular test on July 29th. This cat is alive to date with no observable behavioral problems and periodic tests are being conducted to observe any neural signals. The losses of well isolated neural units is probably the result of many factors; inflammatory responses, mechanical destruction of the neurons close to the electrodes, failure of the electrode tips. The histological studies are on going on the arrays as well as the tissue from the previous two implants.

The temperature elevation caused by an implanted Utah Electrode Array was measured in *in vivo* state. The UEA has a deposited microheater on its backside so that a specific amount of power can be dissipated

through the array. The microheater and the substrate were uniformly coated with black paint to have uniform emissivity. This UEA was implanted in the brain cortex of an anesthetized cat. An infrared camera ThermoCAM PM390 (from Inframetrics) was used to detect the surface heat distribution and a microprobe was used to track the temperature changes about 2mm near the implant in the nerve.

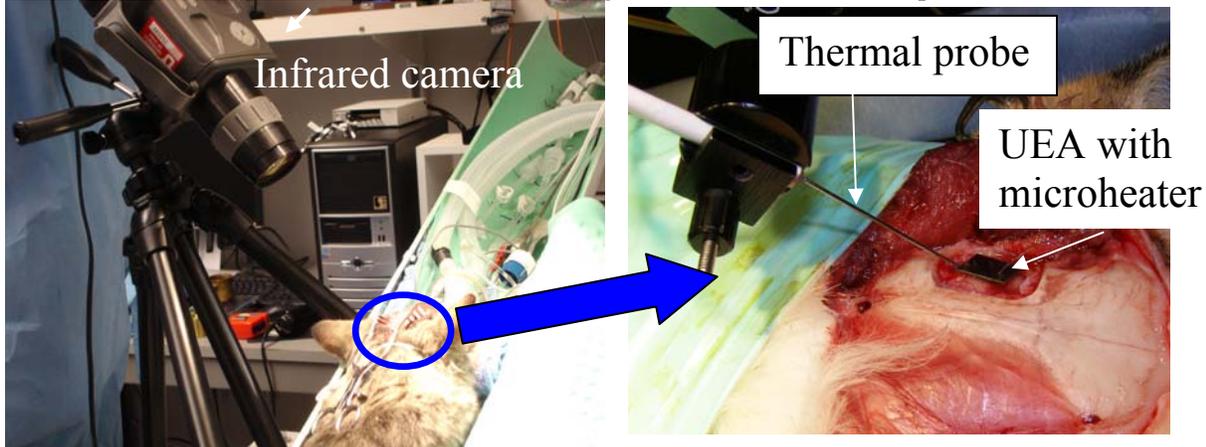


Figure 25: Experimental setup to measure the heat dissipation from the UEA with a microheater

Experimental Results

In vivo recording: The experimental setup for testing the telemetry system was described in detail in the previous report. Figure 26 shows an example of the transmitted data using our wireless system. We have shown a direct comparison between spikes recorded by our wireless system and spikes recorded by a commercial, wired recording system. The comparison showed an excellent agreement between two independent systems. Even though the number of active units has been zero since the day 52 post implantation, periodic tests are being conducted to observe any reactivated units. The testing was done only on 50 electrodes due to a frail connection on one of the two connectors although 100 electrodes (10×10 UEA) were implanted. Figure 27 shows the number of electrodes that sent distinct neural signals during the evaluation period. The number of units was determined using the T-Distribution E-M Algorithm. The number of active units since day 52 has been zero. The loss of units could be due to inflammatory responses, mechanical destruction of the neurons close to the electrodes or failure of the electrode tips.

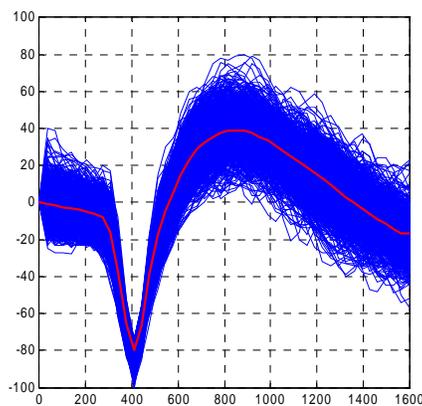


Figure 26: Spikes extracted using MATLAB algorithm from the wireless data (electrode right A9) on July 12.

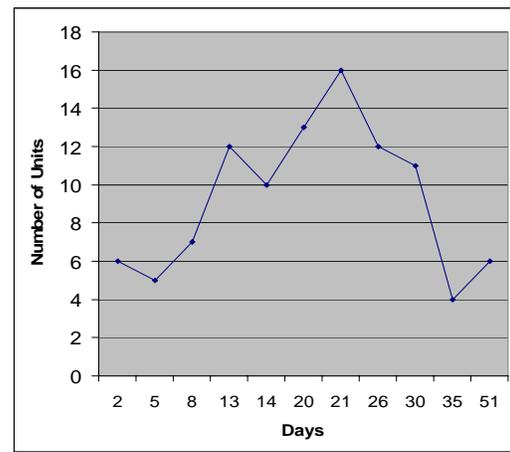


Figure 27: Number of units out of 50 electrodes that sent neural signals during the evaluation period.

Temperature increase on the array and in tissue as a function of input power: We measured the temperature change in cat's cortex where a surface coated array was implanted. The temperature was measured by using an IR thermal camera. Temperature increases on the array and in tissue just next to the array were 0.7°C and 0.4°C, respectively, for 13 mW of power. The temperature increase with the amount of power dissipation is linear, Figure 29. The thermal images of temperature change on the array and tissue according to different power levels are shown in Figure 28.

Before supplying power to the array-heater, IR camera measured 33.0°C and thermocouple measured 31.2°C. A close investigation of these two measurement methods is necessary.

Transient temperature measured by the IR camera and thermocouple: Temperature in the tissue was measured using IR camera and thermocouple. Measured results using two different methods were compared. Transient temperature changes were recorded, Figure 31.

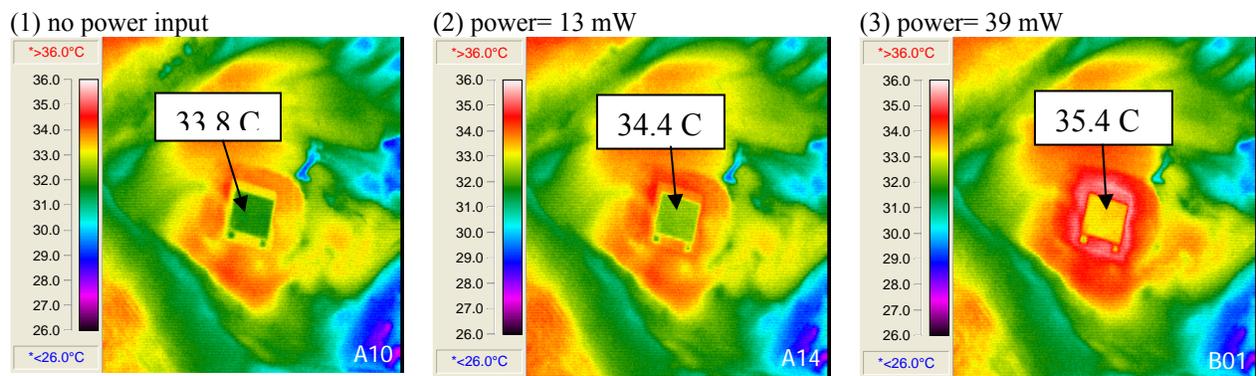


Figure 28: IR pictures of the surface of the array with a heater at different applied powers

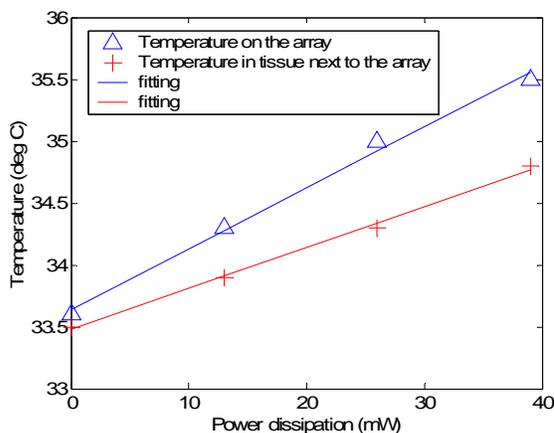


Figure 29: Increase in temperature on the surface of the heater measured with IR camera and in the tissue next to the array measured with the microprobe.

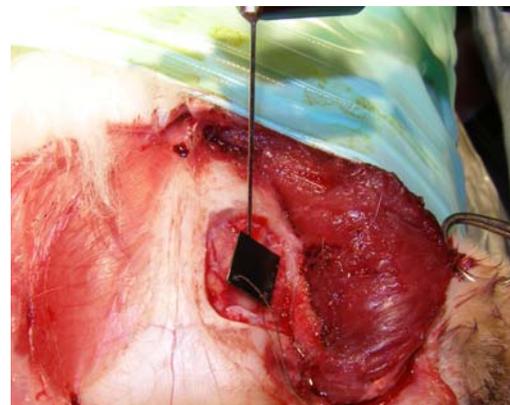


Figure 30: Experimental setup showing the thermoprobe inserted in to the tissue next to the UEA implant.

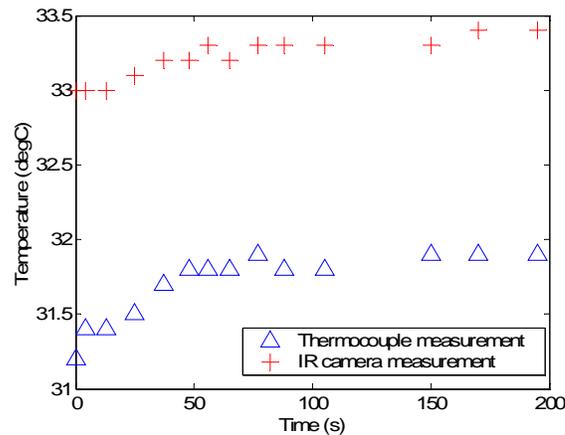


Figure 31: Transient temperature measured with IR camera and thermoprobe

Future plans for the next (2) quarters

Complete histology studies on the explanted arrays and the surrounding tissue. The preliminary results indicate less than 1 C increase in temperature in the tissue next to the implanted array. In the next quarter we plan to conduct more experiments to study the temperature changes of the tissue in the closed/covered *in vivo* state. In the initial experiments the surgical area was exposed to air. This will cause the exchange of heat with the ambience altering the array and tissue temperatures. In future experiments we will close the surgical area and measure tissue temperatures with multiple micro temperature probes.

IV. Concerns

During the 8th quarter of the project no major delays or deviations occurred. Although a sputtering system in the microfab was out of service for a month, time was well utilized by studying and improving the fabrication processes. Flip-chip bonding process has been demonstrated successfully on few more dummy chips. Experiments are designed to be able to test the working of INI chip after assembly. As of now we do not foresee any delays in the project and should move as scheduled at the beginning of phase II.

Salt Lake City, Utah, October 6th 2006

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