Multi-Channel Transcutaneous Cortical Stimulation System

Contract # N01-NS-7-2365

Final Report

Illinois Institute of Technology

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Introduction

The goal of this project was the design, fabrication, and testing of a Multi-Channel Transcutaneous Cortical Stimulation System to be used in a prototype artificial vision system. During the past 25 years, the development of a neuroprosthesis which could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This project used the combined capability four organizations, the Illinois Institute of BioElectric. formerly MicroHelix (formerly P.I. Medical). Technology, Cross Technology, and the A.E. Mann Foundation. This is the final report for this contact. For sake of completeness and consistency, some of the text contained within has appeared in previous progress reports.

Brief History of Visual Prosthesis Research Strategies

The goal of a sensory neural prosthesis is to transmit information from an artificial sensor (e.g. videocamera, microphone) to the part of the brain that normally receives such information from the corresponding biological sensor (e.g. eye, ear). For this to be effective, electrical stimulation must be applied in a well-controlled temporal-spatial pattern that mimics the pattern of cognitive neural activity normally associated with the natural sensory information. This strategy has been highly successful at restoring hearing for deaf patients, implanted with cochlear implants, who require only about 4-8 channels of information to understand speech. Restoring vision presents a considerably greater technical challenge because a much larger number, at least hundreds, of parallel channels are required. There are two places in the nervous system where it appears physically feasible to introduce dense electrode arrays: on the surface of the retina and in the visual cortex.

As early as 1918, Löwenstein and Borchardt (1918), reported that while performing an operation to remove bone fragments caused by a bullet wound, the patient's left occipital lobe was electrically stimulated, and the patient perceived flickering in the right visual field. Foerster (1929), and Krause (1924), reported similar cases of visual perception caused by electrical stimulation of visual cortex during removal an occipital epileptic focus. The significance of their studies was that they demonstrated that position of visual percepts, within the visual field, was systematically related to the area of the occipital lobe that received the stimulation. Urban (1937) inserted electrodes through an occipital burr hole 3cm above the inion and 3 cm from the midline for the purpose of ventriculography in six patients, of which one was blind. All patients perceived spacial visual sensations of various colors and shapes. Stimulation of the human visual cortex by Penfield and Rasmussen (1950) and Penfield and Jasper (1954) revealed that visual sensations, referred to as phosphenes, could be produced by electrical stimulation. In their patients, the visual sensations were described as stars, wheels, discs, spots, streaks, or lines.

The elucidation of the retinotopic map by Hubel and Wiesel (1962) in the 1960's suggested that coherent patterns of electrically elicited sensations might be possible. The first opportunity to investigate chronic stimulation of the visual cortex resulted from experiments by Brindley and Lewin, (1968) in which a 52-year old woman received an implanted stimulation system consisting of 80 platinum electrode discs. placed on the surface of the occipital pole. 80 associated trancutaneously-powered stimulators were placed over most of the surface of the right cortical hemisphere. Approximately 32 independent visual percepts were obtained, and Brindley performed mapping studies and threshold measurements. Although some attempt was made to combine the phosphenes into crude letters and shapes, the implant did not prove to be of any practical use to the subject. Another subject received a second implant in 1972 (Brindley et al., 1972; Brindley, 1973; Brindley and Rushton, 1977; Rushton and Brindley, 1977). Of the 80 implanted electrodes, and stimulators, 79 of them produced visual percepts of varied size and shape. These were meticulously mapped over 3 years, post-implant. While certainly these were pioneering experiments, little knowledge was gained about how such electrodes might be manipulated to introduce meaningful sensory information into the human brain. Dobelle (Dobelle and Mladejovsky, 1974; Dobelle et al., 1974, 1976), Pollen (1975) and others continued to investigate stimulation of the visual cortex through surface electrodes, using relatively large electrodes placed on the pia-arachnoid surface in individuals who were totally blind, following lesions of the eyes and optic nerves. Dobelle et al, implanted at least three subjects with cortical surface arrays. They also tested the ability of the implanted subjects to use the perceptions produced by the electrodes to "read visual Braille" (Dobelle et al., 1976). Reading rates were considerably less that what could be obtained by tactile Braille. Most likely, as in Brindley's subjects, the spatial visual percepts were unsuitable for combining into meaningful patterns as would be required to identify ordinary letters or symbols. An article by Dobelle in the ASAIO Journal (Dobelle, 2000), described the use of an updated computer controller used by a subject who had previously had a surface cortical array implanted. A camera, connected to an improved computer-controlled image processing system converts the image into stimulus sequences. The computer output connects to the 64-electrode array via a percutaneous connector. 21 phosphenes are obtained.

As an alternative to surface stimulation of the visual cortex, intramural and extramural studies were initiated, in the early 1970's, at the NIH, for the systematic design, development and evaluation of safe and effective means of microstimulating cortical tissue. By implanting floating microelectrodes within the visual cortex, with exposed tip sizes of the same order of magnitude as the neurons to be excited, much more selective stimulation can, in principle, be achieved, resulting in potentially more precise control of neuronal function. Studies of intracortical stimulation were initiated at Huntington Medical Research Institute (HMRI) in 1979 in which the feasibility of chronic intracortical stimulation of the sensorimotor cortex was established (Agnew *et al.*, 1986; McCreery *et al.*, 1986). These studies sought to establish margins of safety for intracortical stimulating electrodes. Brummer's (1983) development of a solid theoretical and empirical basis for chronic stimulation without inducing tissue damage eventually resulted in microelectrodes made from activated iridium.

Based upon studies by Bartlett and Doty (Barlett and Doty, 1980) and DeYoe (DeYoe, 1983)in macaques, as well as acute intracortical microstimulation studies were performed in sighted patients undergoing occipital craniotomy (Bak *et al.*, 1990), a study was planned at NIH to explore whether stable visual sensations could be produced from chronically implanted intracortical electrodes, eventually leading to a short-term implantation of intracortical electrodes in a patient-volunteer with blindness.

The initial questions to be answered by the short-term implant of the patientvolunteer were: (i) Does the visual cortex of a person, blind for a long period of time, remain responsive to intracortical microstimulation, (ii) Are the visual percepts induced through intracortical stimulation stable over months of stimulation?

The short-term implantation of the visual cortex was performed in a 42-year-old woman patient-volunteer who had been totally blind for 22 years secondary to glaucoma (Schmidt et al. 1996). Thirty-eight microelectrodes were implanted in the right visual cortex, near the occipital pole, for a period of 4 months. The electrodes were electrically accessed through percutaneous leads exiting the scalp. Confirming prior surface cortical work, 34 of the 38 electrodes initially produced spatial percepts with threshold currents in the range of 1.9 µA - 25 µA. Phosphene brightness could be modulated by varying stimulus amplitude, frequency and pulse duration. Repeated stimulation over a period of minutes produced a gradual decrease in phosphene brightness. Phosphenes did not flicker. The apparent size of phosphenes ranged from a 'pin-point' to a 'nickel' (20 mm diameter coin) held at arm's length. Phosphene size usually decreased as stimulation current was increased but increased slightly as the train length was increased. At levels of stimulation near threshold, the phosphenes were often reported as having colors. As the stimulation level was increased, the phosphenes generally became white, greyish or yellowish. Individual phosphenes appeared, perceptually, at different distances from the subject. When two phosphenes were simultaneously generated, the apparent distances of the individual phosphenes sometimes changed to make them appear at about the same distance. When three or more phosphenes were simultaneously generated, they became coplanar. Except for rare occasions, phosphenes extinguished rapidly at the termination of the stimulation train. When stimulation train lengths were increased beyond one second, phosphenes usually disappeared before the end of the train. The duration of phosphene perception could be increased by interrupting a long stimulation train with brief pauses in stimulation. Intracortical microelectrodes spaced 500 µm apart generated separate phosphenes, but microelectrodes spaced 250 µm typically did not. This two-point resolution was about five times greater than had previously been achieved with electrodes on the surface of the cortex. With some individual microelectrodes, a second, closely-spaced, phosphene was sometimes produced by increasing the stimulation current. As had been seen with cortical surface stimulation, phosphenes moved with eye movements. When up to six phosphenes were simultaneously elicited, they all moved with the same relative orientation during eye movements. All phosphenes were located in the left hemi-field with the majority above the horizontal meridian. There was a clustering of most of the phosphenes within a relatively small area of visual space. The 4-month study was concluded by following the patient-informed protocol and removing all extradural components. Two years after the completion of the study, the patientvolunteer died, unexpectedly of natural causes, unrelated to the implant. During these two years there were no observable residual complications from the implant.

The findings from all of these human studies have the following significance: It appears feasible to invoke point-topographic visual precepts using both surface and intracortical electrodes. Using intracortical electrodes, visual percepts are typically smaller than those invoked by surface electrodes, the amplitude thresholds are up to two orders of magnitude lower than those of surface electrodes, they are stable over weeks to months, and these percepts can be crudely modulated by varying the stimulation parameters.

To advance research in this field, there remains a need for reliable implantable hardware through which large numbers of intracortical electrodes can be safely stimulated for a period of years to decades. It has been the subject of this contract to develop technology useful for that purpose.

Challenges

The device specified and designed in this contract has significantly higher packaging and functional density than any other implantable neural prosthesis previously developed. The contract required the design an implantable module capable of driving 256 cortical electrodes. Four of these modules would be combined to produce a system capable of controlling and driving 1024 channels. This is approximately ten times the functional capacity of existing peripheral nerve stimulation devices.

To obtain this high packaging density we chose a modular approach to the physical configuration of the implantable system. The implant is powered transcutaneously, so no through-the-skin connectors or percutaneous wires are used. The external transmitter is comprised of a closed-loop Class-E power oscillator running suspended carrier mode. Modulation of the power carrier is accomplished by 100% modulation of the 4.48 MHz carrier.

System Organization

Each 256-channel stimulator module is comprised of four individual 64-channel Submodules. A block diagram of the 64-channel Submodule is shown in Figure 1, below.



Figure 1 – Block diagram of the 64-channel submodule

The rationale behind the use of 4 individual Submodules, each driving 64 of the 256 microelectrodes, per module, is two-fold. First, the four Submodules can be physically stacked, thus providing a more efficient use of the allowable volume than would be possible with a planar design. Second, since each Submodule is electrically and physically separate, the resulting redundancy enhances the overall system reliability. Each Submodule contains its own inductive power link, to the extra-corporeal transmitter, and each Submodule is hermetically sealed in its own ceramic package. For a 1024-channel system, a total of 16 Submodules would be used.

Within each Submodule, this concept of redundancy is retained. Since each electrode has a dedicated biphasic current driver and pulse-width timer, a failed electrode channel will typically not affect others on the same Block Chip. In the event that the failure of an individual channel is catastrophic, the power to the individual Block Chip that controls the failed channel can be disconnected by the Logic and Control Chip, thus disabling only 8 channels of the 64 within that Submodule. Electrodes can be stimulated via several different command modes.

Entire Submodules, Blocks of 8 channels, or individual channels can be addressed in one command. Alternatively all channels can be randomly accessed as desired. A hold-off feature permits "setting-up" whole groups of channels with stimulation occurring at a later time by sending a single command. True simultaneous, or complete sequential stimulation of all 1024 channels is possible. Anticipating interface with a video input, the addressing allows for the implant to be used as a type of video frame memory. For each frame, only the parameters of changing electrodes, (or pixels) would need to be altered. Using a typical mix of simultaneous and sequential stimulation it is possible to obtain a frame-rate of greater than 60 Hz.

Package Design

Packaging for the Visual Prosthesis is hermetic. Each Submodule is comprised of a 4-layer ceramic package. The thickness of each Submodule is 0.06". Stacking 4 Submodules together results in a 256-channel Module thickness of 0.24". A drawing of the 256-channel Module is shown in Figure 2, below. A sectional drawing of the module, showing the internal integrated circuits is shown in Figure 3, below.



Figure 2 – Drawing of the 256-channel implantable module



Figure 3 – Cross-section of the 256-channel implantable module

Each 64-channel submodule is comprised of 4 Macor ceramic layers. Ceramic layer #1, Figure 4, below, is used as a substrate for the integrated circuits and as the Submodule power coil. As shown in Figure 5, below, the gold-plated coil is printed on the

ceramic substrate, and is positioned within the glass-seal area. The printed spiral inductor is fabricated from thin-film deposited metal, with subsequent electroplating to a thickness of 0.001". Within the inductor are placed 8 block DAC chips, 8 thin-film anodic bias resistor chips, output capacitors, rectifier and demodulator chip, and a logic state machine chip.



Figure 4 – Floorplan of the 64-channel submodule at layer #2.



Figure 5 – Coil placement within glass seal area

The 256-channel Module includes four 64-channel connectors. These connectors are based upon the principle of "pressure sealing". An anisotropic elastomer is placed between two opposing sets of metal contacts. Using the 0-80 screws, approximately 300 psi is placed upon the elastomer. The pressure is sufficient to prevent water from condensing at the interface. Such connectors have been designed and tested by BioElectric Corp. under other NINDS contracts. Two cross-sectional views of the connector/module interface can be seen in Figures 6 and 7 below.



Figure 6 – Section #1 of 256-channel module, from Figure 4, above.



Figure 7 – Section #2 of 256-channel module, from 4, above.

A microscope photograph of the gold pads on the connector insert can be seen in Figure 8, below. The anisotropic elastomer is comprised of small gold plated filaments which act as conductors between the connector pads and the pads on the Submodule. The filaments are embedded in a silicone rubber base. Pressure on the anisotropic elastomer serves the dual purpose of forcing the filaments into contact with the pads, as well as compressing the silicone rubber. This pressure is provided by the 0.80 screws shown in Figure 4, above. A microscope photo of the interface between the connector insert and the Submodule edge, that shows the anisotropic elastomer can be seen in Figure 9, below.



Figure 8 – Microphotograph of gold pads on the ceramic connector insert.



Figure 9 – Microphotograph of interface between connector and ceramic package

The interface between the connector and the ceramic package, in an edge view, can be seen in Figure 10, below. Note the small gold filaments that can be seen between the connector and the ceramic submodule.



Figure 10 – Microphotograph of the pressure seal connector mated to the submodules.

Photographs of mechanically complete submodule packages are shown in Figure 11, and 12 below.



Figure 11 – Submodule internal construction



Figure 12 – Submodule prior to sealing of lid

Glass Seal Design

The ceramic layers are sealed together using a low-temperature glass. In Figure 13, we show the location of one of the glass-to-ceramic seals between ceramic layer #2 and ceramic layer #3. The seal is formed by depositing the glass, in the green state, on layer #2 via a syringe controlled by the X-Y-Z table. The green glass is dried at $100^{\circ}C - 150^{\circ}C$ in a convection oven. Layers #2 and #3 are pressed together, then fired in a furnace using a ramped temperature profile at a maximum of $380^{\circ}C$.

The glass must seal against the ceramic, as well as the interconnection feedthroughs. The feedthroughs are fabricated by depositing a base layer of tantalum nitride, followed by a titanium-tungsten adhesion layer, followed by the final gold top layer. The gold and titanium-tungsten are then etched away in the region of the glass seal. This concept is shown in Figure 14, below. In Figure 14, the blue areas depict the location of the tantalum nitride conductors. This approach has another electrical benefit: the tantalum nitride conductor, within the seal region, will have an electrical resistance of about 30-70 ohms. This resistance will be in series with the electrode outputs, and provides a mechanism of protection against electrostatic discharge damage.



Figure 13 – Submodule section at layer #2 showing location of the glass seal.



Figure 14 – Detail of the electrical feedthroughs showing the location of the tantalum nitride

Analytical Tests on the Glass Seals

We investigated whether the binding strength is a function of firing temperature. Samples were made by using different maximum firing temperatures and tested for tensile strength on an INSTRON test machine.

- (a). For sealing glass B-10041 (vitreous): Softening point: ~343°C, Firing Temperature: ~370°C.
 Seven different firing temperatures were tested: 330, 340, 350, 360, 370, 380, 390 °C.
- (b). For sealing glass B-10042 (crystalline): Softening point: ~336°C, Firing Temperature: ~370-400°C.
 Nine different firing temperatures were tested: 320, 330, 340, 350,360, 370, 380, 390, and 400°C.

Code	B-100041	B-100042
Туре	Vitreous	Crystalline
Softening Point	343°C	336°C
Annealing Point	289°C	281°C
Crystalline Peak	N/A	491°C
Firing Temperature	370°C	370-400°C

Our initial testing was performed using glass microscope slides. This permitted refining of the sample preparation and testing protocol. We believe that these glass slide tests are relevant to the use of the glass seal with the ceramic since SEM examination of the seals whether on glass or ceramic shows consistent cohesive failure.

Methods:

Green seal material preparation:

The glass powder is a high-purity material with an average particle size smaller than 0.1 micron. A dispensing vehicle was added to the glass powder according to a fixed weight ratio, empirically determined, in order to make a creamy paste-like mixture. The mixture was mixed for about 5 minute in an aluminum container to help break up agglomerates. The mixture was then poured into the reservoir of a 3-cc dispensing syringe.

Dispensing:

A syringe fitted with a small-gauge dispensing tube was controlled by an EFD auto air syringe system. To obtain the required controlled geometry of the seal, a numerically-controlled X-Y table was used to move the syringe over the sample.

Drying:

The green seal were examined by optical microscopy to ensure the topography of the seal track. An oven was used to dry out the moisture and the vehicle from the green seal. Any residue left in the green seal can form voids and holes inside the bulk of the seal during the firing process.

Firing:

A variety of tests were used to determine the temperature range suitable for firing the glass seal. Small glass pieces were sealed on ceramic plates using various firing temperatures. Each sample was examined with an optical microscope to determine whether crystallization had occurred. The temperature at which the glass particles began to spheroidise (due to surface tension) was taken as the lower firing temperature limit, while that where the glass pieces showed visible uniform crystallization on either the surface or in bulk was taken as the upper firing temperature limit.

Each package was fired by placing placed in a open-air atmosphere furnace and heated to 300-400 degree centigrade, with the specific temperature determined by the sample classification. The heating rate was carefully controlled to eliminate the pressure-induced blow-out effect caused by the difference of the air pressure between inside and outside of the package. The main principle of controlling the heating rate is to slow it down sufficiently so that the pressure can equalize before the temperature gets up to the softening point of the glass seal. This method helps to ventilate the air out of the package before the sealing material changes into liquid and seals. We found a heating rate around 2°C/minute to be effective. After the softening point, the heating rate was increased to about 5°C/minute until the temperature reached the desired firing temperature. All packages were kept in the furnace at the highest sintering temperature for at least 30 minutes to improve the homogeneity of the seal. The cooling procedure for all of the packages was identical: After the desired firing temperature was reached, the furnace power was turned off until the temperature of the chamber dropped close to room temperature.

Mechanical Properties Testing

Sample preparation:

After the green glass was mixed, it was dispensed on the surface of substrates. Our initial test specimens consisted of glass microscope slides and were used to refine the testing methods. Duplicate tests, using the Macor ceramic, showed no significant difference due to the similarity between the coefficient of thermal expansion of the glass slides and the Macor.

Ten straight lines (about 1 inch long and 0.02 inch wide) were deposited on the one of each pair of glass slides. The distance between each glass line was 0.04 inch. The green seal was dried and fired. Sintering temperature varied from 350°C to 400°C.

To each sealed pair of glass slides, two aluminum pull-handles were affixed using 2ton clear epoxy. The pull-handles were subsequently connected to the jaws of the tensile tester.

Tensile Test:

A tensile test, using constant strain rate, was used to evaluate the binding strength of the glass seals. All the tensile tests were carried out at room temperature on an Instron tensile machine (Model 4507). The tensile strain rate was fixed at 5x10E-2 in/min for all samples. The data we obtained from the tensile test are a series of load and displacement pairs. The maximum stress was calculated based on the raw data. To determine the relationship between the firing temperature and the binding strength, seven samples were tested for each firing temperature.

Results:

The mechanical properties requirements for the seals of the hermetic package and feedthroughs are not industry-standardized. There are a variety of implantable electronic packages, used in different applications, and each has different requirements for the mechanical properties of the seal and the package. In this project we have concentrated our efforts on determining the optimal combination of firing time and temperature that results in highest mechanical strength of the seal.

The mechanical property test results, as shown in Figure 15, indicate that the binding strength (psi) of the glass seal increases with the increasing firing temperature over the range of 355°C to 400°C. There is a significant change in maximum stress of the seal when the firing temperature goes from 360°C to 380°C, with the maximum stress increasing from about 600 psi to 900 psi. After 380°C, the maximum stress goes up slowly with increasing firing temperatue. The thin-film metalization that we intend to use on layers #1 and #2 may deteriorate if exposed to firing temperatures in excess of 400°C. Based upon this limit, our criteria for choosing the optimum firing temperature, 385°C, was made on the relationship between the mechanical properties, the metalization limit, and the firing temperature.



Figure 15 – Tensile Breaking Stress of Glass Seal in PSI

Accelerated life Testing of Glass Seals

We fabricated packages comprised of $\frac{1}{2}$ glass, and $\frac{1}{2}$ ceramic Macor. Once sealed, we then submersed them in 85-degree C saline. The glass permits us to examine the seal under microscope and look for signs of corrosion, or moisture condensation within the sealed area. A typical sample is shown in Figure 16, below:



Figure 16 – Glass/ceramic sealed samples for 85°C saline testing

Figure 17 shows an expanded view of the corner of a typical sample after 6 months in the 85°C saline. Note the complete absence of any discoloration that might suggest corrosion of the seal.



Figure 17 – Microphotograph of corners from a typical saline-soaked package.

During microscopic examination there is no evidence of moisture penetration into the sealed area. In fact, due to the sealing of the package at elevated temperature, a slight vacuum is created within the sealed area, and it is possible to see the deflection of the glass sheet. Following the 3-month hot saline exposure, the deflection still visible, indicating that there has been no gas leak of the sealed area. Below, we show a close-up view of a glass seal after 60 days exposure to 85-degree C saline.



Figure 18 – Microphotograph of a glass seal.

Note that there is no visual evidence of corrosion of the glass. We have been concerned about glass corrosion because this is a low-temperature fired glass, and typically such glasses are susceptible to corrosion.



As further evidence of the stability of the glass, the sample below is shown:

Figure 19 – Glass seal sample fabricated in 1998

The sample shown in Figure 19 was fabricated in 1998, and has been under continuous hot saline soak since that time. Although our fabrication methods were crude, we continued to test this sample because of the fortuitous necked-down region of the seal, enclosed by the circle in the figure above. Below is shown a close-up of the narrow necked-down area of the seal.



Figure 20 – Microphotograph of region encircled in Figure 19

Note the absence of visible corrosion of the glass, despite exposure to the hot saline for almost 4 years. The width of this necked-down region is approximately 1/5 that of the seals designed for the implantable package.

Helium Leak Testing

In order to further test the integrity of the glass seal, we fabricated a prototype package comprised of 4 layers of ceramic that were cut in the shape dictated by the Submodule package design. These can be seen in Figure 21, below. In the upper right of Figure 21 is shown the CAD tool drawing, from AUTOCAD, that is used as input into the numerically-controlled milling machine.



Figure 21 – Machine tool drawing shown next to fully machined ceramic sheets.

The 0.015" thick ceramic sheet is held down on the lapped tool aluminum block using paraffin. The milling machine automatically cuts the shape of all four layers, for a single package, in less than 20 minutes. Once the machining operation is completed, the ceramic is removed from the aluminum block by heating on a hot plate. The paraffin is removed from the ceramic by placing the individual cut pieces, for each layer, on the hot plate, between two layers of absorbent material while weighting down with a steel block. This blotting procedure removes almost all of the paraffin. To insure that no residual paraffin remains, the 4 pieces of ceramic are baked in a 450-degree Celsius furnace for several hours.

The glass was deposited by syringe, as described above. The deposited glass is dried by baking in an oven at 100 degrees Celsius for 24 hours. Then it is prefired at 350 degress Celsius for 2 days. This is necessary to bake off the vehicle prior to firing of the seal. The 4 layers of ceramic, with the green-state seals, are carefully loaded into a stainless steel fixture that uses weight to apply a compressive force to the ceramic layers. The fixture is then placed in the electronically-controlled furnace for the ramped firing profile. The glass is fired at 385 degrees Celsius. The ramped profile includes a dwell time, just below the firing temperature to allow pressure equalization within the package

relative to the external environment. This is important to prevent "blow-out" of the seal. A passive, ramped cool-down cycle minimizes the residual stress in the seal.

We sent a prototype package to the Mann Foundation for Helium leak testing. In this test, the package is Helium-bombed at 45 PSI. Then the residual Helium emanating from the package is measured. As a control, we used a solid piece of Macor, of approximately the same dimensions as the prototype package. The results from this test are shown below. Note that there is little difference between the solid "blank" Macor piece and the sealed 4-layer package. However, both of these specimens had residual Helium levels that were significantly above the background level. This is disturbing and we investigated this phenomena.

Package type			
Blank Macor	6 x 10 ⁻⁸	1 x 10 ⁻⁹	
Sealed	1 x 10 ⁻⁷	4 x 10 ⁻⁹	
Helium bomb = 45 psi Background = 10 ⁻¹¹		cc-atm	/sec

Since the Macor is a composite material, we hypothesized that it might contain micro-crevices that could trap Helium beneath the surface. We imaged the solid Macor



Figure 22 – SEM photograph of the surface of the Macor

in the SEM to examine the size and character of the micro-crevices. Figure 22, above shows the surface of the Macor. Indeed the irregular topology and the crevices can be seen. However, the size of these crevices is well below the width of the glass seal. The glass seal is approximately 750 microns wide, whereas the average size of the crevices shown in Figure 22 is 10 microns. We then investigated whether the glass melts into the crevices at the interface between the glass and ceramic. Figures 23, 24, 25, and 26, show varying magnifications of the cross section between two ceramic sheets, and the glass seal.



Figure 23 – Interface between two Macor sheets and the Glass seal (500x)



Figure 24– Interface between two Macor sheets and the Glass seal (900x)



Figure 25 – Interface between upper Macor sheet and the Glass seal (1500x)



Figure 26 – Interface between lower Macor sheet and the Glass seal (1500x)

As can be seen in the SEM photos above, there is excellent integration between the glass and ceramic. This leads us to believe that the residual Helium seen in the Helium bomb test is an artifact of the measurement method and does not represent a leakage of the sealed package. We remain committed to our theory that the measurements of the Helium Leak test are not representative of the seal integrity, but rather are an artifact caused by the surface morphology of the Macor. In this regard, our extended testing in the hot Saline, is persuasive.

We intend to do a direct measurement of water penetration into a sealed package by using impedance spectroscopy on traces buried within the cavity of the package. We are preparing special metallization patterns that will be electrically accessible by the package feedthroughs.

Transmitter Design

The basic topology of the Class-E oscillator is shown in Figure 27, below. The combination of the series capacitor, the shunt capacitor, and the transmitter coil form a multifrequency network. The impedance vs frequency plot of the multifrequency network shows a double resonance: one a series resonant frequency, and one at a parallel

resonant frequency. Between these two frequencies can be found the Class-E frequency. At this special frequency, the loss in the switching element of the converter becomes very low. The switch, across the shunt capacitor is turned on at a strategic point in the resonant cycle for which the switch voltage, and the derivative of the switch voltage are zero. Using a closed current-mode loop control maintains operation of the converter at the precise Class-E frequency. Operation and typical waveforms of a closed-loop Class-E converter can be



seen in Figure 28, below. Note that when the gate of the FET is turned on, the FET drain voltage is at the negative crest of the sinusoid. This point corresponds to the coil-current zero crossing. Since the FET is only turned on for a brief portion of the cycle, FET losses can be very low.



Figure 28 - Operation and typical waveforms for a closed-loop Class-E converter

We use a specially-designed spreadsheet that calculates the value of the shunt and series capacitor given the desired values of the coil inductance, coil Q, power supply voltage, the frequency of operation and the peak coil current. An example of this spreadsheet, for a 5MHz, 0.5 Amp, converter operating off of 12 volts is shown in Figure 29, below.

Close	ed Loop			
N.A 143				
Mult	frequency	Converte	er	
Desi	an Sheet			
INPUT Vdc	12	D	f(D)	f'(D)
INPUT L in henrys	2.00E-06	0.2	0.118503	1.360654
INPUT I peak in amps	0.5	0.112907	0.024321	0.783094
INPUT f in hertz	5.00E+ 06	0.08185	0.003459	0.560178
INPUT Coil Q	78	0.075676	0.000137	0.515912
w = 2*pi*f	3.14159E+ 07	0.075411	2.51E-07	0.514015
XL = WL	6.28319E+ 01	0.07541	8.56E-13	0.514012
R = XL/Q	8.05537E-01	0.07541	0	0.514012
$Idc = (I^2 R)/(2^*Vdc)$	0.010714476	0.07541	0	0.514012
C.R. = Idc/I	0.018963674	0.07541	0	0.514012
D	0.075410349	fseries	3949175	
Vp = (2*Vdc)/(1-D)	2.59575E+ 01	fparallel	5010812	
re(a)	-6.49412514	fp/fs	1.268825	
im(a)	-1.5679587	V(C2)	19.59849	
mag(Vs')	13.36146037	V(L2)	31.41593	
Zs = Vs'/I	2.36486E+ 01	Output va	Output values	
$Xs = (Zs^2 - R^2)^{.5}$	2.36349E+ 01	Cseries=	8.12E-10	farads
C2 = 1/(w(XL-Xs))	8.12078E-10			
re(b)	0.118402325	Cshunt=	1.33E-09	farads
im(b)	-0.25312442			
Ic'	0.55889563	"ON" time	0.02	uSec
$C1 = \frac{1c'}{(w^* \vee s')}$	1.33146E-09	DC current	0.01	amps

Figure 29 – Format of the spreadsheet used to design the closed-loop Class-E converters

In the spreadsheet, the values in the yellow-highlighted block are inputs. The values of the series capacitor, Cseries, and the shunt capacitor, Cshunt, are outputs. Other important parameters that the spreadsheet calculates are: the power supply current, the switch on-time, the series and parallel frequencies, and the peak coil voltages.

To modulate the transmitter, we are using the suspended-carrier method. Implementation of this technique can be seen in Figure 30, below. Note that a second switch is inserted in series with the transmitter coil. During the normal resonant cycle, the suspended-carrier switch is left closed. For this normal operation the energy moves back and forth between the shunt and series capacitors, and the coil. When all of the energy is stored on the two capacitors, and the inductor current crosses zero, the

suspended carrier switch can be opened. To prevent discharge of the capacitors a diode is placed in series with the power supply and the Class-E converter switch is left open. The charge can be stored on the capacitor for an extended period of time with little to no decay. In this manner, the converter coil current can be made to change from the normal peak value to zero within a fraction of a cycle, and the converter can remain "suspended" in this state for as many equivalent as desired. Oscilloscope cycles waveforms taken from the 5MHz Class-E converter can be seen in Figure 31. In the top part of Figure 31 below.



simulation waveforms from a PSpice simulation are shown. In the lower half of Figure 30 an oscilloscope photograph can be seen. Note that the converter current quickly returns pack to the level that is was at prior to the suspension of the carrier.

It can also be seen, in Figure 30, that the current does not immediately cease, as theory would predict. Rather, there is a transient ring-out that occurs each time the suspended-carrier switch is opened. The cause of this can be seen in a revised model shown in Figure 31, below.



500 nsec/div

Figure 30 – Simulation and Oscilloscope waveforms for the suspended-carrier transmitter



Figure 31 – Modified suspended-carrier model showing addition of the switch capacitance.

The suspended-carrier switch is not ideal. Rather it is implemented using a power FET. In order to obtain a low on-resistance, it is desirable to use a large area FET. However, a large area FET also is characterized by a large capacitance. When the switch is opened, this capacitance must be charged. For this to happen, current flows through the inductor transferring energy from the series capacitor to the suspended-carrier switch capacitor. Analysis of the circuit during the charging of this switch capacitance shows that the circuit would continue to ring at a new higher frequency determined by the value of the switch capacitance. Although not shown in Figure 31, it is necessary to use a snubber network across the suspended-carrier switch in order to cause the higher-frequency ringing to damp out. Of course some energy is lost when the switch is turned back on, while resuming normal operation. This is the cause of the first cycle of the resumed current being slightly lower than the steady state peak current value.

The energy lost during the charging and discharging of the suspended-carrier switch can be minimized by choosing an FET with a capacitance that is significantly lower than that of the series capacitor. However, high-voltage, low-resistance, FETS are also characterized by high-capacitances, thus resulting in a design compromise. This is a fundamental limitation of the suspended-carrier method.

ASIC Design

Three different ASICs were developed for use in the 64-channel Submodle. Their function is illustrated in Figure 32, and the ASICs are pictured in Figure 33, below.



Figure 32 – Block Diagram of Submodule showing 3 types of ASICs



Figure 33 – Microphotographs of the ASICs used in the 64-channel Submodule

The Rectifier/Data demodulator ASIC's function is to rectify the stimulator's coil voltage, establish a band-gap reference and biasing for the data demodulator, clock recovery, and power supplies, recover a clock from the stimulator's coil voltage, demodulate the suspended-carrier data, provide a digital data stream and associated control signals to the State-Machine Controller. The State-Machine Controller takes the data stream from the Rectifier/Data demodulator ASIC and decodes the mode, and address of the desired electrodes channel. The stimulus parameters for the desired channel are routed to the appropriate BLOCKCHIP. Within the BLOCKCHIP, the

output of the State-Machine Controller is loaded into a serial shift register. The register is dumped into the addressed channel on the leading edge of a BLOCKCHIP latch enable.

Rectifer/Data Demodulator ASIC

Figure 34 shows a microphotograph of the Rectifier/Data demodulator ASIC and identifies the location of the major circuit blocks.



Figure 34 - microphotograph of the Rectifier/Data demodulator ASIC

Figure 35, below, shows a schematic of the rectifier bridge, clock recovery, and data demodulator current sensor. Operation of the circuit is as follows. The coil voltage is rectified by the upper and lower rectifiers in a standard switched-FET bridge. What is unique about this design is the use of a floating n-well to fabricate the p-type upper rectifiers. This is required to avoid turning on the parasitic bipolar junction transistors when the coil voltage rises above the power supply rails. The rectified voltage on HV is used in the band-gap reference to create biases for the clock recovery and rectifier current sensors. The clock recovery circuits operate as two high-speed comparators that switch when the coil voltage exceeds the substrate (circuit ground). Both nodes of the floating coil are sensed, creating two anti-phase clock signals, ACLK and BCLK. These clock signals are the master clocks used for all logic in the rest of the system.



Figure 35 - Schematic of the rectifier bridge, clock recovery, and data demodulator.

The implant coil voltage cannot be used as a high-speed demodulation signal because when the carrier is suspended the rectifier current drops to zero. When that happens the Q of the coil rises to a value that is much higher than when the rectifiers conduct. Consequently the unloaded coil shows little to no further reduction in terminal voltage because when unloaded the loss in the coil resonant circuit is very low. However, the rectifier current can be used as a reliable measure of when the transmitter carrier is turned on or turned off. This is accomplished in the rectifier current sensors. The current in the upper rectification p-type FETs is mirrored to a high-gain comparator circuit. On each peak of the sinusoidal current, presence of rectifier conduction is converted to a digital pulse whose width is equal to the conduction time of the rectifiers.



Figure 36 – Waveforms associated with suspended-carrier data demodulation and clock recovery

Figure 36, above, shows the outputs of one side of the demodulators and clock recovery circuits. Note that transmitter current is sensed on the peaks of the transmitter current when the transmitter is turned on. Typically the first cycle following a suspension of the transmitter is not sensed. This is due to the need to build up energy within the stimulator coil so that the coil's terminal voltage can once again exceed the power supply and rectification can resume. Also it can be seen that the clock recovery continues even during the suspended cycle. This is a direct consequence of the high voltage gain of the clock recovery circuit.

State Machine Controller

The State Machine controller accepts digital inputs from the Rectifier/Data Demodulator ASIC, and Decodes the electrode stimulus commands. The State Machine then sends the appropriate data stream to the BlockChips for further processing.

The design of the State Machine Controller was done entirely in VHDL. The code was simulated on the MAXPLUS2 PC-based software package. Synthesis of the netlist was performed by SYNOPSYS. A custom interface driver was used to create a TANNER netlist for logic place and routing. A microphotograph of the completed State Machine ASIC is shown in Figure 37, below.



Figure 37 – State Machine Controller ASIC

Description of the Eight Channel Stimulator BLOCKCHIP

The BLOCKCHIP provides 8 channels of integrated biphasic stimulation capability. Each Channel consists of a 7 bit current output DAC and a 4-bit timer circuit. The DAC produces the stimulation current while the timer controls the biphasic pulse duration. In addition, a Polarity bit determines the starting polarity of the biphasic pulse, and a Holdoff bit determines whether or not stimulation will begin immediately after data is transferred to the Channel.



The chip architecture is shown in the above diagram. Incoming data is clocked into the shift register left to right. After all data bits have been clocked in, LE is asserted, and steered to the channel selected by the Mux, which causes the leftmost 13 bits of the shift register to be transferred into the 13 bit latch in the selected channel.

Pin Description:

GND 0V reference for the logic, and power return and substrate connection for the chip.

HV 10V max. Powers the DAC circuitry and output current drivers.

LV 5V max. Powers the shift register, latches, timer and logic in the chip

Indif This is the reference terminal for the lout current outputs. This would typically be held midway between HV and GND by an external voltage. It could be connected to LV as well.

Iout These are the stimulation current outputs. The current may be set from 0.5uA to 64uA in 0.5uA increments. The device will always produce symmetric biphasic pulses, i.e. a pulse of 30uA source current will be followed immediately and automatically by a pulse of 30uA sink current of identical duration. After both halves of the biphasic pulse have been completed, Iout will either source or sink a maximum of 0.5uA as required to reduce the voltage between the Iout terminal and the INDIF terminal to 0V. As Iout approaches INDIF, this "balancing" current is proportionally reduced to zero. This "balancing current" is intended to remove any residual voltage on the Iout terminal caused by any imbalance in the source and sink phases of the biphasic pulse.

RESB A low logic level on RESB will reset the timer and state machine logic of all the channels, thereby immediately terminating any stimulation pulses currently in process. RESB does not affect the contents of the latches or shift register. This line is intended to be held low during system power up to prevent spurious stimulation.

TCLK This is the timebase for the timers in the channels. It may be asynchronous with DCK. Simulation shows the maximum TCK rate to be around 4MHz. The timers may be programmed from 0001binary to 0000binary, thereby giving pulses with widths from 1 to 16 units of time. This is the width of one half of the biphasic pulse. TCK is divided by 16 to produce the width step size, e.g if TCK=1MHz, a timer setting of 0001binary will produce a positive current pulse 16uS long immediately followed by a negative current pulse 16uS long.

DIN This is the Data input to the shift register.

DCK This is the clock input to the shift register. According to simulation, DCK can run to about 4MHz. The logic level on DIN is clocked into the shift register on the rising edge of DCK.

LE The rising edge of LE sets a flip-flop. On the next rising edge of TCK, the 13 bit data latch of the selected channel loads the data from the shift register. The channel is selected by the Muc, which takes as the channel address the rightmost three bits contained within the shift register. To insure a proper data load into the proper channel, the shift register contents must be stable until after the first rising edge of TCK after the rising edge of LE.

SIM The rising edge of SIM sets a flip-flop. On the next rising edge of TCK, any channel in the block chip which has in its 13 bit register its Holdoff bit (H) set will emit a stimulation pulse according to the parameters stored in it's 13 bit latch. This way, any number of channels in the block chip may be made to stimulate simultaneously.

Data Description

AD2, AD1, AD0

The channel address, 0 to 7 (000b to 111b) determines in which channel the pulse parameters will be stored after the next LE pulse.

A6 through A0

Stimulation amplitude, 128 steps in 0.5uA increments (0uA to 63.5uA). A value of 0000000b results in no stimulation pulse. Also, with a programmed amplitude value of 0, the timer is never started, so that channel may be immediately reprogrammed and stimulated without having to wait for the channel timer to complete its cycle.

T3 through T0

Pulse width. This is the width of one half the biphasic pulse. The time increment is 16 times the period of TCK. The shortest time is when T3,T2,T1,T0 = 0001b, the next shortest is 0010b, all the way up to 0000b, which produces a pulse of 16 times the shortest pulse. Once the timer starts counting and the channel is producing the specified pulse, further attempts to load data to the 13 bit latch within that channel are inhibited until the timer completes its entire cycle, or the RESB line is brought low to reset the timers and logic in all channels on the chip.

P The Polarity bit. If set to one, the biphasic pulse will start with Iout sourcing current. If 0, the pulse will start with Iout sinking current.

H The Holdoff bit. If set to 0, stimulation will begin on the next rising edge of TCK after the rising edge of LE. If set to 1, stimulation will not begin until the next rising edge of TCK after SIM is asserted. In other words, a channel will stimulate as soon as the data is loaded into the channel unless the Holdoff bit is set.

Typical Timing, Holdoff bit not set



tsu1= The minimum time data must be present on DIN before the occurrence of the rising edge of DCK.

This time will be approximately 200nS.

tsu2= The minimum time between the clocking in of the last data bit and the rising edge of LE.

This time will also be approximately 200nS.

tsu3= The minimum time between the rising edge of LE and the rising edge of TCK. This time will also be approximately 200nS, however since TCK may be asynchronous with LE, if tsu3 is not met, stimulation will begin normally on the next rising edge of TCK.

pwmin= The minimum LE pulse width is approximately 100nS.

The above times depend on the LV logic supply voltage. As was stated earlier, the chip operates properly in simulation with a 4MHz DCK.

Specific Timing

In the implant, all internal clock frequencies will be derived from the excitation carrier frequency. The internal dividers in the implant and the exact carrier frequency will be chosen to insure the timing requirement of 50uS pulse time increments will be met, and the data transfer rate is sufficiently high to support the required update rates. Although the block chip places no restrictions on any synchronization between DCK and TCK, these rates will ultimately be derived from the carrier frequency. In the implant, the timing will be as follows:

TCK must be 320,000.00Hz to produce pulse width time increments of 50uS.

The carrier frequency will be 14*TCK = 4.480MHz

Using 4 carrier cycles/Bit for the data modulation, the DIN data stream will come in at 1.120MBPS, DCK will therefore be 1.120 MHz

Depending upon the dynamics of our magnetic link, it may be possible to double the data transfer rate by using only 2 carrier cycles/bit for our data modulation. In this case, DIN and DCK will double to 2.240MHz.

Blockchip Electrical Design



Figure 38 – Microphotograph of the Blockchip



Figure 39. Block diagram of the BLOCK3 ASIC



Figure 40. Schematic of the Data Shift Register Block

A Block diagram of the BLOCK3 ASIC is shown in Figure 39, above, and a schematic of the Data Shift Register Block is shown in Figure 40, above.

The data input to the BLOCK3 ASIC is on the serial data line DIN. At each Data Clock cycle, on line DCK, the serial input data is shifted over, to the left, in the 16-bit shift register, with the most significant bit, #16, on the left. Bits 14, 15, and 16 determine which of the 8 DAC output stages are addressed. The address decoder, on the extreme left of the schematic decodes bits 14-16 so that on the rising edge of the Address Latch, LE, the appropriate DAC address line is set to a 1. The remainder of the bits, 1-13, are encoded as follows:

Bit	Description
#	
1	Bit H – 1=holdoff stimulation until the leading edge of the Stimulation Command
2	Polarity of the first phase of the stimulation -1 =anodic
3	Least significant bit, T0, of the pulse-width timer – 50usec
4	Bit T1 of the pulse-width timer
5	Bit T2 of the pulse-width timer
6	Most significant bit, T3, of the pulse-width timer – Maximum pulse-
	width=750usec
7	Least significant bit, A0, of the current amplitude -0.5 uA
8	Bit A1 of the current amplitude
9	Bit A2 of the current amplitude
10	Bit A3 of the current amplitude
11	Bit A4 of the current amplitude
12	Bit A5 of the current amplitude
13	Most significant bit of the current amplitude $-$ Maximum current $= 64$ uA

Once all the data are valid in the shift register, LE, is asserted which transfers the contents of the shift register data bits, 1-13, to the appropriate Channel Output Stage. Within the Channel Output Stage is control logic that activates the pulse-width timer, based on the T0-T3 pulse-width bits. The control logic also creates the biphasic timing to insure that the anodic and cathodic phases of the biphasic waveform are identical. And, the control logic locks out further commands until the stimulus pulse is completed.

In Figure 41, below, the schematic of the Bias Reference Generator is shown. This circuit generates the gate voltages for all of the current mirrors in the Channel Output Stages. One common reference is used for all 8 of the output stages to conserve power and insure uniformity between the output stages. A band-gap generator is shown on the extreme left. Gate voltages of the p-type cascodes are mirrored over to the right remaining stages and establish the gate voltages of the 3 least significant bits, AO - A2, in the Channel Output Stages. The reference current for these bits is 0.5uA. The balance of the Bias Generator creates gate reference voltages for 8 times the least significant bit current. These gate voltages establish the gate voltages of the current mirrors used for bits A3 - A6 in the Channel Output Stages. The voltage drop across each of the of the current mirrors, used Bias Reference Generator are controlled by a high-gain amplifier feedback loop, and set to be approximately 0.3 volts. Within the Channel Output Stages, identical amplifiers set the same voltage drop across the current mirrors used to covert the bits A0 - A6 into balanced biphasic output currents. This is necessary to insure that the



mirrors in the Channel Output Stages are set to the same current as those in the Bias Reference Generator, while allowing for output electrode voltages within 0.3 volts of the power supply rails.

Figure 41. Schematic of the Bias Reference Generator

A schematic of the Channel Output Stage is shown in Figure 42, below. The Gate Voltages from the Bias Reference Generator connect to the Current Source Mirrors. They are divided into two groups consisting of A0 - A2, and A3 - A6 This is done to reduce the number of parallel transistors that would be needed in order to produce the scaling of the bits. If two groups were not used, then bit A6 would have to have 128 times the number of parallel transistors that bit A0 uses. With the groups, bit A6 only needs 8 times the number of parallel transistors used by bit A0, because the gate

reference voltages for the A3 - A6 bits is generated by a current mirror that is 8 times the value of that used for the bits A0 - A2 (in the Bias Reference Generator).

The Current Source Mirrors connect directly, in series with the output transistors. The voltage drop on the Current Source Mirrors is controlled by the Voltage Drop Regulating Feed-back Amplifiers. These amplifiers, and their bias point, matches those in the Bias Reference Generator. The amplifiers use extra-large transistors, 30u x 30u, in order to desensitize them to variations in photolithography.

The Balance Regulator is enabled between stimulation pulses and maintains the value of the voltage at the electrode output of the Channel Output Stage close to the value of the indifferent electrode. This is to insure that the implant output charge coupling capacitor does not charge up during the interpulse interval. Charging would take place due to infinitesimal leakage currents from the Channel Output Stage.



Figure 42 – Schematic of Blockchip Electrode Drive. 8 Drivers/chip

In series with each current mirror is a switch that is controlled by the bit inputs to the circuit. All of the current mirrors, for the Source and Sink drivers, respectively, have their drains connected to a common point. This common point is connected to the source of the respective Source and Sink output transistors. The voltage at these common nodes is controlled by a feedback amplifier, that matches the drain voltage of the all of the current mirrors to that in the bias reference generator circuit. This is accomplished by controlling the gate voltages on the output transistors. In this manner, the combination of the current mirrors and the output transistors form a cascode circuit. Using a cascode corrects for the non-flat characteristic curves of the output transistors. The common node is regulated to a voltage that is approximately 0.5 volts away from the respective power supplies. This provides an extremely wide compliance voltage range with almost flat Source and Sink current curves, with varying electrode voltage.

In spite of the success of these circuit topologies we were left with some residual non-balance between the anodic and cathodic phases of the biphasic current waveform. This imbalance can be seen in the plot of Figure 43, below.



Figure 43 – Left: Residual imbalance in biphasic current. Right: New topology corrects the imbalance.

The residual current, for the Sink drivers was caused by impact ionization current that the cascode circuit was unable to correct. It must be that this current is substrate current, otherwise the cascode circuit would have corrected it. In Figure 44, below, a diagram of an ideal FET and channel are shown. Note that the channel profile linearly changes from the source to the drain of the transistor.



Figure 44 – Ideal channel profile for an FET.

In Figure 45, below, the impact ionization effect is shown. Increased voltage on the drain (shown on the right N region), causes shortening of the channel due to a depletion region around the drain. As the carriers leave the channel they complete the path to the drain by means of drift mechanism. As the channel shortens, the velocity of the carriers increases. As they leave the channel, the carriers impact into the crystal lattice and cause the creation of pairs within the substrate. This current becomes base current for the lateral NPN bipolar transistor. It is this current that results in the impact ionization current.



Figure 45 – Diagram showing impact ionization current effect.

The consequence of this current are the non-ideal characteristic curves shown in Figure 46 below.



Figure 46 – Non-ideal characteristic curves due to impact ionization. Problematic current is circled in red.

We implemented an extended drain transistor for the output transistors to correct for the residual imbalance. The extended drain transistor uses a diffusion around the drain to smooth out the electric field in the vicinity of the channel. This dramatically reduces the impact ionization effect. In Figure 43, above, one can see the improved performance in the right-hand plot.

Electrical Testing of the Combined System

These three ASICs were packaged, individually in 40-pin ceramic dip carriers. They were interconnected by means of wires on a protoboard. A prototype implant coil was connected to the Rectifier/Data Demodulator ASIC. A 5MHz suspended carrier transmitter was connected to a PC. A Labview module was written to command the transmitter in order that the appropriate data stream could be sent, over the inductive link, to the Rectifier/Data Demodulator ASIC.

Commands were issued, via the PC, to the transmitter. The output of the BLOCKCHIP was observed on a multichannel oscilloscope as the stimulus parameters were adjusted. All channels appropriately responded to the computer commands. Two versions of the State-Machine Controller were tested: one that used parity checking, and one that did not. It was interesting to see that there were no observed errors in the stimulus outputs when using the non-parity checking ASIC. It is likely that there may have been intermittent cycles of error, that did not show up on the repetitive oscilloscope waveforms. The initial prototype of the parity-checking version of the State-Machine Controller had a design flaw. This was corrected in a subsequent fabrication run, and the latest version of this ASIC functions as expected.

Complete details of the communication protocol for the 256-implantable stimulator can be found in the Excel spreadsheet attached to this report. In summary, data modulation for the 256-channel stimulator is as follows: The beginning of a command is marked by leaving the transmitter turned on for 610 cycles followed by the suspension of the transmitter for 2 cycles. This is called a TAG sequence. Dedicated digital circuitry detects this unique TAG condition and synchronizes the data clock, at the output of the Rectifier/ Data demodulator ASIC with that in the transmitter controller. Synchronization of the data clock allows for alignment between the bit edge detection in the stimulator and the bit edge generation in the transmitter. Following the TAG data is encoded by using 4 cycles per bit. A zero is encoded by leaving the first 2 cycles of the 4 cycle bit period with the transmitter turned on, followed by the last 2 cycles of the 4 cycle bit period with the transmitter turned off. A one is encoded with the opposite sequence: the first two cycles are turned off followed by the last two cycles turned on. In this scheme no more than 4 consecutive cycles would be suspended. The digital circuitry in the Rectifier/Data demodulator ASIC counts the half cycles during with rectifier current is sensed for each of the two halves of the bit period. During the first half, a counter counts down based on the number of half-cycles of conduction. During the second half, the same counter counts up. At the end of the bit period a decision is made about the value of the bit based upon the residual count in the counter.



Figure 47 shows the 5MHz transmitter being modulated with this suspended-carrier data protocol and the output response of the Rectifier/Data demodulator ASIC.

Figure 47 – Oscilloscope waveforms for the Rectifier/Data demodulator ASIC

In Figure 47, two different modulation patterns are shown, representing two different stimulator commands. In interpreting the waveforms of Figure 6 it is important to correlate the value of the Modulation Out signal with the Modulation In signal, at the leading edge of each Data Clock cycle. Note the TAG sequence at the beginning of the commands.

Computer-based Block Chip Controller. During this contract our Block Chips have been used to drive simulated electrode loads consisting of a series access resistance of 20k-ohms, and a simulated double charge layer capacitance of 2nF, as shown in Figure 48, below. These values resulted from testing that we performed at the Laboratory of Neural Control, at NIH. However, we have become concerned that actual electrodes may present load characteristics that are different, and therefore the performance of the Block Chips may not fully meet the target application.



100 usec/div

Figure 48 – Oscilloscope photograph of a Blockchip driving a simulated electrode load.

To study this, we implemented a computer-based controller system that directly communicates with a group of 16 Block Chips. One of the major problems in communicating with the implant, or with a bench-top version, as we are building now, is how to get a precise data stream out of the computer. Although modern PC-based machines are high-speed, they are encumbered by the Windows operating system. We made several attempts to use PC-based software to generate timing signals for use by our transmitter, and for use by individual Block Chips. We have explored several possibilities, including: LabView-based VI's, assembly-level programming, external microcontrollers operated over a USB, and use of a high-speed parallel port with compiled C-programming.

We have identified a digital I/O card that uses a novel buss-mastery technique. This card includes 32 digital I/O lines. Once commanded, the card assumes control of the PC buss, and sets itself at the highest priority level. As description of the hardware follows below:

We are using the High Speed 32-Bit Pattern and Handshake Digital I/O (DIO-32HS) and Timing I/O Counter/Timer Card (NI-6602). The DIO-32HS is a highspeed 32-bit, parallel digital I/O interface for PCI, PXI, PCMCIA and ISA. We are using the one with PCI interface. The 6533 (DIO-32HS card) incorporates the national instruments DAQ-DIO ASIC, a 32bit general-purpose digital I/O interface specifically designed to deliver high performance on plug-in digital I/O boards. The 6533 perform single point I/O, pattern I/O and high-speed data transfer using a wide range of handshaking protocols at speed up to 76Mbps. All 32 lines can be configured in groups or individually.

The 32 digital I/O lines are divided into four 8-bit ports. The ports can be grouped into two 8-bit or 16-bit groups or single 32-bit group. Each I/O line is 5V/TTL compatible. When configured for output, each data line can sink or source 24mA when set logic low or high respectively. When configured as input, the 6533 data lines are diode-terminated to dampen line reflections.

The 6533 can be operated in Pattern I/O, Pattern detect, Handshaking I/O and Burst modes. To serve our purpose we are using Pattern I/O mode. Pattern I/O is reading or writing digital data at predetermined rate without wait states. We control this rate by an internally supplied frequency. (This frequency is generated by the NI 6602 counter/timer card). The 6533 works with start and stop triggering as well as digital pattern detection. Stop trigger is the primary trigger. The 6533 transfers specified amounts of data both before and after a stop trigger. If a stop trigger is not enabled, the 6533 stops automatically after transferring a number of data equal to the size of the buffer. The VI (Lab View program) generates the data stream and fills up the buffer in the memory. Then it asserts a start signal to enable the board. We are able to output the data at 5.2MHz (which is the required rate to test the Block Chip) on a PC (Win 98) with a graphical interface.

Using this card, we have been able to write software in Visual Basic that implants a user friendly Graphical User Interface (GUI). A screen snapshot of the GUI is shown below in Figure 49.

This GUI allows us to set the amplitude, frequency, pulse width, and polarity, for up to 128 electrodes channels, controlled by 16 block chips. This hardware-software combination is extremely versatile, and will permit us to test our Block Chips under actual laboratory conditions, using implanted microelectrodes. We are interested in understanding the performance of the constant-current drivers while driving implanted micro-electrodes. We are also interested in testing the susceptibility of the Block Chips to electrical damage in order to better access the reliability of a complete implantable transcutaneous stimulator.

We plan to complete the implementation of this system in the next quarter. We are also discussing an opportunity to test the 128-channel bench-top stimulator in some animal tests at the University of Chicago.

Presently we have taken measurements of the Block Chip's performance while driving the simulated electrode load of 10k-ohms, and 20 nF. Below, we present an oscilloscope photograph of a computer-controlled Block-Chip driving the simulated load with 40uA/phase and 200usec/phase. Note that the constant current is maintained in spite of the changing electrode voltage.



Figure 49 – Screen snapshot of GUI used to control 128-channel benchtop stimulator

We used this stimulator in series of primate experiments at the University of Chicago. Electrodes implanted in area V1 of a Rhesus monkey were driven by the stimulator, and controlled from the computer. In a series of experiments, voltage waveforms were recorded by a digital PC-based recording system. The electrodes were driven a 1.5mC/cm², constant current. Two typical waveforms are shown in Figures 50, 51, below. Note that the stimulator is able to maintain the stimulus current in spite of the increasing output voltage. This is a direct result of the design of the Blockchip output stage which contains the active-regulated cascode circuitry.

Electrode Voltage



Figure 50 – Typical voltage waveform for 500 sq micron Iridium oxide electrode driven at 1.5mC/cm².



Electrode Voltage

Figure 51 – Typical voltage waveform for 500 sq micron Iridium oxide electrode driven at $1.5 mC/\rm{cm^2}$

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