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A Microelectrode Stimulation System for a Cortical Neuroprosthesis

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***Abstract*—This paper describes an integrated microelectrode stimulator for intracortical neuroprosthesis. The implantable microelectrode stimulator uses flip-chip technology to be fully implantable without wiring, reducing the risk of infection and increasing robustness. It is small enough to be undetectable and has low power consumption which can be obtained directly from the carrier, through an RF low-coupling transformer, discarding the need for batteries.**

The system architecture and circuit techniques which overcome some of the application issues are presented. Simulation results and the layout of a prototype prove its feasibility.

I. INTRODUCTION

Biomedical applications have seen an intense research effort in the last few years. Due to its huge complexity it is a multidisciplinary area where microelectronics plays an important role for the feasibility of most systems. Implantable stimulators for biomedical applications, most commonly applied, are in the area of muscular or nerve stimulation, for heart, limbs or hearing diseases [1-3].

Some of these applications, such as pacemakers, require very low power systems, to avoid the replacement of batteries, but its action requires also almost no signal processing.

Biomedical implementations in the field of visual rehabilitation, is in its early stages. Besides the mechanical and optic mechanisms associated with vision which are already fully understood and can be corrected by surgery or external lenses, other mechanisms like the image processing that takes place from the retina down to the visual cortex is still not well known.

Recently research results on experiments to stimulate the visual cortex to improve the quality of life for blind or partially blind people have been presented [4-7]. In this paper we address an integrated microelectrode stimulator for intracortical neuroprosthesis. The system architecture was presented in [8] where the system is divided in two parts: a primary system placed outside the human body where all the processing takes place, and a secondary system, placed inside the human head, just to activate the electrode array implanted in the visual cortex (Fig. 1).

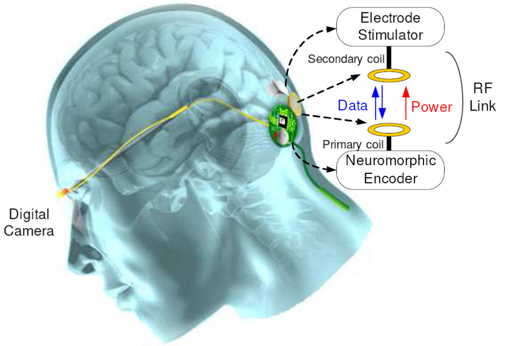

Fig. 1: Cortical Visual Prosthesis.

The first solutions to interface the implant with data and power were by a wired link [4]. However, it requires a large number of wires and, apart from the discomfort, it poses a high risk of infection.

With RF coupling, data and power can be obtained directly from an RF low-coupling transformer discarding the need for batteries or wiring.

Here, we address the implantable microelectrode stimulator which uses flip-chip technology to be fully implantable without wiring, reducing the risk of infection and increasing robustness. It is small enough to be undetectable and requires a power on the order of miliwatts which can be obtained from the low power RF carrier itself.

The system architecture is revised in Section II and the implantable solution is proposed in Section III. The circuit techniques used to overcome some of the application issues are presented in Section IV. Simulation results and the layout of a prototype that prove its feasibility are presented in Section V. Finally, we draw some conclusions in Section VI.

II. SYSTEM ARCHITECTURE

The system architecture represented in Fig. 2 [8] has two parts connected by an RF link: a primary system responsible

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for the processing which is placed outside the human body, and a secondary system, placed inside the human head, which obtains energy from the signal through the RF link and recovers the data and the clock.

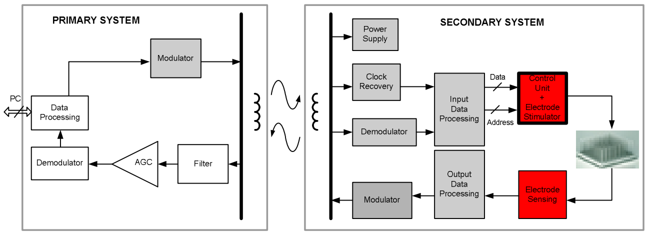

Fig. 2: Architecture of the intracortical prosthesis RF link system.

The system has two RF links in the same transformer: the forward link where a power/data signal is transmitted using Frequency Shift Keying (FSK) modulation with a 10 MHz frequency carrier and up to 1 Mbps data bit rate and a backward link where data is transmitted in the reverse direction using DBPSK modulation with a 1.25 MHz frequency carrier data bit rate is up to 156.25 kbps. The secondary power, data and main system clock are derived from the forward link signal. After demodulation and frame disassembly, useful data is forwarded to the electrode stimulator. This paper addresses the "control unit and electrode stimulator" block, and the "electrode sensing" block (Fig. 2) as these are the most sensitive analog circuits of the system. A prototype with 4 electrode stimulators is being layout in a VLSI CMOS technology (0.35µm).

III. IMPLANTABLE SOLUTION PROPOSED

The array of microelectrodes is a matrix of 10 by 10 and has a total area of 4.2x4.2mm^2. The number of electrodes in a microelectrode array is limited due to technology issues; the size of each electrode is limited by mechanical robustness and the enlargement of the matrix is ineffective because the brainis not plain, and there is an ideal deepness in the visual cortex that should be stimulated. Therefore, with the available technology it is just possible to implant several arrays.

The Electrode Stimulator block is responsible for stimulating the electrodes and is essentially a digital-to-analog converter (DAC). The Control Unit block is a digital controller that provides the Electrode Stimulator with the current amplitude and the duration of stimulation in clock cycles. It also controls the charge/discharge mode of the DAC.

The two most opposite solutions are to have: only one DAC with the output addressed to the chosen electrode, or a DAC for each electrode.

We have favoured the second, because it gives more flexibility, we can address several electrodes at the same time, and if any problem should occur in one electrode, all the other can keep on functioning.

The problem of such solution would appear to be power and area, but we solve the area problem because we decided to do a flip-chip circuit to be placed directly in the microelectrode array (represented in Fig. 3). This, removes the need for wiring, reduces overall size and increases reliability. Therefore, each Control Unit and Electrode Stimulator blocks are located at the base of a microelectrode, the circuit with the DAC and the digital controller can occupy an area equal to a microelectrode, which has 0.42x0.42mm^2, not to waste die area.

Regarding power, although the circuit is to be powered externally, special care has to be taken to reduce the power consumption. The available energy extracted from the input (modulated) signal is low. because the signal is sent through a transformer with a low k factor [8]. The power issue is overcome having each DAC in idle mode and being only activated when the respective electrode is addressed.

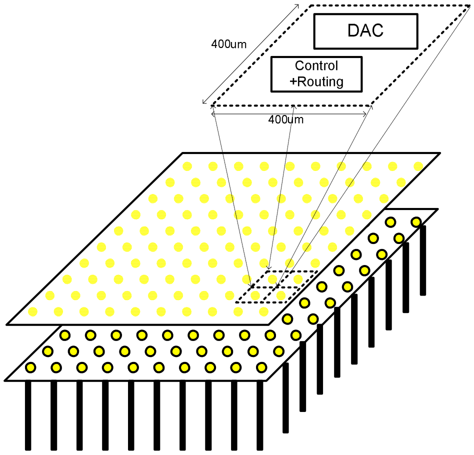

Fig. 3: Flip-chip solution for the electrode matrix and electrode stimulator circuit.

Special care has to be taken not to harm the patient with an accumulation of electric charges in his brain. The microelectrode has to be discharged after being charged and both phases have to have similar behaviour.

The DAC has to stimulate a microelectrode for $2T$ seconds with a maximum current I. Such stimulation consists in charging the load with a pre-determined current amplitude I for T seconds and, after that, discharging the microelectrode with the same current amplitude I for T seconds. It also has to support an output voltage variation of ±1V. The microelectrode is represented by a 10kΩ resistance and a 2pF capacitance and is connected to ground. The stimulation has a maximum of T=100µs and I=100µA. The duration and the amplitude of the stimulation are controlled by two five bits signals. The expected output of the Electrode Stimulator is represented in Fig. 4.

One main issue considering this application is that the impedance of the electrode changes for each patient and even for each electrode. It is therefore, necessary to monitor what is happening in each electrode when addressed in a system calibration mode after the system is implanted. This makes necessary a backward link where an ADC is used to sense the voltage at the electrode. This ADC is shared by all the electrodes and in test mode only one electrode should be addressed at a time.

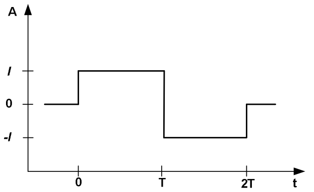

Fig. 4: Charge/discharge cycle of a stimulated electrode.

IV. CIRCUITS DESIGN

All the circuits presented here are designed and simulated for process and mismatch variations. Power supply voltage variations are compensated by a self compensated bias circuit with a start-up circuitry, tolerant for such variations. The temperature was set to 37º Celsius as this is the human body temperature. The power supply voltage is 3.3 V, with V_{DD}=+1.65V and V_{SS}=-1.65V. The technology is a 0.35µm CMOS technology.

Electrode Stimulator (DAC)

The most important block to be designed is the DAC circuit. Although, the specifications in terms of frequency and resolution are not difficult to meet, other issues like ensuring equal charge and discharge of the brain for each electrode activity, settling time of the DAC when addressed and reduction of spikes in the transitions made the design more challenging.

Two approaches were considered to buffer the DAC output current to the electrode which are compared here.

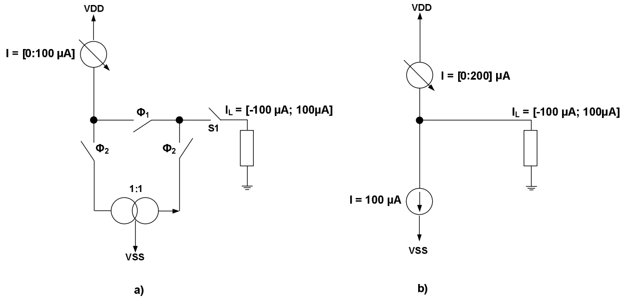

Fig. 5: Electrode stimulator output stage (electrode buffer).

The electrode buffer topologies are represented in Fig. 5. The topology in Fig. 5 a) has a current source connected to V_{DD} which represents the five bit converter's output current. In phase ϕ_1 and with switch S_1 on, the current from the converter is mirrored and is fed into the microelectrode. This is the charge phase. In phase ϕ_2, with switch S_1 on, the current flows from the load through the converter. This is the discharge phase. This architecture does not ensure a similar behaviour between charging and discharging operations due to the use of a current mirror. Hence, mismatches between charge and discharge current should be prevented.

The topology in Fig 5 b) has a current source connected to V_{DD} which can set a current from zero to 200µA, and represents the converter's output current. A current source connected to V_{SS} has a fixed current of 100µA. Depending on the 5-bit DAC the load is charged/discharged with a maximum current of 100µA.

Notice that the operation of charging the load is no different from discharging it, which ensures a good circuit performance, since the load seen by the converter is always the same.

Although this, more complex, architecture has a better performance, providing a better compliance between the charge and discharge current than the simple architecture that uses current mirrors, it uses much more power (depending on the amplitude from two to 30 times). We have decided to use the first topology, and its implementation using a wide swing cascode is represented in Fig. 6.

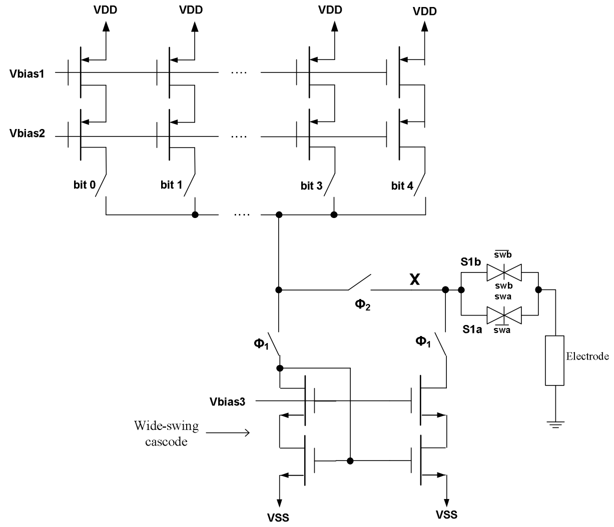

Fig. 6: Electrode Stimulator (DAC) schematic.

The glitch in the microelectrode occurs when switch S_1 commutes. When the Electrode Stimulator block is enabled, in the transition from phase ϕ_2 to phase ϕ_1, while switch S_1 is off, the voltage at node X (Fig. 6) is almost 1.5V, and all switches have low resistance, working on the triode region because of the headroom available. When switch S_1 turns on, there will be a small resistance connecting two nodes with different voltages. Since node **X** has a voltage of almost 1.5V and the output is grounded, the current spike can be significant. To prevent this glitch to occur, an extra switch (with a higher resistance) is placed in parallel (S_{1a} and S_{1b}) lowering effectively the current spike.

Control Unit

The Control Unit block activates or configures the Electrode Stimulator block. The digital controller must allow the configuration of both the amplitude of the Electrode Stimulator's output current and the duration of the stimulations that will be applied to the microelectrode, which is done by means of a counter respective to the clock master. It must also allow the Output Data Processing block to read such configurations. Hence, the digital controller has activate, read and write operations. The digital blocks are written in synthesizable Verilog to be incorporated with the DAC in each electrode slot. The digital block high level fluxogram is represented in Fig. 7.

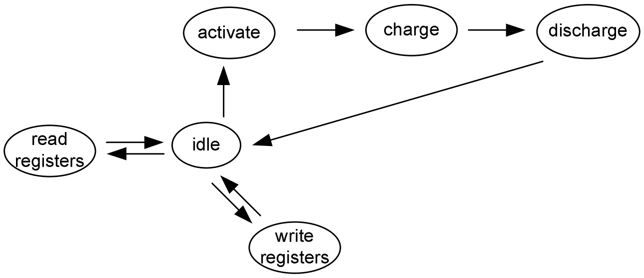

Fig. 7: Control unit digital fluxogram for each electrode stimulator.

Analog-to-Digital Converter

The ADC to be used in the backward link should have high impedance, low capacitance input in order not to disturb the electrode being measured. We have used a successive approximation converter, with a dynamic comparator at the input.

V. SIMULATION RESULTS AND LAYOUT

To be compared with that of Fig. 4, in Fig. 8 it is represented the simulation result of the charge/discharge cycle of a stimulated electrode, where it can be observed that the spike is indeed negligible.

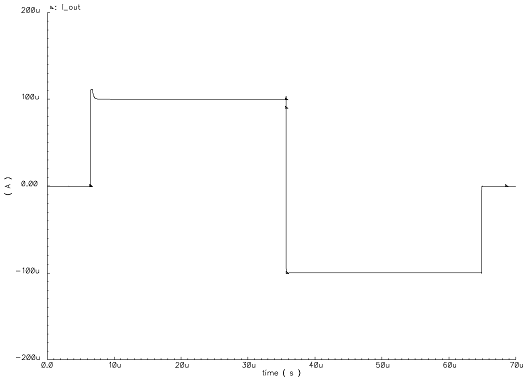

Fig. 8: Simulation of a charge/discharge cycle of a stimulated electrode.

A prototype with 4 electrode stimulators is being layout in a VLSI CMOS technology (0.35µm) sharing a bias block, with the diagram represented in Fig. 9 (in the final circuit a bias circuit will be shared among each 25 electrodes). The digital part is compliant with the 10 by 10 electrode array and the layout is fully scalable. For the final version of this paper a layout will be presented. A first version of the circuit in a 0.8um technology was designed and fitted the target area, with more and larger transistors, thus we expect no difficulties.

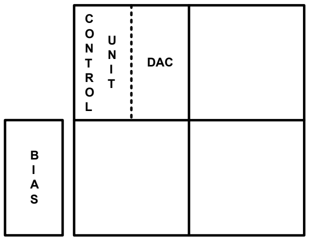

Fig. 9: Prototype circuit distribution.

VI. CONCLUSIONS

This paper describes an integrated microelectrode stimulator system for an intracortical neuroprosthesis. The implantable microelectrode stimulator uses flip-chip technology between the circuit and the microelectrode array. The system architecture and application issues are discussed. It has a DAC for each electrode stimulator, which is the best solution once the area is limited by the electrode array. The designed DAC has low power consumption and small area and special care was taken to reduce glitches and ensure that the charge and discharge cycles are equal.

Simulation results are presented and a 2x2 electrodes prototype IC is being layout.

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