Florida Wireless Implantable Recording Electrodes (FWIRE) for Brain Machine Interfaces

Rizwan Bashirullah, John G. Harris, Justin C. Sanchez†, Toshikazu Nishida and Jose C. Principe

Department of Electrical and Computer Engineering,
†Department of Pediatrics Division of Neurology
University of Florida, Gainesville, FL 32611
{rizwan, nishida}@ufl.edu, {harris, justin, principe}@cnel.ufl.edu

***Abstract*— This paper reviews on-going efforts towards the development of the Florida Wireless Implantable Recording Electrodes (FWIRE). The FWIRE microsystem platform is a fully implantable flexible substrate microelectrode array that employs state-of-the-art integrate-and-fire (IF) signal representation and wireless interface circuitry for recording neural activity from behaving rodents. The modular nature of the implantable neural recording electrode allows future enhancements to be seamlessly added to improve functionality including but not limited to rechargeability through inductive coupling, custom microelectrode arrays, higher capacity batteries, and more advanced integrated circuit technologies. This paper concentrates on custom integrated circuits such as neural interfacing amplifiers, baseband signal processing, wireless data and power interfaces, and battery management system.**

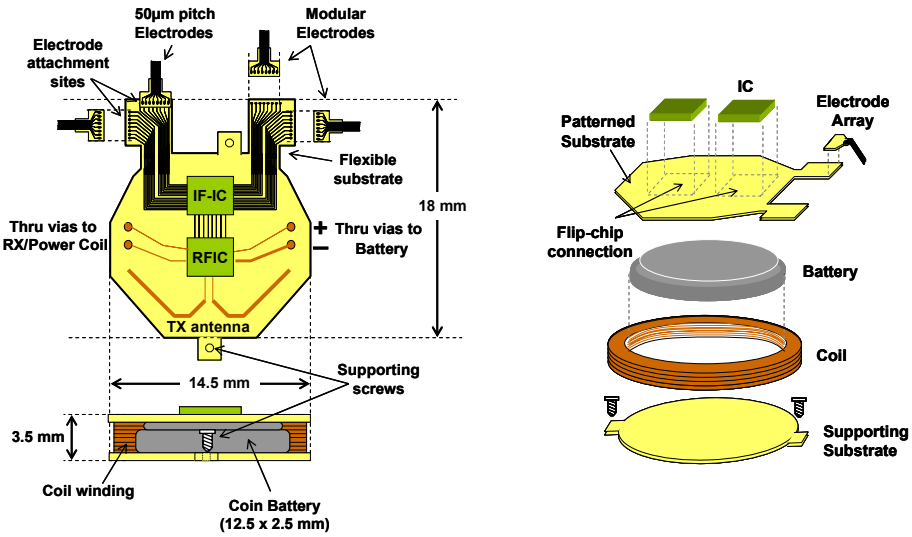
I. INTRODUCTION

Neuroscientists have long recognized the importance of distributed representations to understand brain function [1]. The wish list of the neuroscientist for microelectrode array systems includes (but it is not limited to): minimal injury to brain tissue, biocompatibility, longevity, subcutaneous implantation, long operation, high channel count, high and stable cell yields, and access to the spike data and/or field potentials with high signal-to-noise ratio. From an engineering perspective, the functional building blocks of a probe are the electrodes, the amplification stages, and the transmission of information to a base station if the animal is not tethered. The design constraints are easy to state but much harder to comply with: basically one wishes to minimize the power consumption per transmitted bandwidth with a given signal-to-noise ratio from the electrode to the external receiver. The degrees of freedom (materials, electrode geometries, amplification, A/D, wireless) to accommodate the experimentalist and engineering are enormous, and are visible on the very different engineering solutions proposed and implemented by several research groups [2].

To date, the most commonly used neural recording electrodes are still the insulated microwire arrays (tungsten or platinum) because they have been the most successful for chronic implantation [3], and they can be handcrafted and shaped at the time of the implant in the researcher's lab, allowing for many different possibilities of insulation and tip coating. Other approaches employ microfabrication and micromachining techniques to overcome the one-at-time manufacturing of mechanically assembled electrode arrays and enable integration of electronic circuits into a low profile microsystem platform. Using photolithography to transfer electrode patterns, precise control of electrode geometry to less than 1μm tolerance has been demonstrated [4]. Moreover the RS/NTD (recording sites per volume of neural tissue displaced) is much higher because the electrode form factor is smaller and multiple pads can be placed in the same tip. The great appeal of this solution is that inter-component electrode and electronic assembly is virtually eliminated, although independent optimization of the arrays is not possible after fabrication because electrodes and electronics share the same substrate. An intermediate electrode design known as the Utah Microelectrode Array (EUA) [5] uses micromachined arrays of single contact electrodes, electroplated to a connector with local amplification. This approach allows for flip-chip attachment of electronic circuits for neural signal amplification, processing and wireless transmission over an RF link. The manufacturing repeatability of this electrode system is much higher than the microwires, but the RS/NTD is virtually the same and the electrode array dimensions (i.e. length) are essentially fixed at the time of implantation.

Numerous wireless platforms with varying degrees of functionality and complexity (channel count, data rates, signal processing, etc) have been proposed to amplify, process and transfer signals to an external base station [6]. These microsystems are often powered from relatively large primary batteries, or are operated using an extracorporeal and close-proximity backpack to continuously power the implanted unit via wireless inductive links, which in the case of small animals such as rodents, creates many inconveniences to the researchers during electrophysiology experimentation. Other implementations employ microwire arrays with local amplification and head-mounted connectors with bulky backpacks [7].

This brief review provides the context to outline the proposed platform investigated in this paper. The proposed Florida Wireless Implantable Recording Electrodes (FWIRE) is a low-profile neural recording platform with bidirectional communication capability that achieves (1) miniaturization via CMOS integration of electronic components (2) power reduction via alternate signal representation of neural signals (3) extended operation using miniaturized wirelessly rechargeable (secondary) battery and (4) modular electrode implementations for greater flexibility during experimentation. This paper presents a brief overview of the FWIRE platform but concentrates on the custom integrated circuit development including neural interfacing amplifiers, baseband signal processing, wireless data and power interfaces, and battery management system.



(a) (b)

Fig. 1. Florida Wireless Implantable Recording Electrode (FWIRE) (a) microsystem platform (b) assembly.

II. SYSTEM OVERVIEW

As illustrated in Fig. 1, the FWIRE microsystem consists of a flexible substrate that serves as the platform for the signal processing (IF-IC) and wireless telemetry (RFIC) chips, transmit antenna, receive and power coil, and microwire electrode array. A low profile rechargeable battery is located below the flexible substrate and is used to power the implant electronics during recording sessions. The external coil wraps around the battery for a very compact package assembly and enables wireless battery recharging. The CMOS ICs are flip-chip bonded onto the flexible substrate, which is encased in medical grade silicone for isolation from fluids. Mechanical stability of the patterned flexible substrate is provided by the underlying battery/coil, supporting substrate and screws, which attaches the platform to the skull of the behaving animal and provides the required ground reference for the on-chip electronics. Multiple electrode attachment sites onto the flexible substrate using micromachined flexible polyimede ribbon cable provide additional flexibility for experimentation. The metal traces and corresponding bond sites can be made to any size specification and spacing distance via photolithography. The initial prototypes of the electrode array consists of a row of eight (30 µm diameter with 50 µm pitch) gold-plated nickel electrodes with parylene-C insulated shanks that extend 4 mm from the edge of the flexible polyimide cable [8]. *In vivo* studies produced a high neuronal yield with SNR ranging from 10 to 27 dB. The resulting FWIRE platform is a highly modular architecture that takes into consideration the mechanical and physical constraints of the implant site, and facilitates independent development and testing of its individual components.

III. NEURAL SIGNAL PROCESSING AND REPRESENTATION

At the core of the engineering difficulty are the data rates required, which are related to the representation of information from analog to digital domains embodied in the Nyquist theorem. The core innovation is an alternate signal representation to translate analog waveforms to samples which we call integrate-and-fire (IF) that uses asynchronous sampling: the integral of the analog voltage is transformed into a pulse when it reaches a threshold. Hence the information about amplitude is contained in the timing of the pulse. There are three main advantages of the IF representation: (1) the implementation of the IF in analog VLSI is trivial compared with the A/D converter resulting in substantial power savings; (2) the data rates decrease drastically because the information is in the timing of pulses, so transmitting a continuous sequence of for example 12 bits per sample is not necessary; (3) wireless asynchronous communications are possible, which also simplifies the RF circuits.

A. Neural Amplifier

The analog hardware design for the amplification of extracellular neural signals is quite challenging. These neural signals have amplitudes ranging from 50 to 500µV, but large DC offsets also arise across different recording electrodes due to electrochemical effects at the electrode-tissue interface. The magnitude of these DC offsets is about 1-2 *V*, much larger than the neural signals to be measured. The relevant frequencies of the brain waves range from 100 *Hz* to 7 *kHz*, while the Local Field Potentials (LFP) extend to below 1 *Hz*. Thus, the ideal band-pass filter for neural recording must reject the DC offset while passing the LFP signal. The first stage of our circuitry is a pre-amplifier providing about 40 *dB* gain at the passband and an AC coupling technique is used to reject the inherent DC offset [9]. The structure of the preamplifier was originally proposed by [10].

B. Integrate and Fire Representation

The voltage output of the amplifier is first converted into current and, by integrating this current, the amplitude information is encoded into an asynchronous digital pulse train. This integrate-and-fire (IF) module efficiently encodes the

analog information as an asynchronous train of pulses [9]. The principle is to encode amplitude in the time difference between events. The advantage is that a single event represents a high resolution amplitude measurement, with great bandwidth and power savings. These pulses have better noise immunity than conventional analog signals in transmission and also eliminates the need for a traditional ADC. The latest version using a delta-sigma modulation style to produce timing events resulted in 52μW of power dissipation with 8-*bit* resolution [11]. Given a bandlimited continuous signal $y(t)$, we create an alternate representation

$$\hat{y}(t) = h(t) * \sum_k w_k \delta(t - t_k) = \sum_k w_k h(t - t_k) \quad (1)$$

where $|y(t)-\hat{y}(t)|<\varepsilon$ for all time, w_k are appropriate weights and $h(t)$ is the sinc function. Sampling times t_i are given by: $f(t_k)=k\theta$ where

$$\int_{t_k}^{t_{k+1}} y(t)dt = \theta \text{ and } f(t) = \int_{t_0}^{t} y(\tau)d\tau \quad (2)$$

Previously, simple linear low-pass filters were used as crude reconstruction filters from integrate-and-fire outputs, computing something similar to rate coding from the spike train, and the performance was poor. Pulse times are determined by the local area under the signal input $x(t)$, and they can be used for perfect reconstruction. Let us assume that $x(t)$ is bandlimited to Ω_s and the maximum interspike interval $\boldsymbol{T_{max}}$ satisfies $T_{max}<\pi/\Omega_s$. From mathematical frame theory, it is known that any bandlimited signal can be expressed as a low-pass filtered version of an appropriately weighted sum of delayed impulse functions which is expressed in Eq. 1. So the signal recovery problem is how to calculate the appropriate weights. We can define the timing of pulses: $\boldsymbol{T}=[t_1, t_2 \ldots t_k, t_{k+1} \ldots]$. Let $y(t)=v_{in}A_{in}-V_{ref\text{-}supply}+V_{mid}$. Substituting Eq. 2 into Eq. 1, we obtain

$$\theta = \int_{t_i}^{t_{i+1}} y(t)dt = \int_{t_i}^{t_{i+1}} \sum_j w_j h(t - t_j)dt = \sum_j w_j \int_{t_i}^{t_{i+1}} h(t - t_j)dt \quad (3a)$$

and

$$c_{ij} = \int_{t_i}^{t_{i+1}} h(t - t_j)dt \quad (3b)$$

which can be rewritten in matrix notation as $\boldsymbol{CW} = \theta$. Unfortunately, $\boldsymbol{C}$ is usually ill-conditioned necessitating the use of a SVD-based pseudo-inverse to calculate the weight vector $\boldsymbol{W}$. We have extended the reconstruction algorithm to work for a biphasic pulse train with positive and negative pulse indicating when a positive or negative threshold is surpassed [12].

C. Measured Results

We have fabricated a biphasic integrate and fire chip and successfully quantified its performance. We used an Agilent 1693 digital analyzer to record the timing information of the pulse output with a sample rate of 5ns. When the bias current of the comparator was 0.3μA, the average pulse width was 108.24 *ns* with a standard deviation of 2.39 *ns*. As IEEE-STD-1241 requires, a curve fitting method (sine wave fitting) was used to evaluate the reconstruction performance with the algorithm described below. There are 4 basic steps to characterize an ADC: 1) set up the device; 2) apply a single tone sine wave as an input; 3) collect sampled and quantized data; and 4) calculate standardized parameters using off-line algorithms. The input is a 2 *mV* 1 *kHz* sine wave. An off-line al ADC test evaluation program determines that the reconstructed sine wave has 8 effective bits. Fig. 2 shows the recorded pulse train from a fabricated chip and the reconstructed sine wave.

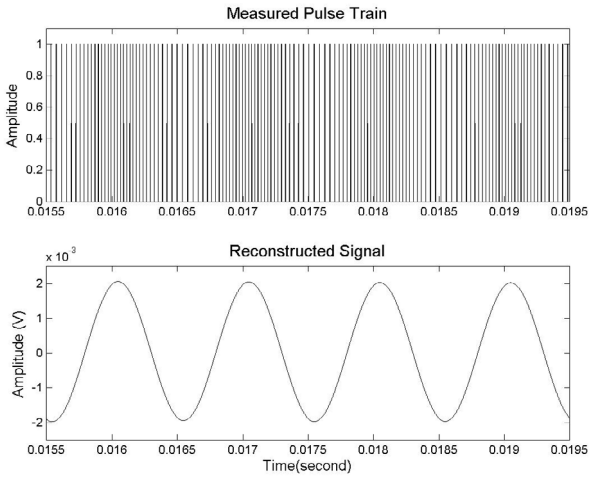


Fig. 2. Top shows measured pulse train. Bottom show reconstructed sine wave input.

IV. WIRELESS

A. System Architecture

A wireless interface for the FWIRE microsystem is currently being developed to facilitate in-vivo neural recording in behaving animals. As shown in Fig. 3, the system includes a power recovery, regulation and battery management module; an ASK clock and data recovery circuit to download external system commands; a transmitter and signal processing circuits to upload neural data from the various recording channels; and a small controller with register bank to oversee system functionality, decode/encode data packets and store on-chip settings. All components are fully integrated with the exception of the power/downlink coil, the uplink antenna and the battery.

B. Wireless Power and Data Interface

A 4MHz LC tank with on-chip resonant capacitor, full-wave rectifier, storage capacitor, low drop-out voltage regulator and RF limiting circuit provide a stable supply and over-voltage protection to the implant electronics. Schottky contact barrier diodes are used in the bridge rectifier circuit to improve the frequency response and lower the turn-on voltage. As shown in Fig 4a, Ti-Si_2 schottky barrier diodes are fabricated in standard 0.6μm CMOS process by selectively blocking the n+/p+ implants in desired diffusion areas [13]. The measured I-J characteristic of the schottky barrier devices is shown in Fig. 4b. The devices have an ideality factor of ~1.16 and barrier height of ~0.5eV, which was computed using the Richardson-Dushman equation for the thermionic current [14]. The measured turn on voltage is ~300mV,

which is lower than standard pn junction based implementations [15]. The diodes are fabricated with small schottky contact area as this yields a higher cutoff frequency [16], and multiple cells are placed in parallel to improve the current handling capability.

Fig. 4c shows the transient regulator response when an externally generated 0 to 2mA load step is applied as the link is powered by the primary coil voltage. The measured response is within 15% (or 600mV/4.1V) of the target 4.1V supply. The regulator exhibits a load regulation of 2mV/mA (or 240ppm/1mA), a line regulation 2mV/V and a low dropout voltage of 50mV. At 4MHz, the worst-case measured peak-to-peak ripple voltage at the output is within 100mV. A battery management circuit has been implemented to charge and monitor the external Li-ion cell battery [13]. Charging profile experiments for the battery control loop (Fig. 4d) shows that during the constant-current phase, the circuit delivers 1.5mA resulting in a linear increase in battery voltage (V_{BAT}). The end-of-charge (EOC) during the constant-voltage phase is detected once the battery current reaches 5% of the nominal constant charging current of 1.5mA, triggering the EOC signal.

An on-chip clock and data recovery (CDR) circuit is used to download external system commands. Synchronization of clock and data is achieved via a modulation scheme based on amplitude shift keying and pulse position modulation (ASK-PPM) that facilitates clock and data recovery using an ASK demodulator and a charge-pump with latched comparator [17]. The CDR is operational for an input data range of 4kb/s to 18kb/s and exhibits a sensitivity of 3.2mVp-p at 1MHz (Fig. 4e and 4f).

V. CONCLUSIONS

This paper provides a brief overview of current developments towards the Florida Wireless Implantable Recording Electrode (FWIRE) microsystem. Our preliminary modular testing of electrodes, amplifiers and RF subsystem indicates feasibility of a new generation of fully implantable flexible substrate microelectrode array probes for neural recording.

REFERENCES

[1] Hebb 1949; Lilly 1958; Adrian 1965; Fetz and Finocchio 1975; Mountcastle, Lynch et al. 1975; Georgopoulos, Kalaska et al. 1982; Kruger 1983; Georgopoulos, Schwartz et al. 1986; Abeles 1991; Rieke 1996; Nicolelis, Ghazanfar et al. 1997; Freeman 2000.

[2] Salcman 1976; Kruger 1982; Buzsaki 1989; Kennedy 1989; Palmer 1990; Blum, Carkhuff et al. 1991; Campbell, Jones et al. 1991; Jones and Normann 1997; Akin, Ziaie et al. 1999; Bai and Wise 2001; Berger, Baudry et al. 2001; Chang, Brewer et al. 2001; Tsai and Yen 2003; Moxon, Leiser et al. 2004; Obeid, Nicolelis et al. 2004; Wise, Anderson et al. 2004]

[3] Schmidt 1980; Kaltenkack and Gerstein 1986; Fee, Mitra et al. 1996; Westby and Wang 1997; Nicolelis 1999; Porada, Bondar et al. 1999; Williams, Rennaker et al. 1999.

[4] Wise, Anderson et al. 2004; Wise and Angell 1971; Najafi and Wise 1986; Ji and Wise 1992]

[5] Nordhausen, Rousche et al. 1994; Nordhausen, Maynard et al. 1996; Maynard, Nordhausen et al. 1997; Rousche and Normann 1998; Harrison, 2006.

[6] Strumwasser 1958; Warner, Robinson et al. 1968; Beechey and Lincoln 1969; Edge, Horn et al. 1969; Eichenbaum, Pettijohn et al. 1977; Grohrock, Hausler et al. 1997; Xu, Talwar et al. 2004

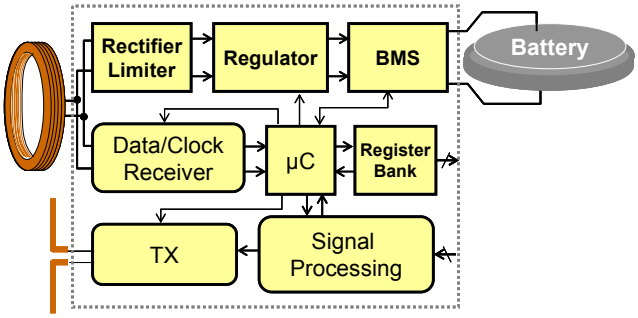


Fig. 3. Wireless interface system block diagram

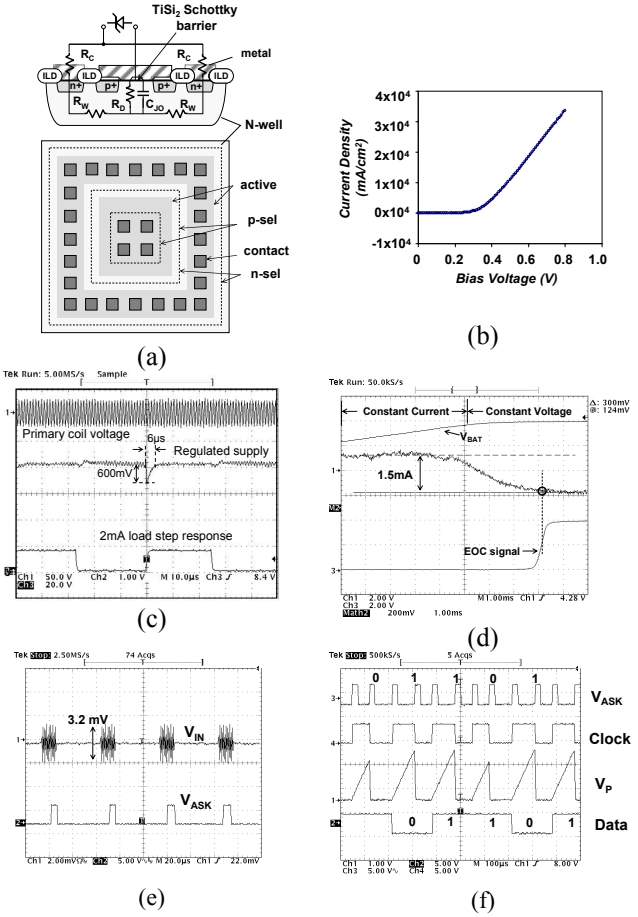


Fig. 4. (a) Schottky contact barrier diode in standard CMOS; measured (b) diode current density vs. bias voltage (c) regulator transient response (d) battery control loop charging profiles (e) ASK detector (e) CDR waveforms.

[7] Obeid et al, 2004; Mohseni et al., 2001; Takeuchi & Shimoyama, 2004; Hoogerwerf & Wise, 1994; Johannessen et al., 2004; Ghovanloo, Najafi, 2004; Irazoqui, et. al 2005; Akin, Najafi 1998, Ziaie, Najafi 1997.

[8] E. Patrick, M. Ordonez, N. Alba, J. Sanchez, T. Nishida, EMBS 2006

[9] D. Chen, J. G. Harris, J. Principe. IEEE EMBS, Sept 2004.

[10] Harrison, R.R. and Guerreri, R. IEEE JSSC, V.38, June 2003

[11] D. Wei, V. Garg, and J.G. Harris. ISCAS, p. 4903-4906, May 2006.

[12] D. Chen, Y. Li, D. Xu, J.G. Harris, J.C. Principe. ISCAS, May 2006.

[13] P. Li, R. Bashirullah, EMBS, 2006

[14] M. Shur, Physics of Semiconductor Devices. Prentice-Hall, 1990.

[15] M. Ghovanloo, K. Najafi, IEEE JSSC, V.39, N.11, Nov. 2004

[16] S. Sankaran, K.K. O, IEEE Elec. Dev. Lett., V.26, N.7, July 2005

[17] H. Yu, R Bashirullah, CICC 2006.