A Neural Recording System for Monitoring Shark Behavior

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Abstract— A neural recording system for monitoring the behavior of sharks is presented. The system consists of an electrode array made of silicon neuroprobes that interface with a flexible parylene cable that connects the electrode array to the electronics to process the neural signals, and a wireless transmission system that transmit the processed signals to the external world. The electronics include amplifiers, multiplexers, analog-to-digital converters, a FPGA, a telemetry chip. The results of the chip designs of amplifier are reported. The challenges in realizing a miniaturized, low power and high density (more than 100 recording sites) recording system are outlined. The choice of architecture and the tradeoffs involved are described.

I. Introduction

Simultaneous recording of a large number of neurons is of great interest to neuroscientists and clinicians to study the behavior of neurons. The knowledge gained by these studies would enable applications such as neural prosthetics and brain-machine interfaces. A multi-channel, low power and low noise neural recording system through microelectrode array (MEA) is necessary for those applications.

The system is designed for the spike signal and local field potential (LFP) sensing in sharks. The signal frequency range is 1 Hz to 10k Hz. LFP recordings can be maintained for longer periods and it is easier to record compared to single cell recordings [1]. LFP in 25-90 Hz is useful for neuroscientists [1]. So 60Hz interference has to be considered if the system is not shielded. Three-electrode technique needs to be employed to reduce the 60Hz interference [2].

Our project goal is first to demonstrate the prototype system, so an off-chip ADC is used. The final goal is to design the entire system in a single chip. Based on the analysis, we propose the one ADC per channel architecture, which improves the performance of the system and consumes less power compare to one ADC multiple channel.

This paper is organized as follows: Section II presents the system architecture for off-chip ADC and circuit block design; Section III presents the proposed system for system on chip based on the comparison between one ADC for multiple channels and one ADC per channel architecture.

II. Architecture with Off-Chip ADC

Figure 1 shows the multiplexed system architecture with off-chip ADC. The goal is to demonstrate a 16-channel 12-bit prototype system. For the multiplexed system, an anti-aliasing filter has to be employed before the multiplexer (MUX). Due to the settling time and crosstalk [3] considerations, a buffer has to be placed before the ADC. For each channel, a low noise amplifier has to be employed since the neural signal is weak.

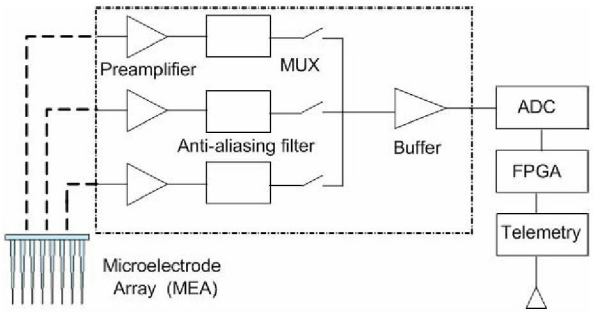

Figure 1. System architecture with off-chip ADC

A. Off-chip ADC

We considered several architectures of ADC for multiplexed system. Successive approximation register (SAR) ADC and sigma-delta ADC are the most poplar architectures for low data rate applications. Since sigma-delta ADC oversamples the time-multiplexed data, the ADC actually correlates the data from multiple channels. Because of this, the sigma-delta ADC actually is not good for multiplexed system. SAR ADC is widely used in multiplexed data acquisition systems.

A 12-bit ADC is required in this prototype system. Considering the matching issue, the capacitive DAC (CDAC) charge re-distribution SAR ADC is chosen. For a standard CDAC SAR ADC, the total capacitance is $2^N C$ if the unit capacitor size is C [4]. Suppose matching dictates C=10fF, a 12-bit ADC needs around 40pF for CDAC capacitor array. There are some ways to reduce the size of the capacitance, but it always comes along with trimming or calibration [5]. CDAC capacitor array inherently has S/H function, so 40pF sampling capacitor is assumed in this paper for 12-bit SAR ADC for calculating the requirement for the previous stages.

B. Anti-aliasing Filter

The cut-off frequency of the low-pass filter (LPF) should be higher than the bandwidth of the measured neural signal. To determine the cut-off frequency, we model the action potential as a simple Gaussian pulse,

$$v_N(t) = k_0 e^{-\pi(t/T_0)^2} \tag{B.1}$$

The Fourier transform of the Gaussian pulse is also the Gaussian pulse, leading

$$V_N(f) = F[v_n(t)] = k_0 T_0 e^{-\pi(T_0 f)^2} \tag{B.2}$$

What is measured at the end of the electrode by extracellular recording is the time derivative of the intracellular signal. If the seal resistance is big enough, we can assume that the signal by extracellular recording is the first derivative of the action potential [6].

$$V_{N,eltd} = j2\pi f \cdot V_N(f) = j(2\pi k_0 T_0) f \cdot e^{-\pi(T_0 f)^2} \tag{B.3}$$

From the fact that the peak amplitude appears at 1 kHz, we can calculate T_0.

$$\therefore T_0 = \frac{1}{\sqrt{\pi} f_1} = 4.0 \times 10^{-4} (\text{sec}) \tag{B.4}$$

Suppose the cut-off frequency of the LPF is f_0, calculating the total energy above the cut-off frequency,

$$E_{N,alias} = 2\int_{f_0}^{\infty} |j2\pi f \cdot V_N(f)|^2 df \tag{B.5}$$

$$\le 8\pi^2 k_0^2 T_0^2 \cdot \frac{1}{4\pi f_0^2} \left(f_0 \cdot e^{-f_0^2 / \left(\frac{1}{2\sqrt{\pi}T_0}\right)^2} + \frac{1}{T_0} erfc\left(\frac{-f_0^2}{\frac{1}{2\sqrt{\pi}T_0}}\right) \right)$$

If we make f_0 such that,

$$f_0 \ge 10\sigma_x \ge 10 \frac{1}{2\sqrt{\pi}T_0} \ge 7(kHz), \tag{B.6}$$

the energy above cut-off frequency eventually approaches 0. Considering a margin, we choose 10 kHz as the cut-off frequency. The result of this analysis is in accordance with the signal frequency range for neural spikes signal in the literatures [7] [8]. This implies that the folding effect for the neural signal due to the MUX and ADC is negligible if 20 kilosamples/s for each channel based on the Gaussian pulse model for action potential.

The order of the LPF also has a direct impact on the total noise at the ADC. The low noise amplifier has the low-pass characteristic resulting that the overall system acts like the LPF of (N+1)th order, and this noise is shaped by the sampling process of the ADC. The flicker noise of the amplifier is much greater than that of the thermal noise, so we can approximate the noise power as the pure 1/f noise in the frequency band of interest. Then we can calculate the added noise power by the sampling process.

$$P_{n,added} = 2\int_{f_0}^{\infty} \frac{N_0 \cdot f_0^{2N+2}}{f^{3+2N}} df = -\frac{N_0 f_0^{2N+2}}{N+1} \cdot f^{-2N-2} \Big|_{f_0}^{\infty} = \frac{N_0}{(N+1)} \tag{B.7}$$

We can also calculate the total noise power before the sampling process, where we assumed that the noise power below low frequency cut-off (1Hz) of the low noise amplifier is negligible.

$$P_{n,original} \cong 2\int_{f_L}^{f_0} \frac{N_0}{f} df + 2\int_{f_0}^{\infty} \frac{N_0 \cdot f_0^2}{f^3} df = 2N_0 \ln\frac{f_0}{f_L} + N_0 \tag{B.8}$$

From the above two equations, the noise is increased by 2.6% and 1.7% if the order of LPF is 1st and 2nd respectively.

So the 2nd order filter is appropriate in terms of noise filtering, area, power and feasibility if 20 kilosamples/s for each channel.

C. Amplifier

Based on session II.B, we could see 10 kHz cutoff frequency for amplifier is reasonable. Considering the LPF and DC open circuit potential at the electrode-electrolyte interface [8], the amplifier should have a high pass pole at low frequency (around 1 Hz). The amplifier is designed for 1Hz-10kHz signal range. Our amplifier architecture is based on [7], as shown in Figure 2. Due to the 60Hz interference appearing at positive and negative inputs, it is common mode noise for the amplifier. So, a high common mode rejection ratio (CMRR) amplifier is required. A high CMRR amplifier also requires a high CMRR OTA. This neural amplifier has been designed and fabricated in 1.8 V, CMOS 0.18 μm process. As shown in figure 2, C1 and C2 are feedback capacitors and C1 is 30pF, C2 is 500fF.

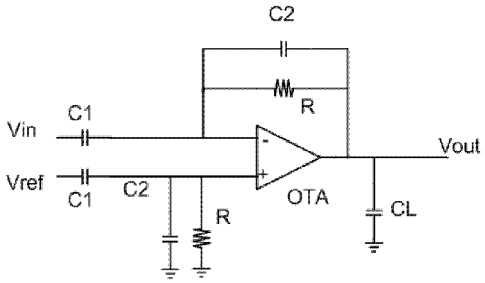

Figure 2. Schematic of Amplifier

Low noise, high CMRR, low power OTA is the core of the amplifier. Figure 3 shows the architecture of the OTA.

In order to achieve high CMRR of OTA, the PMOS is chosen for input differential pair due to the body effect consideration. Using the wide-swing cascode current mirror to generate the high impedance tail current, the CMRR can be improved. To reduce the systematic mismatch, wide-swing cascade current mirror is used in OTA [4].

Small offset voltage of the OTA means high CMRR of the OTA based on (C.1) [12]. The CMRR is improved normally when the offset is reduced.

$$CMRR = \frac{\Delta V_{CM,in}}{\Delta V_{OS,in}} \tag{C.1}$$

Considering the random mismatch, the input differential pair is designed to operate in weak inversion. Due to the large g_m/I_d in weak inversion, the offset voltage due to the input differential pair (M_{DP} in Figure 3) is reduced compared to the input pair in strong inversion as proved by Vittoz [11]. Now let's consider the load transistor M_L in Figure 3. The ratio of transconductance between the load transistor and differential pair g_L/g_{DP} is small since the differential pair is in weak inversion and load transistor is in strong inversion. From the third part in the right side of the equation (C.2), the offset due to the load transistor is also reduced compared to the input pair in strong inversion. So the overall offset is minimized and the CMRR of the OTA is improved when the input differential pair is in weak inversion.

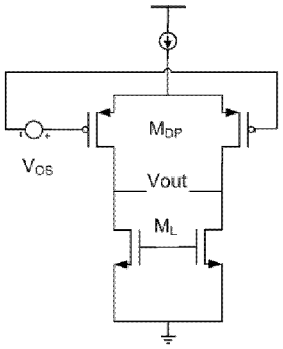

Figure 3. PMOS input pair, NMOS load transistor circuit

$$V_{OS} = \Delta V_{TH,DP} + \frac{I_D}{g_{DP}}\left[\frac{\Delta(W/L)}{W/L}\right]_{DP} + \left\{\Delta V_{TH,L} + \frac{V_{GS}-V_{TH,L}}{2}\left[\frac{\Delta(W/L)}{W/L}\right]_L\right\}\frac{g_L}{g_{DP}} \quad \text{(C.2)}$$

Input differential pair in weak inversion is also good for noise performance [7].

In Figure 4, there are two NMOS shunt current transistors (M_{17}, M_{18}). This technique improves the noise performance [9] and increases open-loop gain [10]. Also, these techniques reduce the power consumption to achieve the performance as listed in Table I.

Input referred RMS noise of the neural amplifier is 12.4 μV, the CMRR of the amplifier is 75 dB and the power consumption of the amplifier is 20.7 μW without biasing circuit based on the measurement of the test chip. Figure 5 shows the die of the chip.

D. 16-channel analog multiplexer design

If the sampling rate for one channel is f and the number of channels is N, the ADC's sampling rate should be N x f. The clock jitter and skew between analog multiplexer and ADC is negligible and therefore the only uncertainty source that affects the sampling window is transition time. So transition time should satisfy (D.1).

$$t_{tran} \le \frac{1}{N \times f} \quad \text{(D.1)}$$

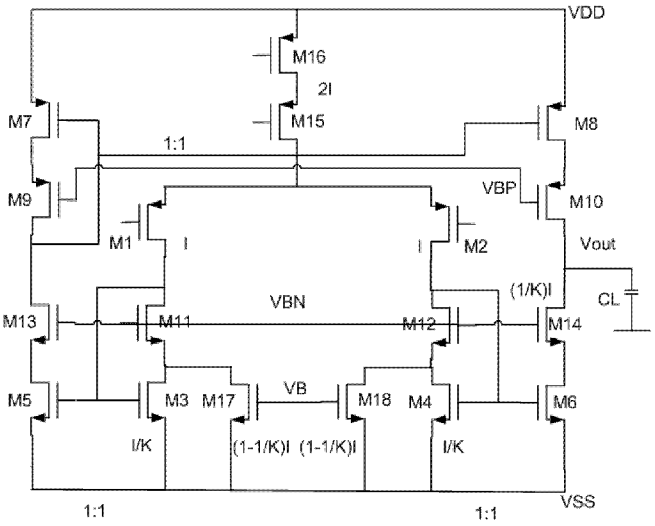

Figure 4. Schematic of OTA

TABLE I. CHARATERISTICS OF OTA (SIMULATION)

Supply voltage	+0.9V/-0.9V
Power consumption	18 μW
Noise [1 Hz,10 kHz]	8.5 μV
CMRR	90 dB
Gain	100.10 dB
Unit gain bandwidth	904 kHz
Load capacitor	15 pF

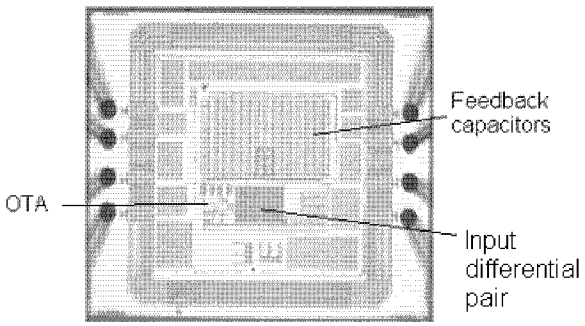

Figure 5. Die of the amplifier chip

The input signal amplitude to the ADC is less than 500mV. The output impedance of the previous LPF to the analog MUX is about 10k ohm. We should choose the width of the switch in the MUX to make the error introduced by the MUX less than 1 LSB of the ADC.

CMOS transmission gate is used as the switch so as to make the turn on resistance of the switch relatively constant regardless of the input signal's level. Because the signal's amplitude after filtering rarely exceeds 500 mV, we can assume that the MOSFETs operate in the triode region. Considering worst case, the turn-on resistance of the NMOS and PMOS is calculated as follows, neglecting the body effect and short channel effects.

$$R_{on} = \frac{1}{\beta \cdot (2V_{DD} - V_{th,NMOS} - |V_{th,PMOS}|)} \qquad \text{(D.4)}$$

$$\text{assume } \frac{W_P}{L_P}\mu_P C_{ox} = \frac{W_n}{L_n}\mu_n C_{ox} = \beta.$$

A dummy NMOS capacitance is inserted in the switch to reduce the charge injection and clock feedthrough.

III. System Architecture for System on Chip

A multi-channel system on a single chip is the next goal. Previous sections presented an analysis of the architecture for one ADC for multiple channels. Now we will consider one ADC per channel architecture.

First, we compare the two architectures, only considering the fundamental components as shown in figure 6. Suppose the signal bandwidth for each channel is 10 kHz, the input bandwidth for one ADC per channel is 10 kHz and the input bandwidth for one ADC supporting two channels is 20 kHz. The overall power consumption requirements for two architectures are same since the power consumption of the ADC doubles if the signal bandwidth doubles if we design ADC just to meet the Nyquist requirement.

For one ADC per channel, the FIFO and digital MUX consume little power. We could also use sigma-delta ADC for each channel, which reduces the order of anti-aliasing filter compared to one ADC for multiple channels. Figure 7 shows the overall architecture for data acquisition system part. Sigma-delta ADC consumes less power for high resolution ADC compared to other architectures [10]. The analog MUX, anti-aliasing filter and buffer in one ADC for multiple channels consumes additional power. So we could see one ADC per channel architecture consumes less power since the digital circuits will consume very little power in the chosen sub-micron CMOS technology. Also, one ADC per channel architecture is more scalable.

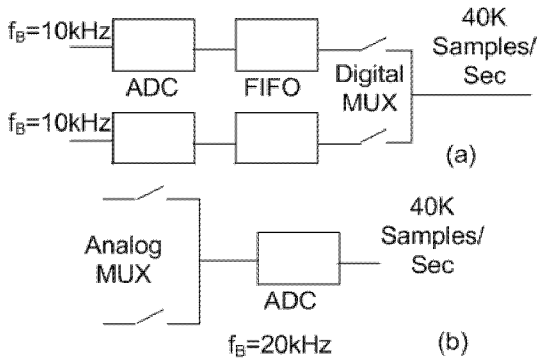

Figure 6. (a) 1 ADC per channel. (b) 1 ADC multiple channel.

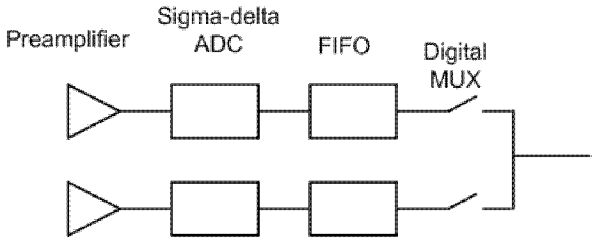

Figure 7. 1 ADC per channel architecture

IV. Conclusion

The preliminary chip design and results of a neural recording system are presented. Two choices of architecture are discussed with their relative merits and demerits. The case of one ADC for multiple channels is analyzed in detail and we propose one ADC per channel architecture for multi channel neural recording system since it is better in terms of power, performance and scalability.

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References

[1] R.A. Andersen et.al., "Recording advances for neural prosthetics", *IEEE EMBC 2004,* Vol. 2, Iss., Vol. 7, pp. 5352- 5355

[2] J. G. Webster, "Medical Instrumentation Application and Design" John Wiley & Sons, Inc. 1998

[3] R.H. Olsson, D.L. Buhl, A.M. Sirota, G.Buzsaki, and K.D. Wise, "Band-tunable and multiplexed integrated circuits for simultaneous recording and stimulation with microelectrode arrays", *IEEE Transactions On Biomedical Engineering,* Vol. 52, No. 7, July 2005, pp. 1303-1311

[4] D.A. Johns, K. Martin, "Analog integrated circuit design", John Wiley & Sons, Inc, 1997

[5] H.-S. Lee, D.A. Hodges, P.R Gray, "A self-calibrating 15 bit CMOS A/D converter", *IEEE J. Solid-State Circuits,*Vol.19, Iss.6, December 2004, pp. 813-819

[6] D.A. Borkholder, "Cell based biosensors using microelectrodes", *Ph.D thesis*, Stanford, 1998

[7] R. Harrison and C. Charles, "A low-power, low-noise CMOS amplifier for neural recording applications", *IEEE J. Solid-State Circuits*, Vol.38, Iss. 6, June 2003, pp. 958-965

[8] P. Mohseni and K. Najafi, "A fully integrated neural recording amplifier with dc input stabilization", *IEEE Trans. Biomed. Eng.*, May 2004, Vol. 51, Iss. 5, pp. 832-837

[9] R.M. Fox, I. Seo, H. Yeo, O. Jeon, "Leveraged current mirror op amp", Analog Integrated Circuits and Signal Processing, Vol. 35, Iss. 1, April 2003, pp. 25 - 31

[10] L. Yao; M.S.J. Steyaert and W. Sansen, "A 1-V 140-µW 88-dB audio sigma-delta modulator in 90-nm CMOS", *IEEE J. Solid-State Circuits,*Vol.39, Iss.11, November 2004, pp. 1809- 1818

[11] E.A. Vittoz, "Micropower Techniques", *Design of analog-digital VLSI circuits for telecommunications and signal processing*, edited by J. Franca and Y. Tsividis, Prentice-Hall, 1994, pp. 53 – 96

[12] P.R. Gray, P.J. Hurst, S. H. Lewis, and R.G. Meyer, "Analysis and design of analog integrated circuits", 4th edition, John Wiley & Sons, Inc, 2001