A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System

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***Abstract*—Recent work in field of neuroprosthetics has demonstrated that by observing the simultaneous activity of many neurons in specific regions of the brain, it is possible to produce control signals that allow animals or humans to drive cursors or prosthetic limbs directly through thoughts. As neuroprosthetic devices transition from experimental to clinical use, there is a need for fully-implantable amplification and telemetry electronics in close proximity to the recording sites. To address these needs, we developed a prototype integrated circuit for wireless neural recording from a 100-channel microelectrode array. The design of both the system-level architecture and the individual circuits were driven by severe power constraints for small implantable devices; chronically heating tissue by only a few degrees Celsius leads to cell death. Due to the high data rate produced by 100 neural signals, the system must perform data reduction as well. We use a combination of a low-power ADC and an array of "spike detectors" to reduce the transmitted data rate while preserving critical information. The complete system receives power and commands (at 6.5 kb/s) wirelessly over a 2.64-MHz inductive link and transmits neural data back at a data rate of 330 kb/s using a fully-integrated 433-MHz FSK transmitter. The 4.7 $\times$ 5.9 mm^2 chip was fabricated in a 0.5-μm 3M2P CMOS process and consumes 13.5 mW of power. While cross-chip interference limits performance in single-chip operation, a two-chip system was used to record neural signals from a Utah Electrode Array in cat cortex and transmit the digitized signals wirelessly to a receiver.**

***Index Terms*—Biomedical electronics, FSK transmitter, low-power circuit design, neural amplifier, neuroprosthetics.**

I. Introduction

In the past decade, neuroscientists and clinicians have begun to use implantable MEMS multielectrode arrays (e.g., [1], [2]) to observe the simultaneous activity of many neurons in the brain. These silicon-based electrode structures are inserted into the cerebral cortex and observe the electrical activity of nearby nerve cells. Neurons communicate with one another using stereotyped voltage pulses known as action potentials or spikes. Each spike has an amplitude of around 100 mV (relative to the extracellular fluid) and a duration of around 250 μs. When observed using an extracellular microelectrode a few tens of microns away, a potential of 50–500 μV can be detected. (Intracellular penetrating electrodes can measure the entire 100 mV signal, but result in cell death within a few minutes and are thus not feasible for chronic implants.) A typical neuron generates 10–100 spikes per second when active. Resting or "spontaneous" activity of neurons ranges up to 1–10 spikes per second.

By observing the action potentials of many neurons in particular regions of the brain responsible for motor planning or control, it is possible to gather enough information to predict hand trajectories in real time during reaching tasks in awake behaving primates [3]–[5]. In a training stage, neural activity is monitored while an animal performs various reaching tasks or other limb movements. Hand or limb movements are carefully monitored and correlated with the simultaneous neural data. Once the correlation between hand movement and neural activity has been determined, the neural activity can be used to drive a robotic arm or a cursor on a screen. Recent clinical trials with paralyzed human volunteers have shown that it is possible to develop neuroprosthetic devices—machines controlled directly by thoughts—if the activity of multiple neurons can be observed [6].

Currently, data is recorded from implanted multielectrode arrays using bundles of fine wires that tether the array to a skull-mounted connector; all electronics for amplification and recording is external to the body. This presents three major barriers to the development of practical neuroprosthetic devices: 1) the transcutaneous connector provides a path for infection; 2) external noise and interfering signals easily couple to the wires conveying weak neural signals ($< 500\ \mu$V) from high-impedance electrodes (> 100 kΩ at 1 kHz); and 3) the connector and external electronics are typically large and bulky compared to the $\sim$5 mm electrode arrays. To eliminate these problems, data from the implanted electrodes should be transmitted out of the body wirelessly. Wireless neural recording systems from the 1990s were built from discrete modules [7], while more recent wireless systems have utilized an integrated circuit for amplification and several off-chip components for power rectification [8]. Recently, a battery-powered system utilizing an IC with an off-chip inductor was used to record and transmit neural signals from an animal using analog FM

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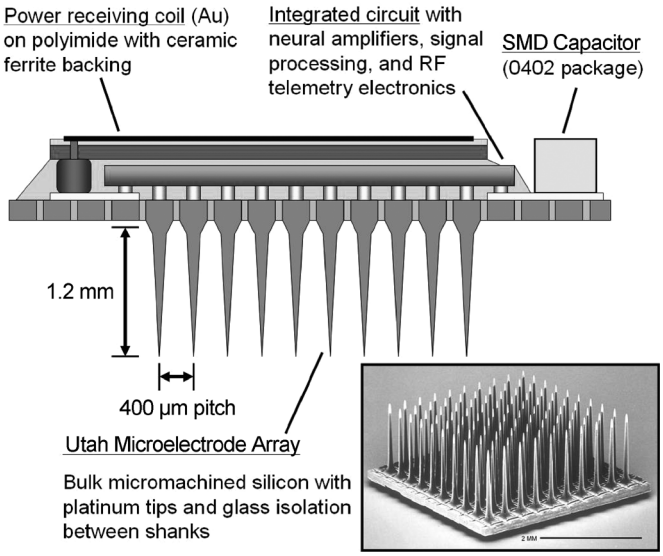

Fig. 1. Complete Integrated Neural Interface (INI) assembly concept. Inset shows Utah Microelectrode Array.

modulation [9]. (Also see [9] for a thorough review of previous wireless biopotential recording systems.)

Wireless neural recording requires electronics at the recording site to amplify, condition, and digitize the neural signals from each electrode. Ideally, these circuits should be powered wirelessly since rechargeable batteries are relatively large and have limited lifetimes. Low power operation ($\sim$10 mW) is essential for any small implanted electronics as elevated temperatures can easily kill the neurons one is trying to observe.

We are developing a wireless, fully-implantable neural recording system to facilitate neuroscience research and neuroprosthetic applications (see Fig. 1). The system is based on the Utah Electrode Array (UEA), a 10×10 array of platinum-tipped silicon extracellular electrodes [2]. This paper describes the development of a mixed-signal integrated circuit (first presented in [10]) that will be flip-chip bonded to the back of the Utah Array. This chip will directly connect to all 100 electrodes, amplify the neural signals from each electrode, digitize spikes and a selected waveform, and transmit the information over an RF link. Power will be delivered to a 5-mm coil mounted on the back of the chip using an inductive link. The entire device will be coated in parylene and silicon carbide to protect it from internal body fluids.

II. System Design

A. Strategies for On-Chip Data Reduction

The description of our chosen system architecture must be prefaced by a discussion of a dominant technical challenge inherent in a multi-channel neural recording system: data rate. Any neural recording device to be used in neuroprosthetic applications will generate data at tremendous rates. To enable prosthetic control in a natural manner, data must be continuously streamed off the implanted device in real time and with little latency. When amplifying neural signals, a bandwidth of 5–10 kHz is typically used to observe the individual spikes. If we assume an ADC sampling rate of 15 kSamples/s and a resolution of 10 bits, each neural signal generates data at a rate of 150 kb/s. A 100-electrode recording device would therefore need to transmit data at a rate of 15 Mb/s. This presents a significant technical hurdle given that extremely low power dissipation ($\sim$10 mW for the entire system) is necessary to avoid heating the surrounding tissue, small size requirements ($<$1 cm) prevent the use of an efficient transmitting antenna, and increased tissue absorption at high frequencies greatly favors telemetry operation below 1 GHz. (It should be noted that optical transcutaneous data transmission using an infrared emitter was demonstrated at data rates of 40 Mb/s, although the power dissipation of 120 mW would prevent it from being used in close proximity to brain tissue [11].)

Given these constraints, we have concluded that data reduction at the level of the implanted device is essential. We chose a simple, power-efficient method for reducing data rate while preserving spike timing information. We perform spike detection by detecting threshold crossings with a comparator and a user-programmable threshold voltage. If the electrode voltage exceeds the threshold, the comparator latches into a logic high state. The comparators are polled and reset roughly once per millisecond, which provides sufficient temporal resolution and results in a total data rate of 100 kb/s for all 100 channels. Of course, the user needs to be able to monitor the analog waveform at any electrode to set the spike detection thresholds appropriately. (Automatic spike-detection circuits have been developed, but were not included on this chip [12], [13].) Thus, we also include an ADC with a 15 kSamples/s sample rate that can digitize one user-selected channel at a time and relay this information (at 150 kb/s) along with all 100 channels of spike detector data over the wireless telemetry link. An analog multiplexer (MUX) connects the selected electrode amplifier output to the ADC. (An alternate approach to neural data reduction is presented in [14].)

B. System Architecture

The overall architecture of the single-chip integrated neural interface (INI) is shown in Fig. 2. The core of the chip is an array of amplifiers that connect to the electrodes and boost the weak extracellular neural signals by 60 dB while isolating frequencies of interest. Each amplifier cell contains a comparator that acts as a spike detector. In our first prototype chip, INI1, a global spike detection threshold was set using one 7-bit DAC. In our second prototype chip, INI2, individual 6-bit DACs were built into each amplifier cell so that different spike detection thresholds could be set for each electrode. An analog MUX is incorporated into the amplifier array, allowing one selected electrode waveform to be routed to a 10-bit ADC. (INI1 used a 9-bit ADC.) The digital data from the ADC and all 100 spike detectors are interleaved into a serial data stream, and this binary stream is used to drive a fully-integrated 433-MHz FSK transmitter.

Power is provided to the chip inductively via an off-chip 5-mm gold-on-polyimide coil [15]. The chip contains a fully-integrated bridge rectifier based on the design by [16], eliminating the need for off-chip diodes. A bandgap-referenced linear voltage regulator provides a steady 3.3 V DC supply for the digital and analog circuits on the chip. Two off-chip

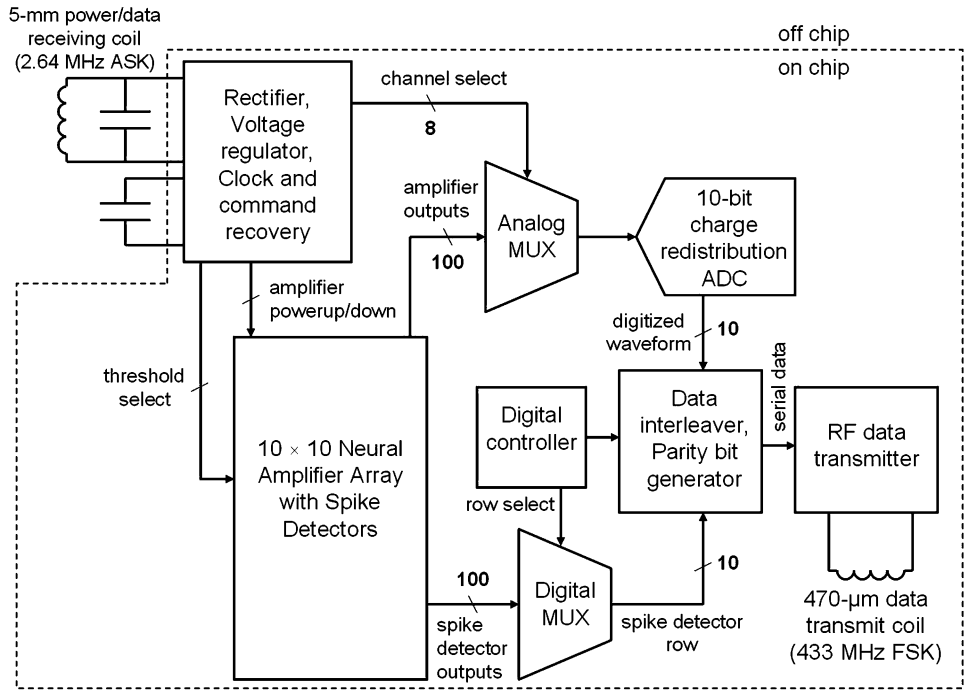

Fig. 2. Integrated Neural Interface system block diagram.

capacitors are needed: one to resonate with the power coil, and another large-valued capacitor to smooth out the unregulated DC supply after rectification. (Small 0402-size surface-mount capacitors will be used.) Commands are sent to the chip by amplitude modulating the 2.64-MHz inductive power signal. On-chip circuits recover this data as well as a system clock from the ac power signal. Since the chip is primarily used to stream neural data out of the body, commands are sent infrequently. Commands may be sent to select which electrode is being digitized by the ADC, to set spike detection thresholds, and to power down any amplifiers connected to electrodes that may not be providing useful neural signals.

The integrated circuits (INI1 and INI2) each measure 4.7 × 5.9 mm^2 and were fabricated in a commercial 0.5-μm 3M2P CMOS process (see Fig. 3). The center of the chip consists of a 10×10 array of amplifiers laid out in a 400 μm pitch, corresponding to the inter-electrode spacing. A bond pad local to each amplifier allows direct connection of the chip to the Utah Electrode Array. Twelve of the 100 platinum-tipped electrodes are used as "ground" or "reference" electrodes; the remaining 88 electrodes are connected to integrated low-noise neural signal amplifiers. In the final assembly of the device, the chip will be bonded face-down on the back of the electrode array, and the 5-mm power coil will be attached to the back of the chip (see Fig. 1). The INI1 chip contains approximately 30 000 transistors and 5000 passives (resistors, capacitors, and inductors); INI2 contains over 63 000 transistors and 5000 passives.

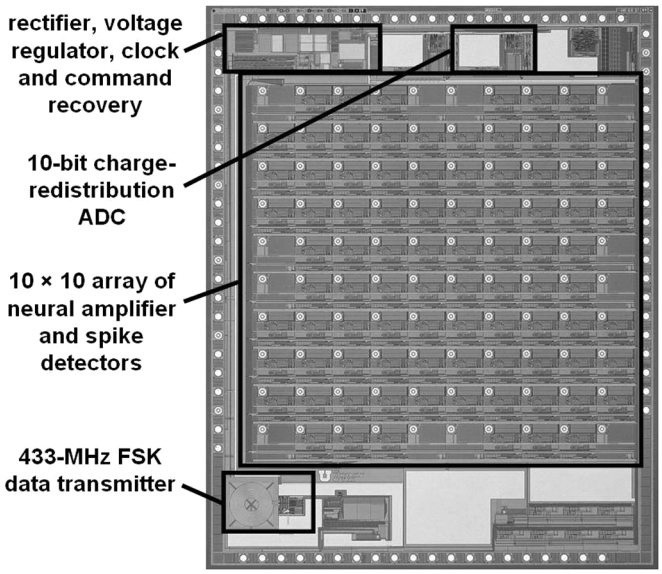

Fig. 3. Die photo of 4.7 mm×5.9 mm integrated neural interface chip (INI2).

III. Wireless Power and Command Transmission

For wireless power transmission, we chose to implement an inductive link operating at 2.64 MHz. The choice of frequency was determined by low tissue absorption in the 1–10 MHz range [17] and the need for particular clock frequencies on the chip (e.g., a system clock of 330 kHz, which is a factor of eight slower than the power signal and thus easily generated). A clock recovery circuit uses a Schmitt trigger and toggle flip-flop to generate a square wave with a 50% duty cycle [18]. The on-chip linear voltage regulator provides a load regulation of 0.15% over a current draw of 2–10 mA. The measured line regulation is less than 0.30%/V for unregulated voltages ranging from 3.5–8.0 V.

We built an off-chip class E amplifier to drive a power transmit coil 2 cm in diameter (31 turns) with an ac current approximately 500 mA in amplitude, which produces a voltage of around 80 Vrms on the 13.4 μH coil. A microcontroller modulates the amplitude of the power coil voltage to send

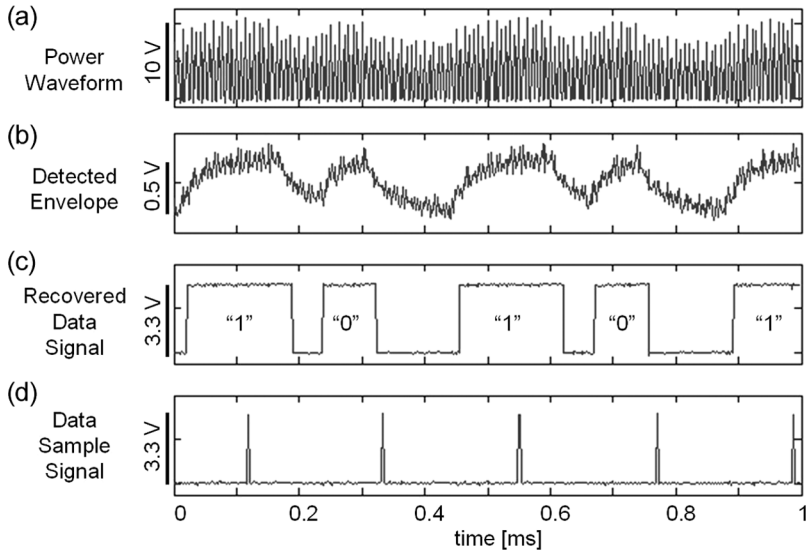

Fig. 4. Command recovery from amplitude-modulated power waveform. (a) Power waveform at one terminal of the power receive coil. (b) Signal from on-chip envelop detector. (c) Binarized amplitude information. (d) Sample signal to distinguish short pulses from long pulses.

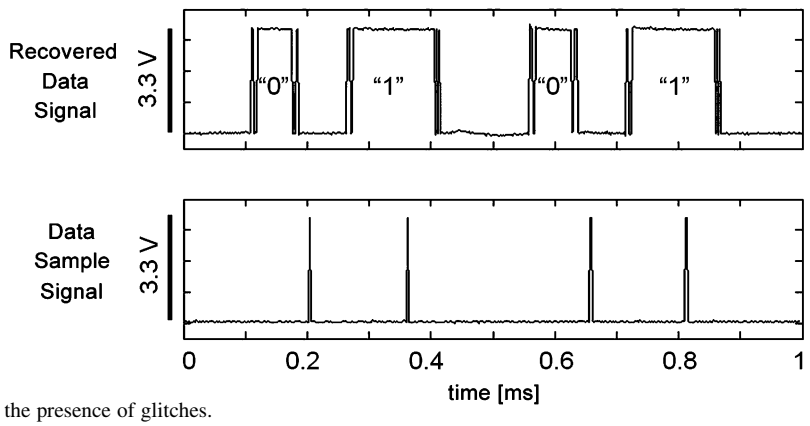

Fig. 5. Robust data recovery in the presence of glitches.

commands to the chip. Data is encoded using an amplitude modulation scheme where short-duration pulses of increased amplitude encode a zero and long-duration pulses of increased amplitude encode a one. (See [19] for a related power and data link.) Fig. 4(a) shows the voltage at one terminal of the power receive coil during amplitude modulation of the transmitted power signal. Since the coil is connected to the on-board full-wave rectifier, negative excursions of the voltage are clamped near ground. (The 2.64-MHz waveform is highly aliased in this oscilloscope capture.) Since the voltage on the power receive coil can reach 8 V or more in amplitude, an integrated capacitor divider is used to attenuate this signal for the command detection circuit. An on-chip envelope detector circuit tracks the amplitude of the coil voltage [see Fig. 4(b)]. A low-pass filter calculates a running average of the envelope, and a comparator determines if the instantaneous output of the envelope detector is higher or lower than the long-term running average. (The minimum required amplitude modulation depth for reliable command transmission was measured to be 9.7%.) The comparator produces a binary signal [see Fig. 4(c)], but this signal may contain glitches at the low-to-high and high-to-low transitions.

A finite state machine (FSM) on the chip implements a robust algorithm for recovering this binary command data in the presence of glitches. The FSM first waits for a low-to-high transition. When this occurs, a timer starts counting. When the timer reaches a specified time (97 μs in our circuit), the binary data stream is sampled. A pulse longer than 97 μs in duration will be sampled as a one, and a pulse shorter than 97 μs in duration will be sampled as a zero. Fig. 4(d) shows the sample signal generated by the FSM. After a falling edge is detected, a second timer is triggered. This timer freezes the FSM for an additional 12 μs before allowing it to return to its initial state and wait for the next low-to-high transition. This waiting period lasts beyond any low-to-high transitions caused by glitches on the falling edge of the pulse and prevents these glitches from falsely retriggering the circuit. Fig. 5 shows the operation of this circuit in response to a synthesized data stream containing large glitches at the rising and falling edges of the binary signal. It is clear from the sample signal that long pulses are being interpreted as ones and short pulses as zeros.

When the FSM first detects ones or zeros being sent over the power waveform it waits for a particular eight-bit header sequence to occur before loading binary command data. This

prevents false commands from being sent by occasional amplitude fluctuations due to relative movement of the power transmit and receive coils. After the correct eight-bit header has been detected, the FSM begins shifting received bits into a long shift register that is distributed throughout the chip. Any configurable circuit on the chip is connected to this serial shift register. Each shift register cell contains two latches. One "external" latch is configured to shift data along the path, and the other "internal" latch is connected to the circuitry to be controlled or configured (e.g., a DAC to set a spike detection threshold). The internal latch is not affected by new command data being shifted through the external latches. When the FSM has received a specified number of command bits (corresponding to the total number of state bits on the chip), it issues a global "load" signal to all the cells in the shift register. This "load" signal causes the contents of the external latches to be parallel loaded into the internal latches so that the entire chip changes state in one clock cycle. More information on the power and data recovery circuits can be found in [20].

This is not the most efficient means to send commands to the chip, as every state bit on the chip must be sent even if only one bit needs to be changed. However, it is extremely simple to implement on the chip and does not incur a serious time penalty since command data can be sent to the chip at rates as high as 6.5 kb/s. In the INI2 chip, there are 678 bits of state on the chip, and a complete programming cycle can be completed in less than 300 ms. Since commands are only used to configure the chip, programming is infrequent and therefore programming time need not be optimized.

IV. Spike Recording and Detection

A. Neural Signal Amplification

Due to the microvolt level of spikes recorded extracellularly, neural signals must be amplified before spike detection or digitization can be accomplished. Electrochemical effects at the tissue-electrode interface can produce DC potentials of 1 V or more, so electrodes must be ac coupled to the amplifiers to eliminate this offset [21]. Neural spike trains contain most of their energy in the 300 Hz–5 kHz range, so amplifiers should reject signals outside of this band. Low-frequency signals in the 1 Hz–100 Hz range known as local field potentials (LFPs) can be measured on electrodes as well [22]. These signals represent the synchronous firing of many neurons throughout a region several hundred microns from the electrode. These signals have also been shown to be useful for neuroprosthetic applications [23], [24] and in previous work we have developed a circuit to isolate LFP signals in narrow bands and calculate their energy [25]. However, LFP detection circuitry was not included on the INI chips, and the low-frequency LFP signals must be removed to facilitate spike detection.

Due to the small amplitude of detectable spikes (as small as 50 μV), it is essential to design a neural signal amplifier with low input-referred noise. However, the severe power restrictions imposed on small implantable devices limits our ability to simply turn up bias currents to lower amplifier noise, especially since the basic amplifier circuit will be repeated many times across the chip. To optimize the trade-off between power dissipation and

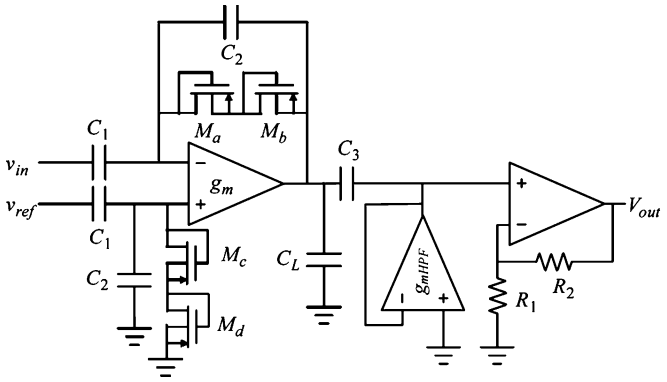

Fig. 6. Schematic of neural signal amplifier. A 40-dB front-end amplifier is followed by a g_m-C high-pass filter and finally a 20-dB gain stage. Resistors are made from high-resistance polysilicon ($R1 = 40\,\mathrm{k}\Omega$, $R2 = 360\,\mathrm{k}\Omega$).

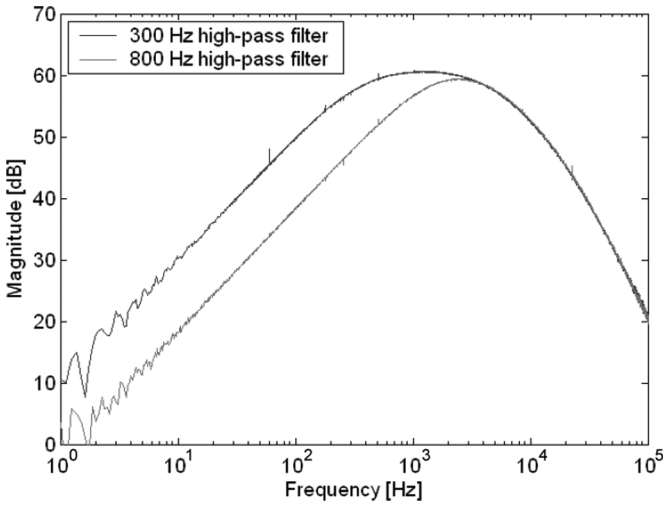

Fig. 7. Measured transfer function of neural amplifier with programmable high-pass filter pole.

input-referred noise, we used circuits and techniques described in [26], where the differential pair transistors in a current-mirror OTA (operational transconductance amplifier) are operated in weak inversion (where g_m/I_D is maximum) and the current mirror transistors in the OTA are operated far into strong inversion (where g_m/I_D is greatly reduced). To reduce $1/\mathrm{f}$ noise, large pMOS devices (300/1.5 μm) are used in the differential pair of the front-end amplifier. The complete 60-dB amplifier is shown in Fig. 6; more details on the design are given in [26].

Since we wish to eliminate LFP signals before spike detection, we use a g_m-C high-pass filter after the first 40-dB stage of amplification. Since this circuit operates in weak inversion, we use the technique of "bump linearization" to extend the linear range [27]. A second gain stage adds 20 dB of additional gain. The bias current to the high-pass filter is set by a current-mode DAC and allows the user to program a pole frequency between 30 Hz and 1 kHz and calibrate this current to account for chip-to-chip variation. Fig. 7 shows the transfer function of this amplifier measured at two bias current settings, resulting in high-pass poles at 300 Hz and 800 Hz. Cutoff frequencies higher than 300 Hz may be useful if this device is used in peripheral nerve, near large muscles. The EMG (electromyogram) signals generated by muscles have significant signal power below 1 kHz,

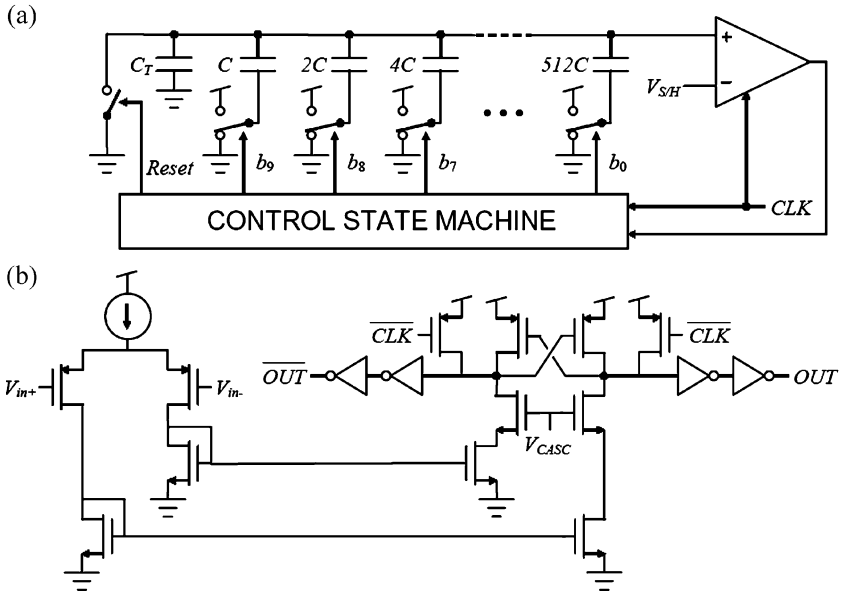

Fig. 8. (a) Schematic of successive-approximation ADC with capacitive DAC. The state machine controls the switches for b_0–b_9 and *Reset*, and senses the output of the comparator. (b) Schematic of track-and-latch comparator used in the ADC. A preamplifier (left) and nMOS cascode devices are used to minimize kickback.

so a higher high-pass cutoff frequency might help to reduce interference from this source. The low-pass poles of the amplifier are set at 5 kHz by the OTA in the first gain stage and the op-amp in the second gain stage. The amplifiers have a measured input-referred noise of 5.1 μVrms, and each amplifier draws only 12.8 μA of supply current. Individual amplifiers may be powered down with a command signal so that unused electrode channels do not dissipate power.

B. Spike Detection and Waveform Digitization

The output of the amplifier is connected to a comparator that performs binary spike detection. An area-efficient, current-mode 6-bit DAC local to each amplifier cell is used to set the spike detection threshold. These DACs have measured INL and DNL errors less than 0.25 LSB across their entire operating range. (See [28] for a similar DAC design.) The amplifier, spike detector, and threshold DAC had to be designed carefully to fit in the 400 μm $\times$ 400 μm area allotment to allow these circuits to match up with the pitch of the Utah Electrode Array for flip-chip bonding [29]. The output of each amplifier is also connected to an analog MUX to allow a 10-bit ADC to sample the selected neural waveform.

To minimize power consumption by the ADC, we chose a successive-approximation, charge-redistribution architecture [see Fig. 8(a)]. For the capacitive DAC, we use an array of poly-poly capacitors with a unit capacitance of $C \approx 33$ fF; the entire array consumes 0.15 mm^2 of chip area and is carefully designed to account for parasitic capacitance in the wiring. While the extra capacitor C_T is typically set equal to C to enable conversion over the entire range from $V_{\rm DD}$ to ground, we set C_T to approximately one-fourth of the total capacitance in the array (i.e., $256C$) to limit the conversion range to $0.75V_{\rm DD}$ since amplifier output voltages will not exceed this range. The track-and-latch comparator used in the ADC uses a differential preamplifier stage and nMOS cascode devices to minimize kickback [see Fig. 8(b)]. The comparator latches a valid output when CLK is low; only the non-inverting output is used, but the inverting output is included for symmetry of parasitic effects. The ADC is capable of digitizing signals at 15 kSamples/s while dissipating less than 100 μW of power [30]. The ADC has measured INL and DNL errors less than 0.6 LSB for codes 60–925 (out of 1024 total codes).

Fig. 9 shows neural data recorded from monkey premotor cortex (courtesy of K. Shenoy, Stanford University) played through a neural amplifier on the chip using an arbitrary waveform generator with an attenuation circuit to achieve microvolt-level signals at the amplifier input. The ADC waveform reconstruction and spike detector output signal are also shown. In this experiment, chip was powered wirelessly via a coil, but the digital output of the ADC was recorded directly from the chip before it passed to the RF transmitter.

V. FSK Data Transmission

Our chip continuously generates spike detector data for all 100 electrodes (though 12 of the electrodes are used as ground or reference wires) and a 15 kSample/s 10-bit digitized analog waveform from one selected electrode. This data must be transmitted out of the body wirelessly. To accomplish this, we use a fully-integrated 433-MHz FSK transmitter. We chose our operating frequency below 1 GHz to minimize attenuation of high frequencies by tissue and to operate near the FCC-approved MICS (Medical Implant Communication System) band at 402–405 MHz if we decide to use this band in the future.

First, an FSM on the chip samples and interleaves the spike detector data with the ADC data. Parity bits are added to facilitate error detection, and a data frame containing 352 bits is assembled. Each data frame contains 16 successive ADC samples (i.e., 1.07 ms of the neural waveform), all 100 spike detector output bits, parity bits, and frame markers to permit data synchronization at the receiver (see Fig. 10). This data stream is

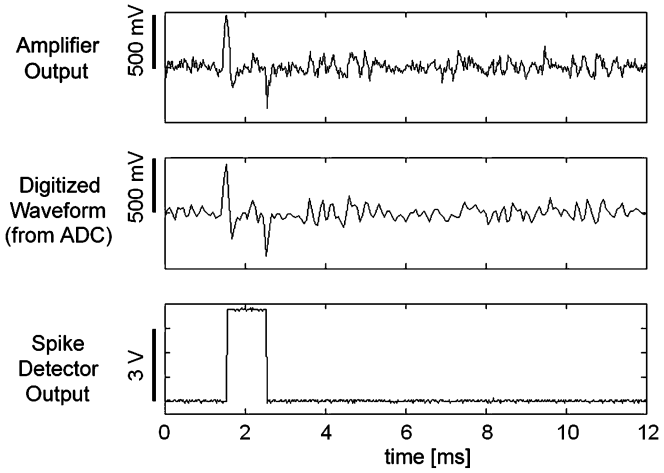

Fig. 9. Response of wireless-powered chip to neural waveform played from waveform generator: analog output of a neural signal amplifier (top), waveform reconstructed from ADC output (middle), output of corresponding spike detector (bottom). Data was taken while chip was powered wirelessly.

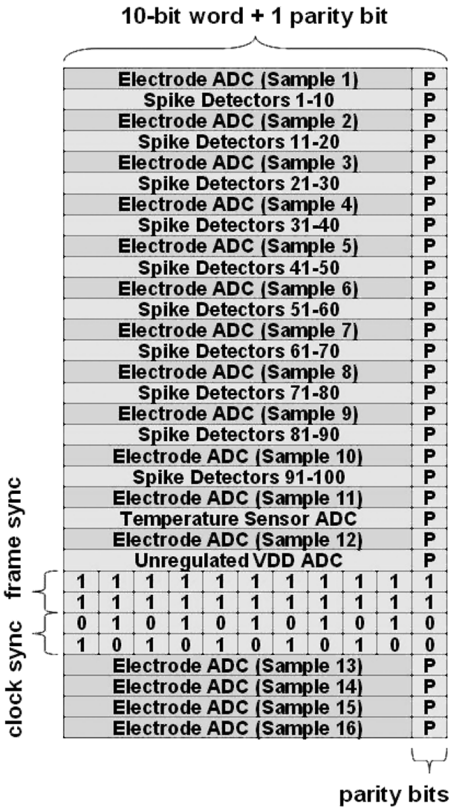

Fig. 10. Single 352-bit data frame of interleaved ADC and spike detector data used for FSK transmission.

sent to the FSK transmitter in a serial bit stream at a rate of 330 kb/s.

Due to power constraints, we designed a bare-bones FSK transmitter consisting of little more than a power-optimized voltage-controlled oscillator (VCO) with an integrated planar spiral inductor (see Fig. 11). The capacitors in the LC tank circuit are accumulation-mode MOS varactors [31]; the gross operating frequency is adjusted by changing the voltage V_{TUNE}, and modulation is achieved by sending a digital signal

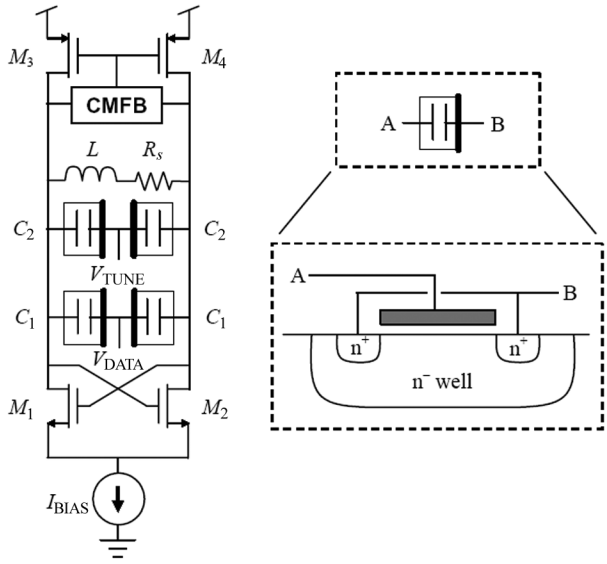

Fig. 11. Schematic of VCO used for FSK transmission. Accumulation-mode varactors are used to vary the frequency of oscillation.

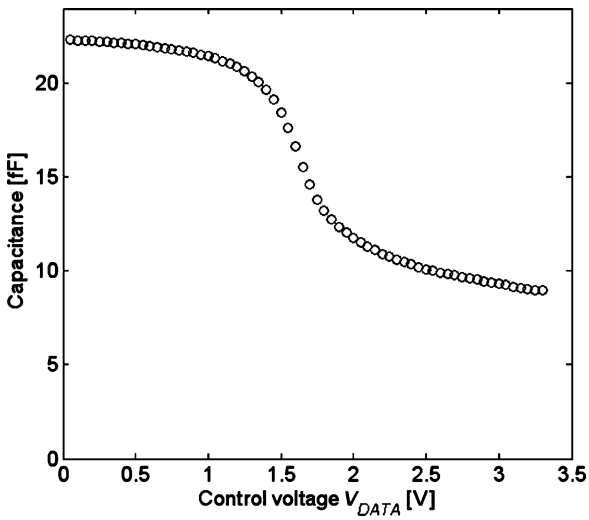

Fig. 12. Measured $C-V$ characteristic of accumulation-mode varactor $(C1)$ used in VCO.

on V_{DATA} (see Fig. 12). The C_1 capacitors are drawn 100 times smaller than the C_2 capacitors, permitting the large (3.3 V) V_{DATA} signal to modulate the frequency by an appropriate Δf for FSK operation. The transistors in the VCO supply enough power to the LC tank circuit to overcome losses and sustain oscillations. The dominant losses in the integrated LC tank are due to the series resistance of the planar inductor. To minimize this resistance, we use the top two metal layers (of our three metal layer process) to implement the inductor. We minimize substrate losses through the use of a polysilicon ground shield with radial slits to minimize eddy currents in the shield [32].

An analysis of this VCO shows that the power required to sustain oscillations is determined by the equivalent parallel resistance R_p of the LC tank, where R_p is related to the series resistance of the inductor, R_s, by $R_p = R_s(Q^2+1)$, and Q is the quality factor of the inductor given by $Q = \omega L/R_s$. Specifically, the power consumption of the VCO is proportional to

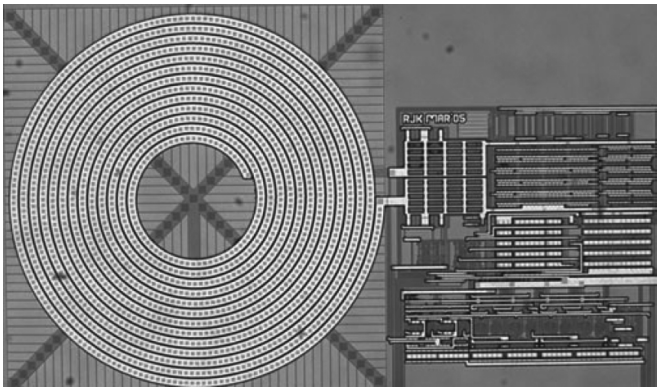

Fig. 13. Photo of FSK transmitter. The 54-nH inductor measures 470 μm in diameter and has $Q \approx 3$ at 433 MHz.

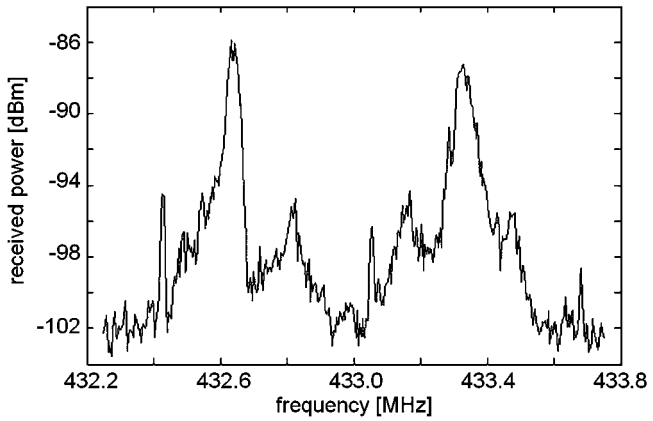

Fig. 14. Spectrum of FSK data transmitter sending a typical data frame at 330 kb/s. Dipole antenna was positioned 13 cm from chip.

$1/R_p^2$. We developed a search algorithm to find an inductor that maximized R_p at the operating frequency while maintaining an acceptably high self-resonant frequency. Optimizing specifically for high R_p can result in significant power savings over the more commonly-used method of optimizing only for high inductor Q without considering R_p [33]. The resulting spiral inductor has a diameter of 470 μm, an inductance of 54 nH, and $Q \approx 3$ at 433 MHz (see Fig. 13). In the INI1 chip, the VCO requires 1.2 mA of operating current during normal operation. In the INI2 chip, we replaced the common-mode feedback (CMFB) circuit shown in Fig. 11 with cross-coupled pMOS transistors. This lowered the operating current to 550 μA.

The VCO operates in an open-loop manner with no phase-locked loop (PLL) to set its frequency relative to a stable reference, such as the clock recovered from the ac power signal. An on-chip 10-bit DAC allows the user to adjust the operating frequency. This approach should result in stable operation when the device is implanted due to the relatively constant environmental temperature. We measured the frequency drift of the VCO to be -400 ppm/°C. For body temperatures ranging from 36 °C–40 °C, this would result in a carrier frequency shift of 0.16%, or 690 kHz. Initial plans to incorporate a PLL into the chip revealed unacceptably high power dissipation by the required frequency divider, despite attempts at low power design.

Since our complete assembled system will measure less than 8 mm in any dimension, we cannot use an efficient transmitting antenna. Instead, we rely on the magnetic field generated by the 470-μm VCO inductor to transmit the signal a short distance. In benchtop experiments using a half-wave resonant dipole receiving antenna, we receive the FSK signal at -85 dBm at a distance of 13 cm (see Fig. 14). To demodulate the FSK data, we use an Analog Devices ADF7025 evaluation board. Fig. 15 shows a data stream as it is sent to the FSK transmitter (top) and then received at the demodulator (middle) which also recovers a data clock (bottom) using an antenna 13 cm away. In this case, we measure a bit error rate (BER) of $10^{-2.5} = 0.003$. While this is higher than desired, it is not likely to seriously impede the operation of a practical neuroprosthetic system due to the stochastic nature of neural signals. We are currently investigating the use of error-correcting codes that can be implemented with minimal on-chip hardware (e.g., convolutional codes) to improve the BER.

VI. Wireless Recording From Cortex

While all the subsystems on our chips work well in isolation, at the system level we have with problems of crosstalk and digital interference with the sensitive analog circuits. When the digital FSMs and ADCs are running, interference appears on the neural amplifiers. Noise in the on-chip reference voltages also degrades neural amplifier performance. We have tracked down likely paths for this interference, and we believe they can be fixed through better layout and isolation of reference voltages. The FSK transmitter also exhibits diminished performance (increased BER) when all digital systems on the chip are active. Again, we believe this can be improved through more careful isolation of reference voltages used across the chip.

While the digital interference did not prevent us from seeing the large (nearly 500 μV at the input to the amplifier) pre-recorded neural signals in Fig. 9, most spikes recorded with extracellular electrodes have amplitudes in the range of 50–150 μV. In order to test our system in an *in vivo* experiment, we used two INI chips in concert: we used an amplifier from one chip to boost the signal by 60 dB, and we used the ADC and FSK transmitter on a second chip to digitize and transmit the neural data (see Fig. 16). Since the digital systems were turned off on the first chip, digital interference did not affect the neural signal amplifier. This two-chip configuration did not permit the use of the spike detectors, and it required that we power the chips from a battery instead of a coil.

We obtained neural signals from a 10×10 UEA implanted in the auditory cortex of a cat. The UEA was attached to a head-mounted transdermal connector via 100 insulated wires, represented by the dotted line in Fig. 16. A shielded cable approximately 40 cm in length was used to connect the neural signal amplifier to one selected electrode from the 100-pin connector. The frame of the connector, which was in contact with the animal's skin and skull, was tied to ground. The chips, which were packaged in ceramic LCC packages, were mounted on small printed circuit boards with the output of the amplifier from the first chip connected to the ADC input of the second chip. A resonant dipole receiving antenna was positioned 2 cm from the second chip. The demodulator/receiver recovered a 330 kb/s binary data from the 433-MHz FSK signal. A custom microcontroller system located and interpreted data frames (see Fig. 10)

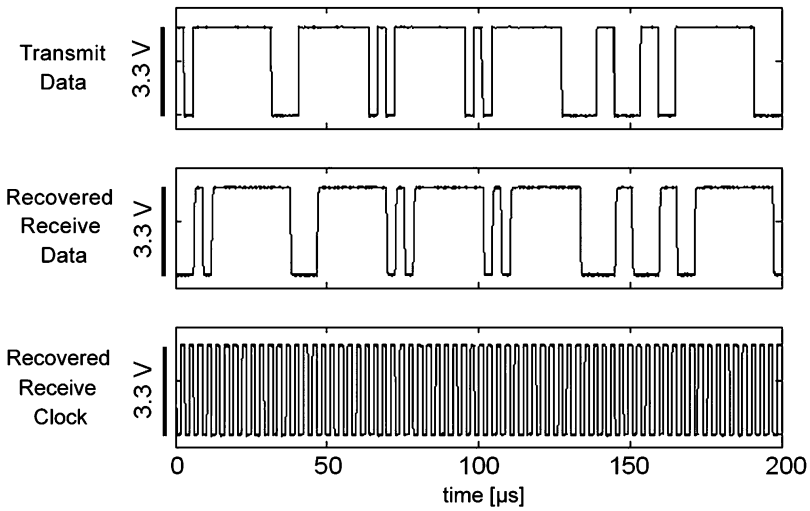

Fig. 15. Transmitted (top) and recovered data (middle) and clock (bottom) streams. The receiving antenna was positioned 13 cm from the chip.

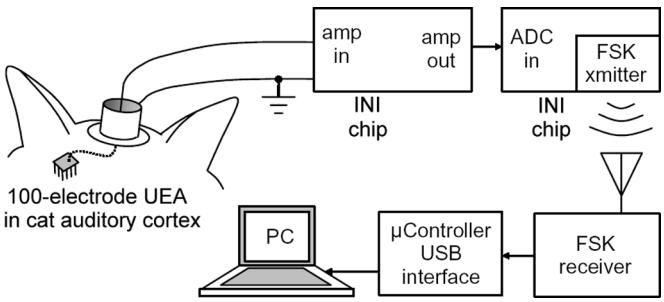

Fig. 16. Diagram of wireless cortical recording experiment. One INI chip was used to amplify the neural signal by 60 dB. A second INI chip digitized and transmitted the signal to an antenna 2 cm away.

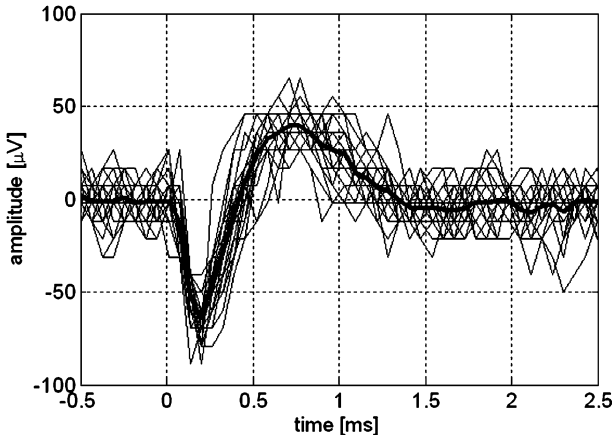

Fig. 17. Electrode-referred neural signals recorded from auditory cortex of cat using a Utah Electrode Array and transmitted wirelessly. The figure shows 30 superimposed spikes along with the average waveform (bold line).

in the binary data stream, and sent the digitized neural signal to a PC via a USB connection.

Fig. 17 shows 30 superimposed neural spikes (with the mean waveform shown as a bold line) recorded from an electrode on the UEA and transmitted wirelessly 2 cm to a receiving antenna and FSK demodulator/receiver. The spikes have been aligned and superimposed in software to facilitate comparison and analysis. We wirelessly recorded neural signals from the same UEA in the same animal twice a week over a period of five weeks. As of this writing, the animal is still healthy and we continue to record signals using a battery-powered, two-chip wireless recording system. Future versions of the chip should permit fully-integrated, coil-powered recording from live cells.

VII. Conclusion

The complete INI1 chip dissipates 13.5 mW of power when the unregulated DC voltage is at its minimum allowable level of 3.55 V. (Since the efficiency of linear voltage regulators decreases with higher unregulated voltage, it is desirable to operate at the lowest allowable coil voltage; at 3.55 V, the regulator consumes about 7% of the total system power.) The FSK transmitter consumes 50% of this power, and the low-noise neural signal amplifiers consume 30% with all amplifiers powered up. The transmitter power could be reduced by using a process with a thick-metal option to increase inductor Q. Moving to a more advanced process with smaller feature size and lower threshold voltages would also reduce power consumption by allowing the chip to operate at a lower supply voltage.

As discussed in the previous section, interference between digital and analog subsystems of our chip currently limits performance. While an SOI technology would allow for better isolation, we do not believe that substrate coupling is the dominant factor in the interference we observe. Fully-differential design of the amplifiers and ADC would likely reduce the impact of digital interference, but space limitations imposed by the 400-μm electrode pitch prevented us from using fully-differential circuits in these chips.

The design of any implantable neural recording device for neuroprosthetic applications is driven by two dominant factors. First, the system is severely limited in its power dissipation due

to tissue heating concerns. Second, large amounts of continuously streaming data must be transmitted wirelessly out of the body with very little latency. These two concerns dictate almost every aspect of circuit and system-level design. Power limitations strongly suggest that the implanted device perform only the minimum required functions of amplification, data reduction and/or compression, and telemetry; any additional computation is best performed outside the body where size and heat dissipation is not as much of a concern. Future neural recording systems may use specialized circuits to isolate and record LFP energy [25] or perhaps perform spike sorting—distinguishing between several distinct neurons recorded by a single electrode on the basis of their action potential shapes [34], [35]. Adding spike sorting does improve the accuracy of neuroprosthetic control somewhat, but at a substantial cost in terms of system complexity. A "middle ground" approach such as transmitting a small number of spike "features" and then clustering the spikes on the basis of these extracted features using external computational power may be the best solution when power is taken into account. Whatever the solution to these problems, the field of neuroprosthetics poses interesting challenges for integrated circuit designers in the years ahead.

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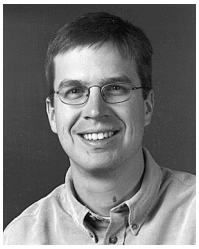

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