ABSTRACT

DAGTEKIN, MUSTAFA. A Chopper Modulated Amplifier System Design for *in vitro* Neural Recording. (Under the direction of Robert J. Trew.)

Neural recording systems measure very low-amplitude signals of less than 5 kHz bandwidth. Low-frequency noise processes such as flicker noise and DC offset can degrade the quality of recordings made by such systems. A chopper modulated amplifier system is described and shown to reduce the flicker noise in neural recording systems by 10 to 20 dB. The amplifier system was implemented using the MOSIS ABN 1.5 micron technology. While the amplifier system contained an imperfection that prevented it from working with actual tissue samples, it worked well enough to prove that chopper modulation does reduce flicker noise appreciably. All of the details are presented along with studies of gate-metal-free transistors and custom-made MOSIS-based recording electrodes.

A CHOPPER MODULATED AMPLIFIER SYSTEM DESIGN FOR *IN VITRO* NEURAL RECORDING

by
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DEDICATION

I dedicate this thesis to my grandfathers, Fehmi Dağtekin and Abdullah Dağtekin. Both of them passed away while I was in the PhD program.

BIOGRAPHY

Mustafa Dagtekin, son of Hatice and Ahmet, was born in a small village called Hacıhüseyinler in Elazığ, Turkey. In 1996, he received a B.Sc. degree in Electronics and Telecommunications Engineering at Istanbul Technical University. After starting his Master's program in Biomedical Engineering at Bosphorus University he was awarded by Turkish Ministry of Education a scholarship for graduate education in US. He attended North Carolina State University and got his M.Sc. degree in Computer Engineering in 1999. He finished his PhD program in 2006. His research interests include analog and digital IC Design, board level systems design, FPGAs and biomedical devices.

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Chapter I. Introduction

Since the beginning of the twentieth century, biologists have been trying to characterize the electrical activity in animal cells that have excitable membranes. The reason that this is important is because it helps scientists understand how nerves work, how the brain works, and how the brain controls bodily functions. It also helps us to diagnose and treat nervous system disorders.

A powerful approach to the characterization of cellular electrical activity is electrical recording from cells or living tissues. Depending on the research goal, the scientist may decide to perform neural recording on a complete live animal (*in vivo*), a tissue sample (*in vitro*), or extracted cells (*in vitro*). Neural recording *in vivo* provides the scientist with the ability to study nervous system diseases, determine how nerves and muscles work, and evaluate an animal's responses to external stimuli. Use of tissue samples simplifies the recording and analysis of the subject. A typical tissue sample would be a slice of brain, a portion of the nervous system, or a slice of the retina. Without the rest of the animal present it is possible to stimulate the tissue electrically or chemically and determine how it reacts. This can be an important tool in the creation of electrical models of the tissue. For example, Hodgkin and Huxley used neural recording of the giant axon of a squid to create models of excitable membranes. Neural recording of extracted cells provides the ability to determine how a cell behaves when it is separated from its host. One common application of the neural recording of extracted cells is to gather information about the characteristics of ion channels.

The object of the research described in this dissertation is to provide improvements in the methods used for performing neural recording. Neural recording is a form of measurement, and all measurement systems contain imperfections. By minimizing these imperfections we can maximize the quality of the results. The electrical information measured by neural recording systems consists mainly of low-frequency signals, and the amplifiers used are generally MOSFET-based. MOSFETS are well-known to be prodigious producers of *1/f*, or

flicker noise, a noise process that produces increasing noise as the frequency is reduced. In the past, to mitigate this problem designers have employed very large transistors --- which reduces the flicker noise generated by the transistors --- or employed filtering. Large transistors take up a lot of space which limits the number of channels that can be simultaneously recorded. Filtering loses information in addition to taking up extra space. Instead, the approach proposed here is to use the well-known chopper modulation technique to reduce the effects of low-frequency noise generated by the input stages of the amplifiers. This provides a significant reduction in the required area and therefore allows more channels to be simultaneously recorded.

The novel contributions of this work include:

- demonstration that chopper modulation does reduce flicker noise in neural recording systems, resulting in smaller layouts and therefore greater channel density
- ASIC design of amplifier system
- design of a gate-metal-free MOSFET with stimulation electrodes
- design of electrodes using a commercial manufacturing process (MOSIS)

In the next chapter background information is provided on the most common cultured-cell recording methods, information about the associated electrical measurement systems and low-frequency noise issues. In the third chapter, some methods to combat the noise problem will be provided. I provide a practical implementation of a neural recording system that uses the suggested chopper modulation technique and the results that show that it provides the predicted benefits. I end with a discussion of the problems encountered implementing our techniques, and provide solutions for these problems.

Chapter II. Literature Review

2.1 Introduction

The focus of this thesis is *in vitro* electrical recording of cultured cells. In this chapter some background for several recording methods will be presented. These methods include those that involve extracellular electrodes, impaling intracellular microelectrodes, patch clamping, planar microelectrode array recording and neuron-transistor recording.

Neural signals in general have a very small bandwidth, usually no more than a few kHz, so low frequency noise can be a very important consideration for recording quality. Different types of low frequency noise sources will be presented. Afterwards, some methods of removing this unwanted noise will be studied.

The noise removal techniques themselves sometimes create additional problems. Those issues will also be reviewed and some solutions will be presented.

2.2 Cultured Cell Recording Methods

Researchers began to culture tissue and cells outside of the body in the beginning of the 20th century [1]. The introduction of the model of an excitable membrane by Hodgkin and Huxley [2] — for which they were awarded a Nobel Prize — was a very important technical advance. It made it easier for researchers to study and understand the excitable membranes of cells and recording electrical activity from them. In this chapter, several ways to record from cells *in vitro* will be examined and categorized. The methods introduced here apply only to recordings of isolated nerves, cultured cells and tissue-slices.

2.2.1 Extracellular and Intracellular Electrode Recordings

As soon as researchers realized that nerve cells exhibit electrical activity, finding ways to measure these signals became very important. In the case of cultured nerve cells or tissue slices, using electrodes with very small tips became a necessity for confining the measurement location to a small area. Indeed the term "microelectrode" emphasizes the fact that the diameter of the tips of these electrodes is on the order of microns.

In extracellular recording, electrodes are placed in close proximity to a single cell or a group of cells without disturbing any cell membrane. In intracellular recording, sharp microelectrodes are used to punch through the membrane of a cell. Microelectrodes can be made of metal, or they might come in the form of a glass pipette [3] with a very small opening at the end of the tip. Glass microelectrodes are filled with a saline conducting KCl solution that is compatible with the intracellular fluid.

2.2.2 The Patch-Clamp Method

Extracellular and intracellular recording are limited because they are inefficient or require large cells or membrane areas. The patch-clamp method, which was first introduced by Neher and Sakmann in 1976 [4], works for fairly small cells; even for a single ion channel. The patch-clamp technique earned Neher and Sakmann the Nobel Prize in 1992.

The patch-clamp technique essentially consists of patching the tip of an electrolyte-filled pipette to the membrane of a cell, clamping it to a preset voltage, and measuring the resulting current.

There are five different configurations, which are called "whole-cell," "cell-attached," "inside-out," "outside-out," and "permeabilized-patch whole-cell" recordings, which are shown in Figure 1. The cell-attached method is the least invasive configuration of all. It involves a mild suction of a small patch of membrane that contains a single or a small

number of ion channels into the pipette tip, which seals the membrane completely. During an ion flux, almost all of the ions flowing through the channel will move through the pipette's tip. If the suction is strong enough, the membrane will break and the tip of the pipette will become continuous with the whole membrane, which results in what is called a whole-cell patch. If a piece of the membrane is detached from the whole cell and the inner face of the detached portion is exposed to a solution, it is now an inside-out patch. The outside-out configuration is obtained by slowly pulling the membrane away from both sides of a whole-cell configured patch so that the external faces of the membrane are facing the solution [5].

The permeabilized-patch whole-cell configuration results when the membrane patch is made permeable by adding antibiotics to the pipette solution that create artificial ion channels while the patch is in the cell-attached configuration [6].

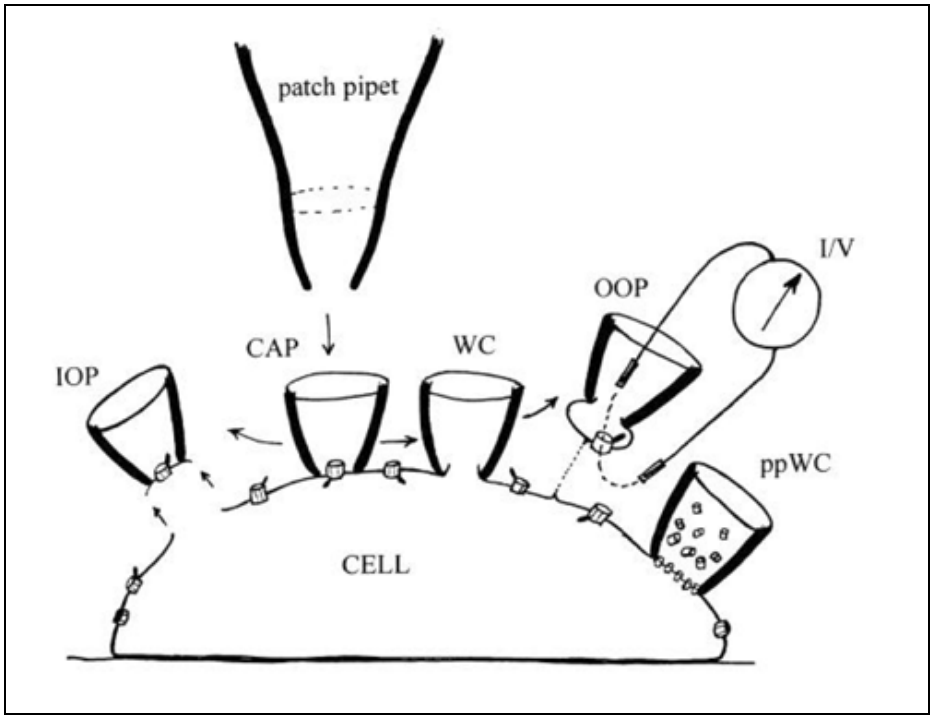

Figure 1. Patch-clamping [5].

2.2.3 Planar Microelectrodes

Although using extracellular electrodes are commonly used to record from populations of excitable cells and intracellular microelectrodes or the patch-clamp method to record from single neurons, there are many disadvantages to these techniques that lead researchers to look for non-invasive solutions. For example, the patch-clamp technique cannot be used for long term recordings, it is not easily used *in vivo*, and only a single cell can be observed at any given time.

In 1972, Thomas, et. al. introduced [7] the concept of planar microelectrodes. A planar microelectrode is a thin-film deposit of gold or platinum on a glass substrate. The planar microelectrode is enclosed in a Petri dish or a glass chamber of some sort. The container is filled with an electrolyte, and the sample is then placed upon the electrode. Generally, planar microelectrodes are implemented in arrays. Planar microelectrodes are non-invasive, can accommodate large numbers of cells, and are simple to implement.

A metal electrode is not generally inert to the electrolyte medium into which it is immersed. There is generally an electrochemical reaction between the electrode and electrolyte [10] [8] [9]. When an unbiased metal item is dipped into an electrolyte, several chemical reactions start at the interface of the metal and the liquid. One of these reactions is *oxidation,* where metal *donors* give out an electron and an *acceptor,* which are metal ions. This reaction is shown in (1). In this equation, donor A gives out an acceptor, A^+ and an electron, e^-.

$$A \rightarrow A^+ + e^- \tag{1}$$

Donated electrons will accumulate at the edge of the metal, because electrons repel each other and are attracted to the metal surface. The ions in the electrolyte will align themselves by forming a double layer called as *inner Helmholtz plane (IHP)* and *outer Helmholtz plane (OHP)* as seen in Figure 2. The space charge layer formed in this equilibrium is usually

modeled as a capacitance known as the "interfacial capacitance." There is equal current flow in both directions which results in zero net current.

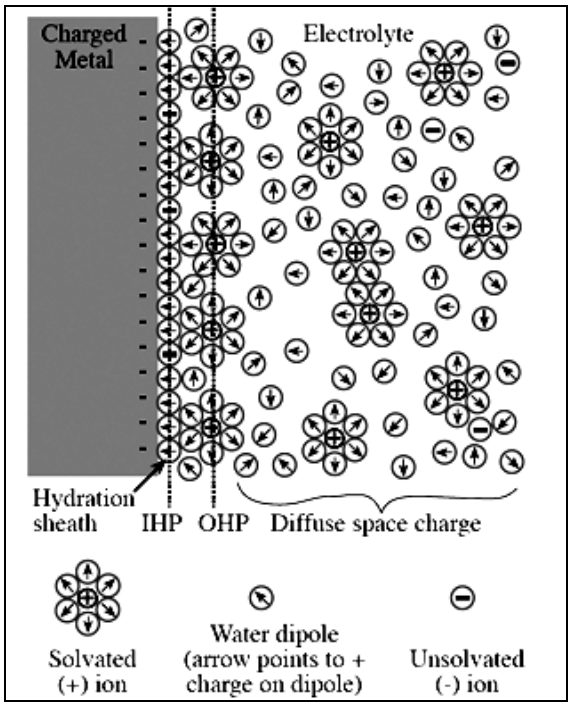

Figure 2. Double Layer [10]

If a DC potential is applied across the interface, there will be a current flow across the plate [10] [11] so we need to add a resistive path to our model. If the potential difference is relatively small, the current flow will be linearly related to the voltage. The equivalent resistance is called "charge transfer resistance."

There is also some impedance effects that is caused by diffusion. This effect has been modeled by Warburg [11] using a resistor and capacitor in parallel (shown as R_w and C_w in Figure 3). He also suggested that this impedance must be in series with the charge transfer resistance [11].

Spreading resistance, which is shown as R_s in Figure 3, is modeled for the current that spread outward from the electrode to the solution it is in. There are several methods proposed to calculate this resistance [11]. In general terms, the calculation depends on the shape of the electrode and conductivity of the electrolyte.

So, the model for the electrode-electrolyte interface is given in Figure 3.

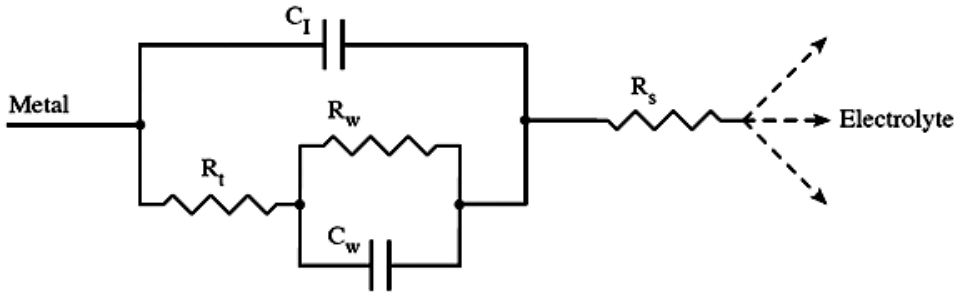

Figure 3. Electrical model of metal-electrode interface [11]

Planar microelectrode arrays have been used extensively by many scientists for all kinds of neural recording experiments. In [8], Pine et al used microelectrode arrays to record signals from rat neurons. In [9], gold conductor electrodes were used to record signals from mammalian spinal cord neurons. In [12], a method for manufacturing gold based platinized microelectrodes has been presented. In [13] an electrode array was embedded with a Petri dish, which helped to make long time chronic recordings. The planar electrode arrays were not exclusive to *in vitro* recordings. It was also used to make *in vivo* recordings. In [14], a 3-dimensional recording array was manufactured. Sharp extracellular penetrating electrodes, each of which has a number of thin film microelectrode on them, were placed on a grid formation to obtain a 3D recording of the subject's brain activity. A similar approach were used in [15].

2.2.4 Neuron Transistor

The ability to couple neurons to transistors was first demonstrated by a German group supervised by Fromherz [16]. Several aspects of this concept have been investigated and will be discussed here.

The most important aspect is the use of gate-metal-free MOS transistors as recording devices. The neurons are placed on top of the thin oxide of a MOSFET as shown in Figure 4, which depicts a first-generation neuron transistor implementation. The neuron is stimulated using the patch-clamp technique via a pipette as shown in the top left section of the figure. The voltage changes on the neuron's membrane modulate the transistor, resulting in a changing current. The silica surface of the metal-free gate provides an inert interface for the neuron and the underlying medium.

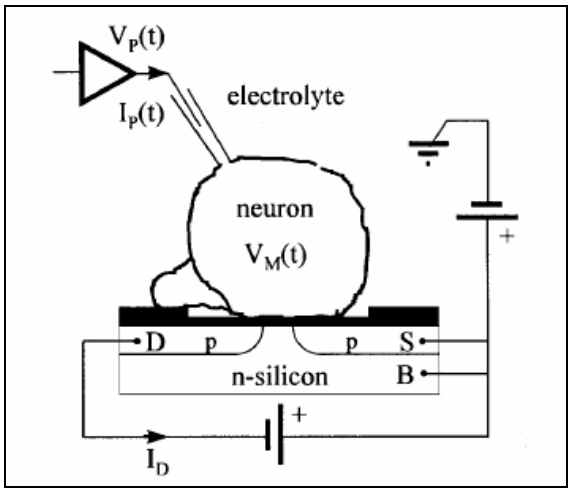

Figure 4. Neuron Transistor [11]

The MOSFET is biased with $V_{sd} > |V_{gs}-V_{th}|$ so that it is in the saturation region. $V_s=V_b=VDD$, and $VDD>>V_{sd}$. This means this circuit will have a current flow even when there is no activity on the neuron's membrane.

This system has been modeled based on Hodgkin-Huxley equations and basic membrane-oxide coupling equations; the resulting circuit model is shown in Figure 5.

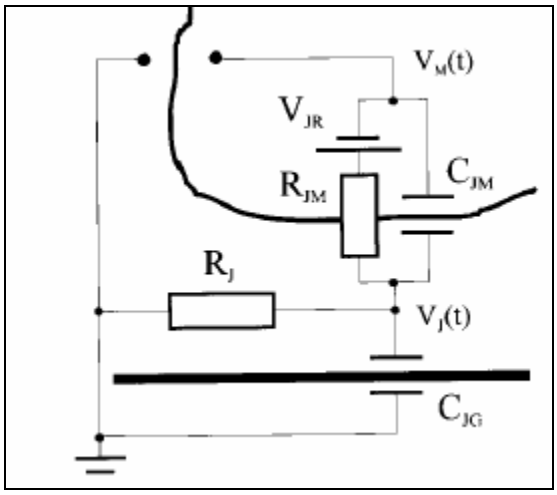

Figure 5. Circuit model.

In this model, R_j is the sealing resistance, C_{jm} is the membrane capacitance, C_{jg} is the oxide capacitance, $V_m(t)$ is the inner membrane potential, and $V_j(t)$ is the outer membrane potential. V_{jr}, R_{jm} and C_{jm} are defined by the Hodgkin and Huxley equations.

Second-generation implementations of the neuron transistor differ from first-generation implementations in that they introduce a "stimulation spot" [19] which makes the system completely non-invasive. The stimulation spot is p-doped silicon covered with a thin layer of SiO_2. Figure 6 depicts this configuration.

Voltage pulses are used to elicit an action potential on the neuron which can be recorded by the neuron transistor the same way it was done in first-generation implementations.

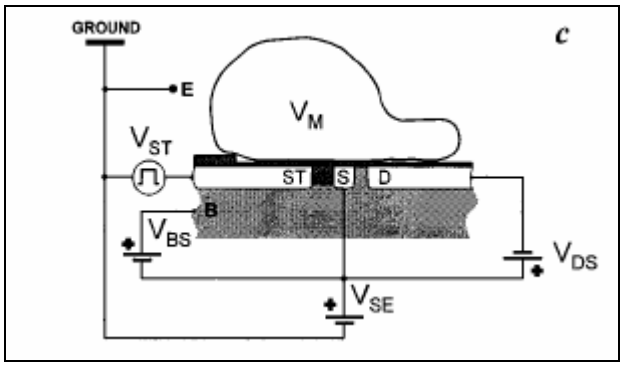

Figure 6. 2nd generation neuron transistor

incubation in an appropriate medium and growth factors. In [20], Jenkner chose the pedal ganglia of *Lymnaea Stagnalis* for their neural cells and conditioned the medium with brain tissue of the same species of snail. The brain tissue created an environment that helped neuron outgrowth.

Next, he put multiple neurons on top of neuron transistors. Some of these neurons formed synaptic connections as seen in Figure 7. The system was used to stimulate a neuron, which generated an action potential. Then this activity propagated to the synaptically connected second neuron, which also elicited an action potential. This activity was recorded by the neuron transistor. This was a demonstration of *chip* → *cell* → *cell* → *chip* communication. This shows that two-way communication can also be achieved by recording a cell's activity after it is stimulated. This hybrid neuro-electronic unit practically implemented all of the networks shown in Figure 8.

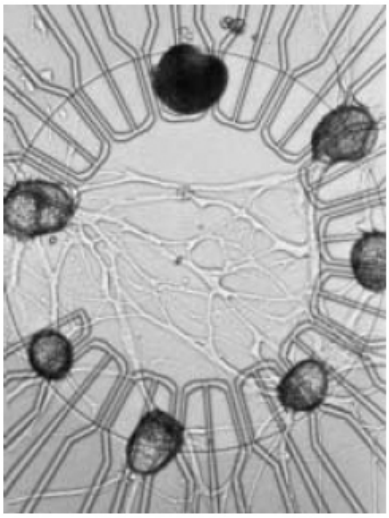

Figure 7. Synaptically connected neurons

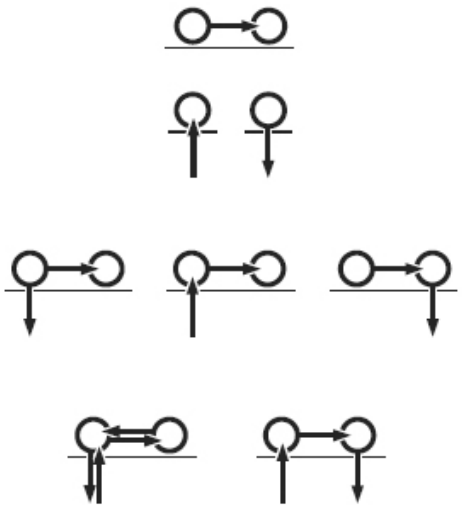

Figure 8. Neural network

One of the problems with these systems is that neuron cell bodies may not stay at the locations at which they are initially placed. One possible reason for this is that the medium may exert forces on the neuron cell bodies that cause them to move about. The most common method that is used to avoid this problem is to coat the chips with adhesion factors. Poly-l-lysine is one of the most used materials for cell adhesion. But, even after using poly-l-lysine neurons will sometimes still move around. Fromherz et. al, found a good trick to overcome this problem [20] they used so-called "picket fences" made out of polyimide to immobilize the somata of *L. Stagnalis* neurons. These obstacles, as shown in Figure 9, were an effective way to keep the neurons on the recording site.

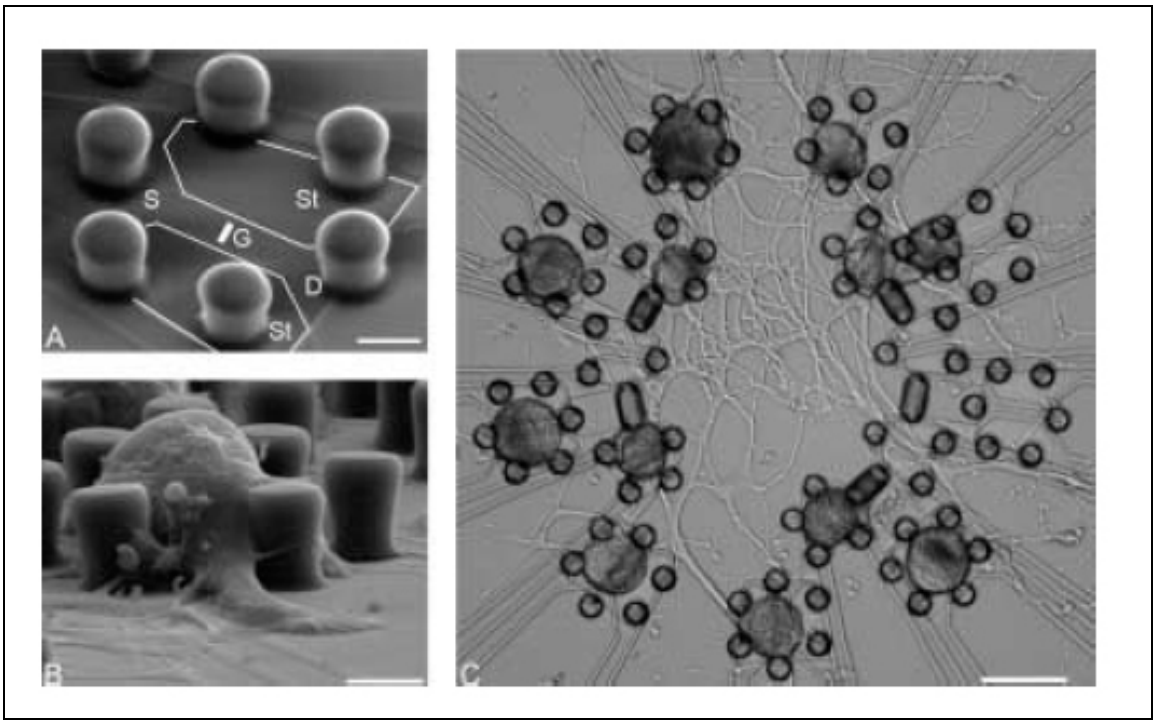

Figure 9. Picket fences [20]

Fromherz et. al. also advanced the research in the area of neuron transistors in several other ways. In earlier work, the electronics were separated from the recording unit. In 2002 Bonifazi et. al. designed a system where the electronics were adjacent to the recording unit. They designed two chips, one with the neuron-transistors and another chip with a preamplifier and some detection circuitry [21] These two chips were bonded in the same package and inter-chip connections were made directly. This system is shown in Figure 11.

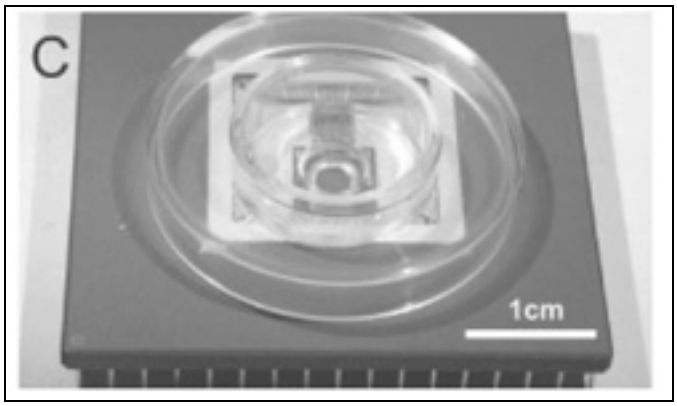

Figure 10. Two chip solution [21]

2.3 Low frequency noise sources

The neural signals usually have a bandwidth between several hertz to around 5 kHz. In this frequency range, some problems that normally would not make too much difference in high frequency circuits start to become very important. In this section, these noise sources will be identified, some of the methods of low frequency noise reduction techniques will be presented and some implementation issues will be addressed.

2.4 Flicker Noise and Thermal Noise

Flicker noise is a significant noise source for low-frequency applications. It originates in the amplifier. The most significant contributors of this type of noise are the input transistors, because the noise generated by them will be directly added to the signal and amplified by the following stages.

Although there has been extensive research about this topic, it is not entirely known how flicker noise is generated. There are two main theories about the origins of flicker noise. The first theory finds the "random fluctuations in the number of carriers near the Si-SiO2 interface" as a cause of this noise [22]. The second theory accredits mobility fluctuations as a

cause of flicker noise [22]. In general, the following equation is used to quantify flicker noise.

$$v^2{}_n(f) = \frac{K}{c_{ox}} \frac{1}{WL} \frac{1}{f^c} \tag{2}$$

The exponent c is usually between 0.7 and 1.2. K is a process-dependent constant and it has been shown to be around $2x10^{-25}$. In this equation f is the frequency, c_{ox} is the oxide capacitance per unit, W is the channel width of the transistor and L is the channel length of the transistor. The exact values of K and c are not known until after testing the device. In most cases, c is considered to be 1, which makes the noise proportional to *1/f*. For this reason, flicker noise is also called "*1/f* noise". The implication of (2) is that flicker noise is dominant at low frequencies and asymptotically approaches infinity as the frequency approaches zero. This means that when we are looking at a signal at very low frequencies and if we observe the signal long enough, the noise ***may*** take on very high values. But practical experiments show that *1/f* noise does not actually approach infinity [23].

Thermal noise is caused by random fluctuations in the energy of the conducting electrons in any resistive element, including transistors. It is formulated as the following.

$$V_n = \sqrt{4kTR} \tag{3}$$

Where k is Boltzmann's constant, T is the temperature and R is the resistance of the resistive element.

At low frequencies flicker noise dominates, and at higher frequencies thermal noise dominates. Thermal noise has a uniform distribution and both thermal and flicker noises can be added together as seen in Figure 11. The frequency at which these two waveforms intersect is called the *1/f noise corner*.

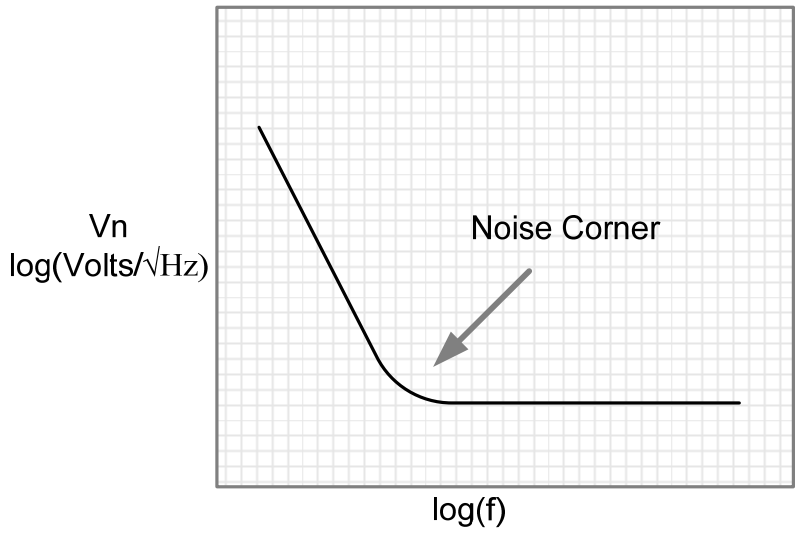

Figure 11. Noise spectrum

2.4.1 DC Offset

Ideally, the differential outputs of an amplifier should be zero when its differential inputs is also zero, but generally there is an offset voltage between the outputs of the amplifier. This DC offset may be a result of the improper design of the circuit but usually it is caused by mismatches in the circuit. The DC offset seen at the output of an amplifier will decrease the dynamic range of the circuit. This offset voltage can usually be compensated by introducing an offset at the input. This offset is referred to as the amplifier's *input offset voltage*. Figure 12 shows this voltage.

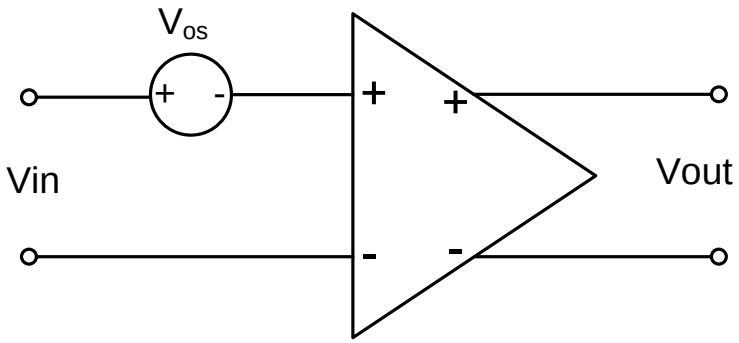

Figure 12: DC Offset

2.4.2 Other noise sources

There are some other noise sources that are specific to the materials chosen and manufacturing processes. In the case of metal electrodes, the resistive elements between metal-electrolyte interfaces create additional thermal noise which will degrade system quality. This noise, especially that created by the spreading resistance *(Rs)*, limits the size and the shape of the electrode, adding another constraint to the recording system design [24] [25]. Another noise source is the *random baseline drift,* which is reported to be very slow [26]. and therefore relevant. This drift is usually around 100mV at a frequency of less than a couple of hertz [26]. Designers usually remove this noise with a high-pass filter which has a low cutoff frequency. It is reported that this noise only applies to metal electrodes [24] and doesn't appear on neuron-transistor based systems.

Another noise source that limits the system's performance is EMI or Electro-Magnetic Interference. Any wire that passes a current can be a source of EMI. One of the problematic manifestations of EMI is the 60 Hz noise that is caused by electric lines. Many designers add a notch filter to attenuate this type of noise.

Crosstalk between adjacent lines that connect to recording sites can cause problems. If a large signal is passed through one of these wires, artifacts may appear on the other line. This

is often a problem when one of the lines connects to a stimulation spot while the other carries a recording signal.

2.5 Noise Cancellation Techniques

2.5.1 Chopper Modulation

The chopper technique is used to reduce the effects of flicker noise and DC offset in amplification systems. This method does not decrease either types of noise; it simply isolates the noise from the signal in the frequency domain so that the noise can be easily removed without affecting the signal.

In this technique, as seen in Figure 13, the input signal is converted to higher frequencies, specifically the odd harmonics of the chopper frequency, where the flicker noise has an insignificant value. The converted signal is amplified and afterwards a second chopper modulator brings the signal back to its original band. The result is that the amplified signal does not contain a significant flicker noise component.

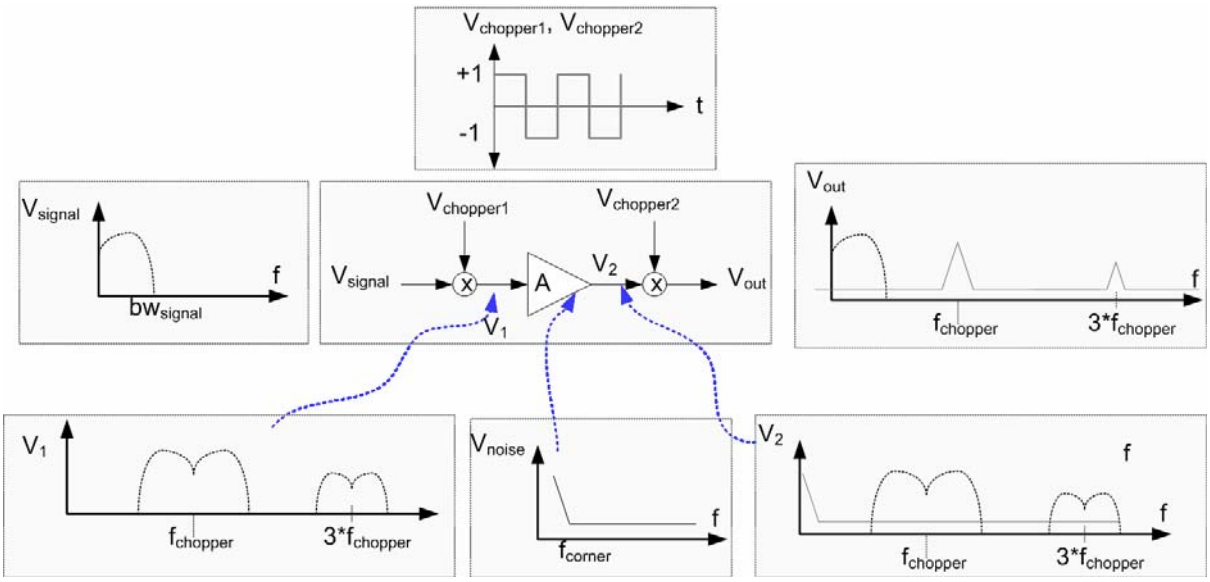

Figure 13: Chopper modulation

If the amplifier has an infinite bandwidth, the amplified signal can be recovered in its full strength since demodulation, which in this case is exactly the same as modulation, will collect the signal from all of the harmonics it is converted to. However, all amplifiers have a limited bandwidth so complete recovery is not possible [21]. As an example, if a signal with an amplitude of V_0 is used with an amplifier which has bandwidth of $2*f_{chop}$, where f_{chop} is the chopper frequency, and a gain of G, the recovered signal's amplitude would be $0.8*G*V_0$ [27]. The chopper frequency, amplifier bandwidth or signal bandwidth can be chosen as seen in (4), provided that they can be changed by the designer. This equation assumes that the signal bandwidth is BW_{signal} , amplifier bandwidth is BW_{amp} and the chopper modulator is a square wave signal with a frequency f_{chop}. The noise corner frequency is f_{corner}..

$$f_{corner} + BW_{signal} < f_{chop} < BW_{amp} - BW_{signal} \tag{4}$$

This equation implies that the smallest value of f_{chop} should at least be able to separate the flicker noise from the signal, and the highest value should not push the signals main harmonic out of the amplifier's passband.

2.5.2 Auto-zeroing

Consider the definition of the DC offset, which was given in the previous pages. Auto-zeroing is essentially subtracting the unwanted offset voltage from the signal, therefore getting an offset-free output. Auto-zeroing consists of two periods: a "sampling phase" and an "offset-free signal" phase. In the sampling phase the offset is sampled and stored and in the offset-free signal phase this stored quantity is subtracted from the signal, which results in a noise-free output [27]. The basic operation is shown in Figure 14.

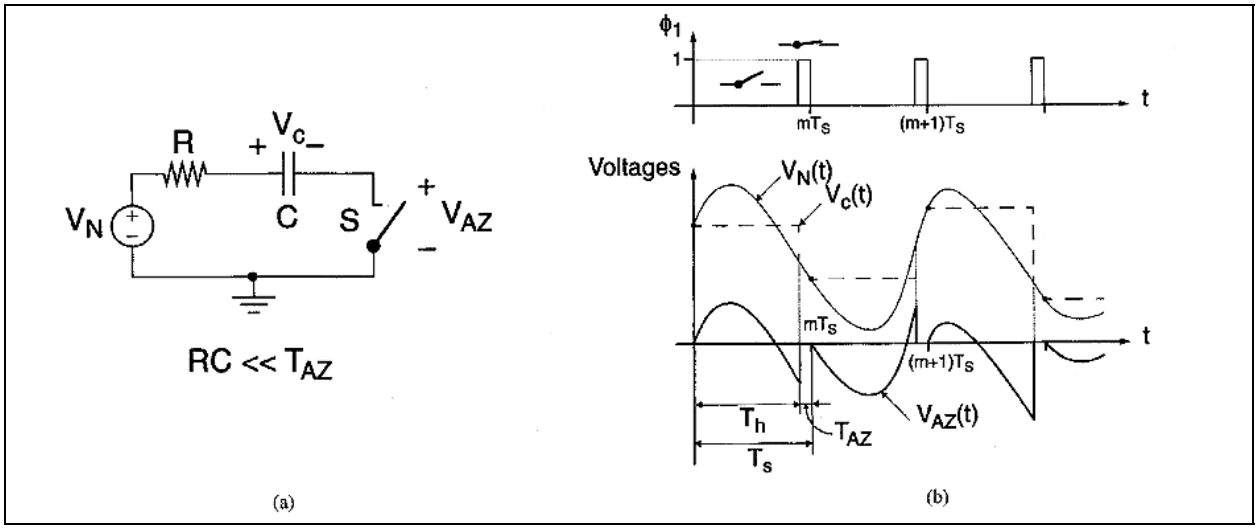

Figure 14: Auto-zeroing [27].

The input signal to an amplifier is assumed to be changing over time *faster* than the very low frequency signals. So, the capacitor shown in the figure will store the slowly changing signal during the sampling phase, and subtract it from the input signal during the offset-free signal phase.

Auto-zeroing is a sampling technique. One of the drawbacks of this technique is that white noise will be aliased to the baseband, thereby increasing the noise floor of the system.

2.6 Implementation Problems and Solutions

2.6.1 Clock Feedthrough and Channel Charge Injection

Every time a MOS switch is turned off, some fraction of the charge that is stored in its channel is injected into the line. These unwanted current spikes will be amplified and low pass filtered by the amplifier and low pass filter, if there is one. This results in a DC offset at the amplifier's output, which is called *residual offset*. Here an important trade-off comes into effect. If the main amplifier's bandwidth is much larger than the chopper frequency, it will result in an increase in the gain as mentioned in previous chapters. However, this will also cause the residual offset voltage to increase because more spectral components of the spikes will be added to the signal and amplified. When choosing amplifier's bandwidth, this trade-off must be taken into account.

One of the important properties of these spikes is that they have relatively low time constant compared to the period of the chopper clock. Therefore much of the energy of the spikes is located at higher frequencies [27]. That being the case, in [27]; the residual offset voltage is quantified in (1) in which τ is the time constant of the spike and V_{spike} is the amplitude of the spike.

$$V_{os} = \frac{2\tau}{T} \times V_{spike} \tag{5}$$

The previous equation assumes that the amplifier has infinite bandwidth. By making the amplifier's bandwidth equal to twice the chopper frequency, the residual offset will reduce to

$$V_{os} = \left(\frac{2\tau}{T}\right)^2 \times V_{spike} \tag{6}$$

So, even without applying any techniques, the residual offset can be reduced to a very low level. The residual offset can be further reduced using some layout techniques [21], as well as some circuit techniques. One way to reduce this injected noise is to use half-sized dummy transistors as seen in Figure 15. The built up charge on the switch will equally split between source and drain and be compensated by these dummy switches. However, this requires that either the input capacitance (Cp) is equal to output capacitance (Ch), or the chopper clock's transition time is very short [27].

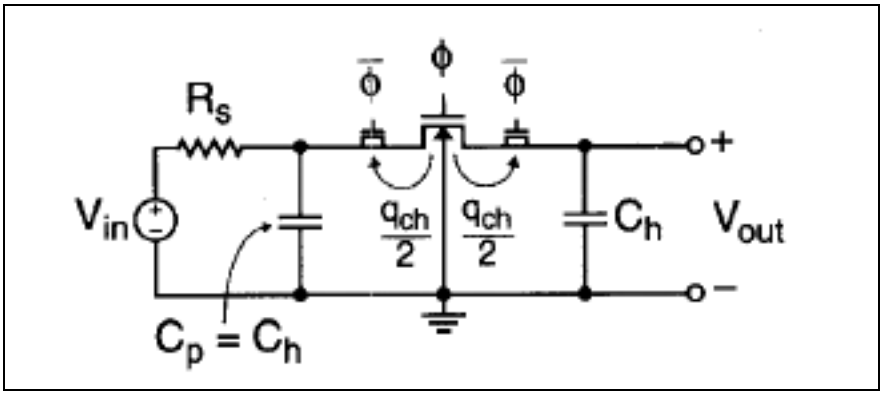

Figure 15: Using dummy switches [27]

Another way of reducing this noise is making the input capacitance much larger than the output capacitance, so that most of the charge is directed to the input capacitance. Furthermore, using a differential configuration will also help to reduce this offset [27].

In chopper modulation, the residual offset is directly added to the signal because the chopper demodulator will bring this offset back to the baseband. One of the ways to prevent this noise

from being added to the signal is to use a small delay between the modulator's and demodulator's chopper signal, as seen in Figure 16 [28].

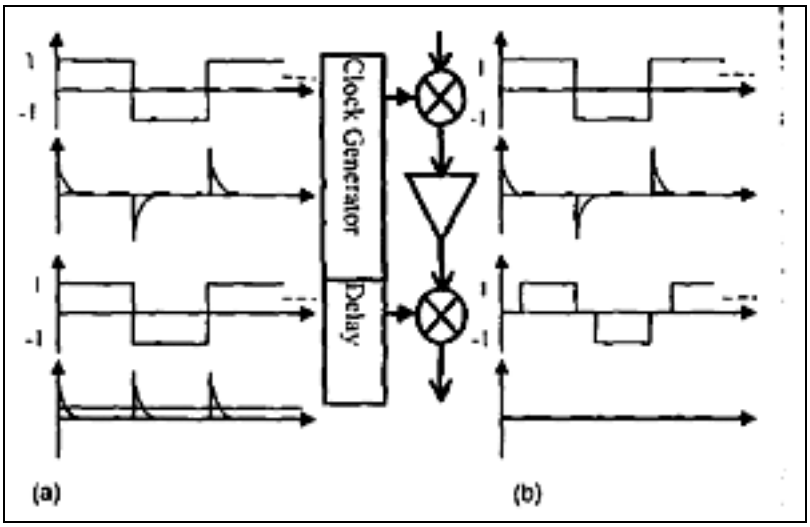

Figure 16: (a) Regular chopper (b) With delayed output modulator [28]

This gap, compared to the chopper period, will be very small thus it will not effect the circuit's operation. During this time, the charge, which would normally cause a residual offset, will decay and a clean signal is passed to the following stages.

Another way of dealing with this problem is proposed in [29]. This idea is depicted in Figure 17. In this technique, another chopper pair, operating at much lower frequencies than the first chopper pair, is included in the circuit. The spikes, which were originally caused by the first chopper modulator, will be inverted by the second chopper modulator, resulting in zero offset. The outer pair will still introduce an offset, but since they operate at much lower frequencies, it will be much lower than that of the version without the second pair. Using this technique, 100 nV offset has been achieved by the authors.

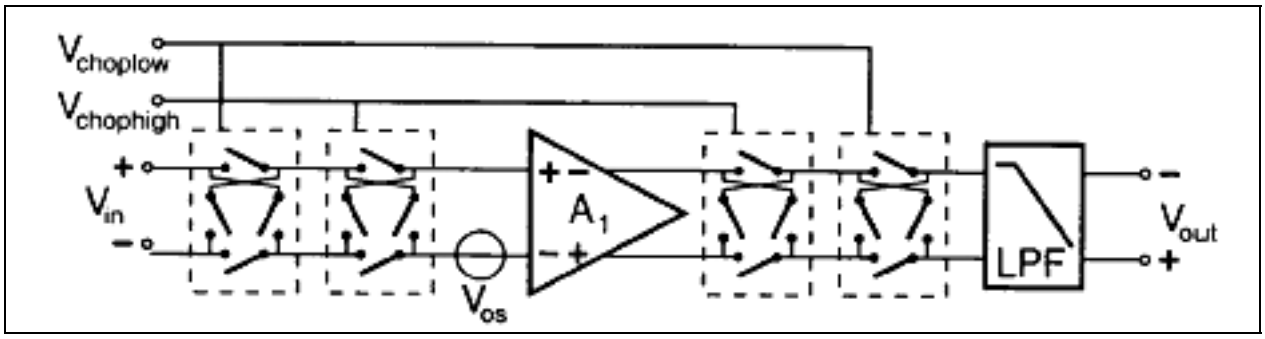

Figure 17: Nested-chopper modulation [29]

2.7 Conclusions

In this literature review, we presented some of the methods that are used to interface electronics with living organisms, specifically cultured cells. We presented the patch clamp technique, metal electrodes and neuron transistors and explained some of the aspects of each technique. We also presented noise sources that will interfere with the neural signals, and some possible solutions and ways to avoid further problems.

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Chapter III. A chopper modulated neural recording system

3.1 Introduction

In this chapter we present practical implementations of some neural recording systems. These systems are designed to stimulate and monitor the electrical activity of a large population of cultured neurons using an array of recording sites within a shared substrate.

First, the design of a multi-channel chopper modulated amplifier is presented. The details of chopper modulation were explained in Chapter II. The compact amplifier cells use the well-known chopper technique [1] [2] instead of large amplifier input devices and high pass filters to reduce problems associated with flicker noise and DC offset. A local voltage reference is used to eliminate DC drift of the recorded signals via differential path amplification. Compact analog switches are used to multiplex the recording signal before amplification to minimize area and power. The amplifier chip is designed to use external neural signals as its inputs, or to use an internal electrode array for interfacing with neurons. The internal array is designed to have probe pads for interfacing with neurons.

Three different approaches were attempted. The first was to use open-gate, metal-free, insulated-gate field-effect transistors [3] for direct coupling of neuron to silicon without the interfering metal interface exhibited in microelectrode arrays [4]. This device was manufactured by the local processing facility at NC State University. The second approach was to use commercial micro-electrode arrays as the recording sources. In this case, commercially available recording devices were interfaced to the amplifier. The third approach was to use extracellular recording electrodes as used in tissue recording as the recording source.

3.2 Specifications

The target in this design is to be able to record neural signals using either planar electrodes, neuron-transistors or impaled microelectrodes. The voltage levels for the neural signals can be as low as 500 μV [5] and the bandwidth is usually not more than 10 kHz [5].

One of the problems with working with low frequency signals is that low frequency noise can interfere with the neural signals. The flicker noise and the DC offset of the amplifier itself can be problematic since their effects increase with the decrease of the frequency. Our system uses the *chopper modulation* technique to reduce the effects of this type of noise.

The output impedance of the recording device is a significant factor in determining the specifications. In the case of using planar or impaled electrodes, the output impedance is higher than 2.2 kΩ . Thus our amplifier should have a high input impedance to transfer the most of the signal. This is usually not hard to achieve because at low frequencies the input impedance of a CMOS-based amplifier is generally high.

The gain of this system is also very important. The signals must be amplified to a reasonable level for the detection of the neural signals. The neural signals can be as low as 500 μV, but they can get higher for situations when there is a very high sealing resistance. Assuming that the maximum amplitude is not higher than 2 mV, a gain between 500 and 1000 seems reasonable. We selected a gain of 650 (56 dB) for this project. Also, to achieve optimum noise performance, we designed the system to be fully differential.

The bandwidth of the system is also an important issue for our application. Neural signals generally have a bandwidth of at most 10 kHz, but chopper modulation requires additional bandwidth to work properly. The internal system, which consists of the amplifier and the chopper modulator/demodulator, has a bandwidth of 130 kHz .

To avoid aliasing in the analog-to-digital conversion process, the signal bandwidth has to be reduced to a low level. To achieve this, we added a 2^{nd} order low-pass filter with a cutoff frequency of 5kHz ~10 kHz. The output signal can also be further filtered by additional filters, if needed.

3.3 Architecture

The top-level architecture of the chopper modulated amplifier is shown in Figure 1. The front-end system consists of an analog multiplexer, a chopper modulator, a cascode amplifier, a chopper demodulator and a low-pass filter. The inputs to the system are 4-to-1 multiplexed using an analog multiplexer. There is also a *reference* input, which is connected to the reference node of the recording environment.

One of the 4 inputs to the system is selected using the analog multiplexer, then it passes through a fully differential chopper modulator, which up-converts the signal to the chopper frequency. The signal is then amplified and demodulated back to the baseband by the output chopper demodulator. A final low-pass filter stage removes the remaining out-of-band noise for subsequent analog-to-digital conversion and signal processing.

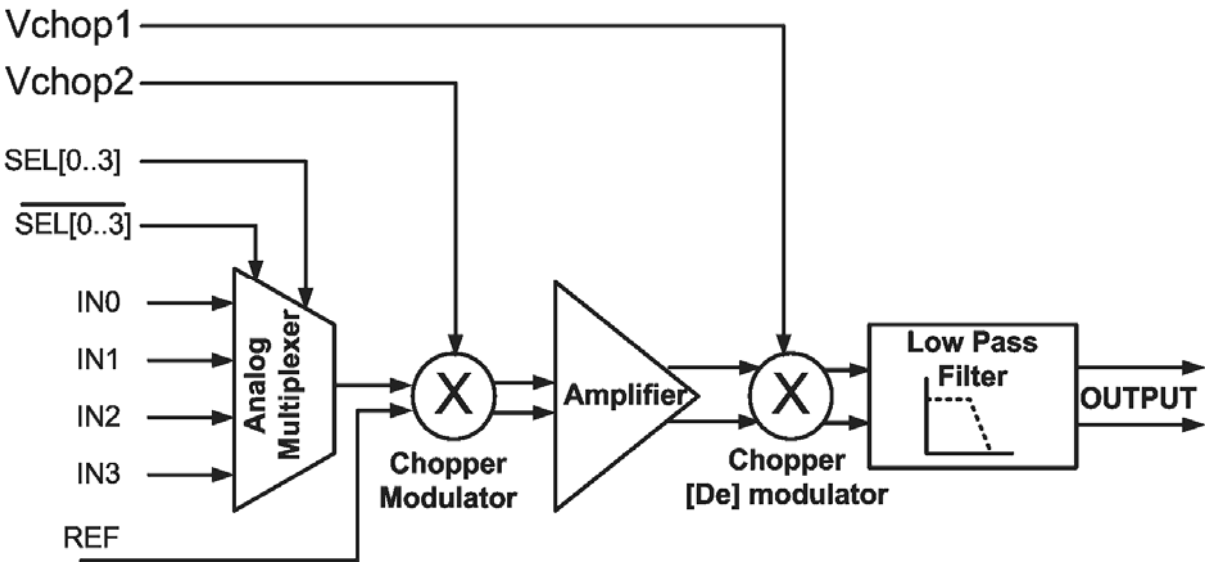

Figure 1. Toplevel

3.3.1 Analog Multiplexer

The analog multiplexer allows the use of a single amplifier to service multiple recording sites. The circuit details of the 4-channel analog multiplexer are shown in Figure 2. The input and select signals are labeled IN0-IN3 and S0-S3, respectively. The select signals go off-chip allowing user control. The multiplexers are simply NMOS transmission gates that pass the signal when their gates are turned on and become high-impedance when their gates are turned off.

Charge injection cancellation is achieved by inserting dummy switches, which are driven by complementary select signals [1]. The dummy switches are also inserted between the recording sites and main switches to isolate the effect of charge feed-through from the neural signal.

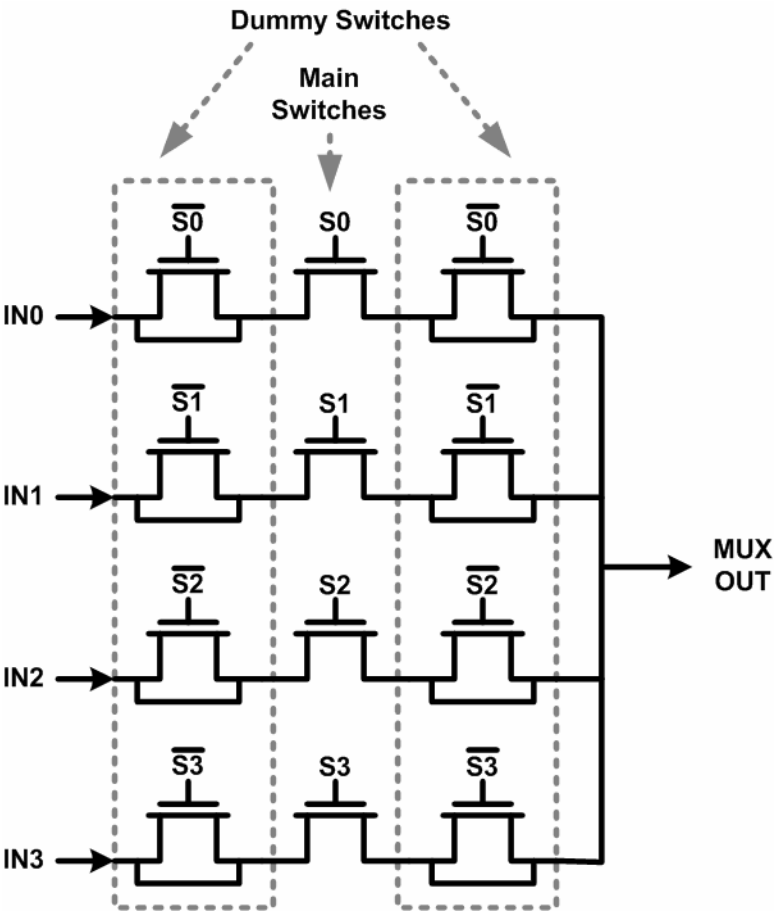

Figure 2. 4-channel analog multiplexer

3.3.2 Chopper Modulator and Demodulator

The purpose of the modulator is to multiply the input with the waveform seen in Figure 3.

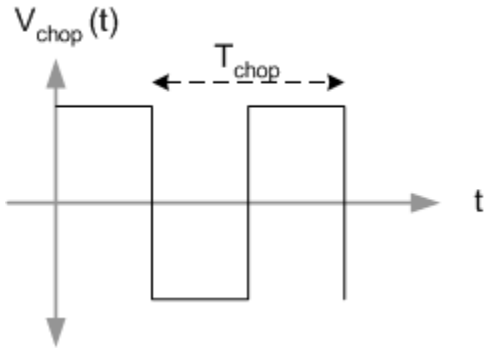

Figure 3. Chopper Signal

The simplest way to do this is using the circuitry is shown in Figure 4 [1]. The modulator inverts the signal when CLOCK is low and does not invert the signal when CLOCK is high. The demodulator is identical. However, the modulator and demodulator can be independently controlled which makes it possible to adjust for phase delay problems [1].

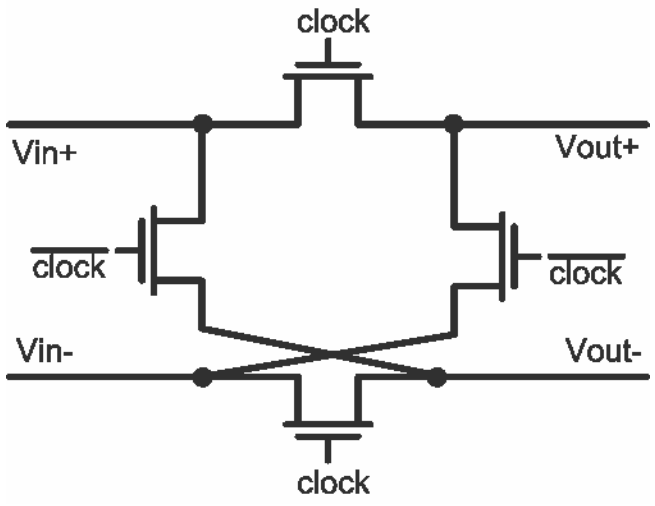

Figure 4. Chopper modulator/demodulator

3.3.3 Bias Circuitry

The purpose of the bias circuitry is to provide bias signals to the amplifiers in the chip. The bias circuitry is shown in Figure 5.

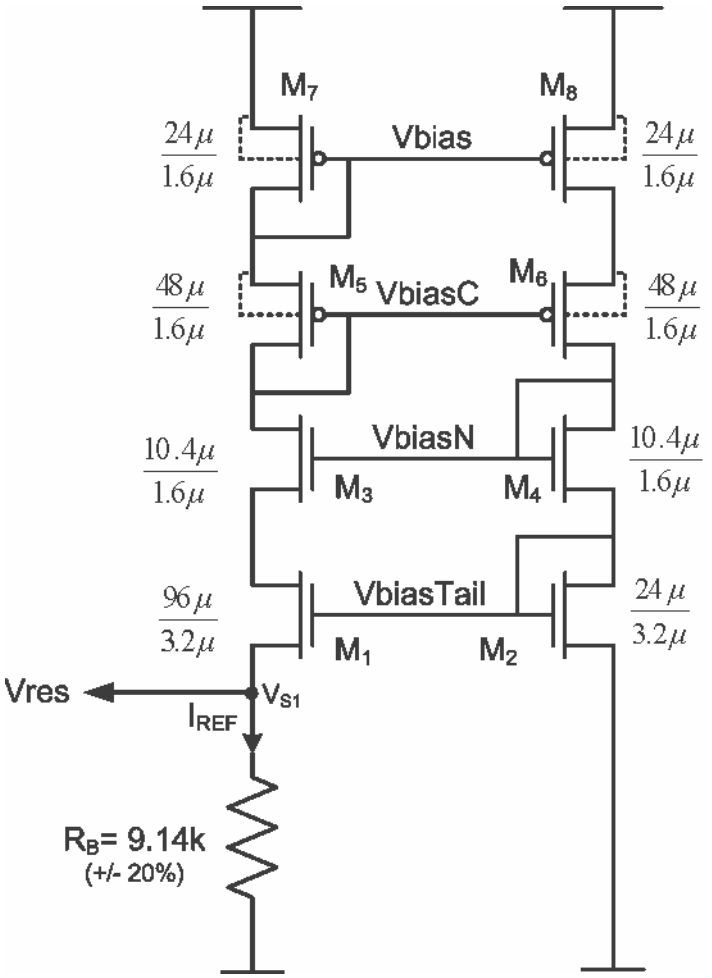

Figure 5. Bias Circuitry

This circuit is a modified version of a common biasing approach used in operational amplifier design [6]. In Figure 5, we can assume $I_{D1} = I_{D2}$, so we can write the following:

$$V_{GS_2} = V_{GS_1} + I_{ref} \times R_B \tag{7}$$

Assuming that threshold voltage is equal for both M1 and M2, we can write …

$$V_{eff_2} = V_{eff_1} + I_{ref} \times R_B \tag{8}$$

… which can also be written as:

$$\sqrt{\frac{2I_{D2}}{\mu_n c_{ox}(W/L)_2}} = \sqrt{\frac{2I_{D1}}{\mu_n c_{ox}(W/L)_1}} + I_{D2}R_B \tag{9}$$

Since $I_{D1} = I_{D2}$, we can write …

$$\sqrt{\frac{2I_{D1}}{\mu_n c_{ox}(W/L)_1}} = \sqrt{\frac{2I_{D1}}{\mu_n c_{ox}(W/L)_2}} + I_{D1}R_B \tag{10}$$

… which leads to:

$$\frac{2}{\sqrt{2\mu_n c_{ox}(W/L)_1 I_{D1}}}\left[1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right] = R_B \tag{11}$$

Remembering that

$$g_m = \sqrt{2\mu_n c_{ox}(W/L)I_D} \tag{12}$$

we can write

$$g_{m1} = \frac{2\left[1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right]}{R_B} \tag{13}$$

This means that the g_m values of the transistors will be determined by geometric ratios of the transistors and R_b. In this design, we selected $(W/L)_1=4(W/L)_2$, which results in:

$$g_{m1} = \frac{1}{R_B} \tag{14}$$

One of the advantages of this circuit is that the bias voltages can be adjusted even after the design using an external resistor. One of the resistor's terminals, which is labeled as *Vres*, is connected to a pad to externally set the resistor value.

3.3.4 Cascode Amplifier

The amplifier used in this system is a fully-differential cascode amplifier which can be seen in Figure 6. A cascode amplifier topology is used because it achieves the highest gain with a single stage. The area of the input transistors can be reduced because their flicker noise contribution will be reduced by the chopper technique.

The principal factors that effected the amplifier type selection were:

Input Dynamic Range: The inputs to the amplifier may range between microvolts to 1 mV. Therefore, a gain somewhere in the range of 500-1000 was required.

Noise: Although our chopper implementation helped with the flicker noise, it offered no reduction in thermal noise. We needed to have a reasonably small amount of noise compared to the signal measured.

Area: The area available is fairly small in a cultured tissue and cell recording environment. Although multiplexing the input signals does reduce the area, it may still not be enough for recording via massive arrays.

The cascode amplifier is the best choice for the following reasons:

- It provides a large gain in a single stage.
- Area is reduced because there is no need for a second stage.

The cascode amplifier has an important drawback, which is the dynamic range of the output is somewhat limited due to the stacking of the transistors.

This amplifier exhibits a gain of 56 dB with a 115 kHz bandwidth. This configuration results in more than 80 dB CMRR.

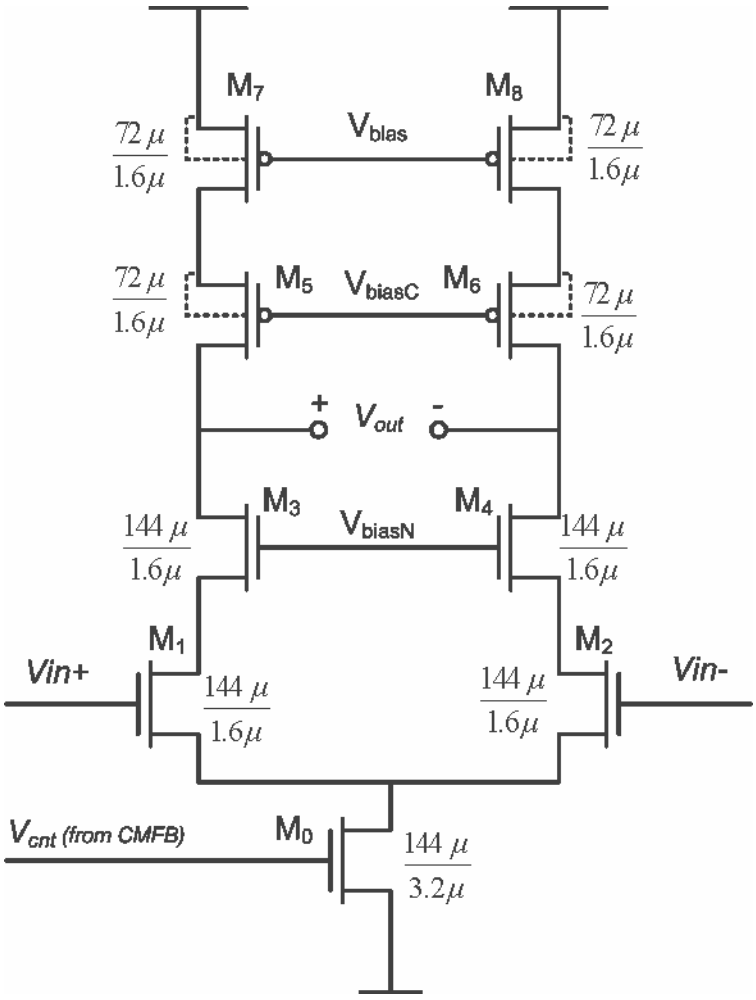

Figure 6. Cascode amplifier

3.3.5 Common-Mode Feedback Circuit

The common mode feedback circuit (CMFB) is used to suppress any variations in the quiescent point of the output voltage. The block diagram of the CMFB circuit is shown in Figure 7.

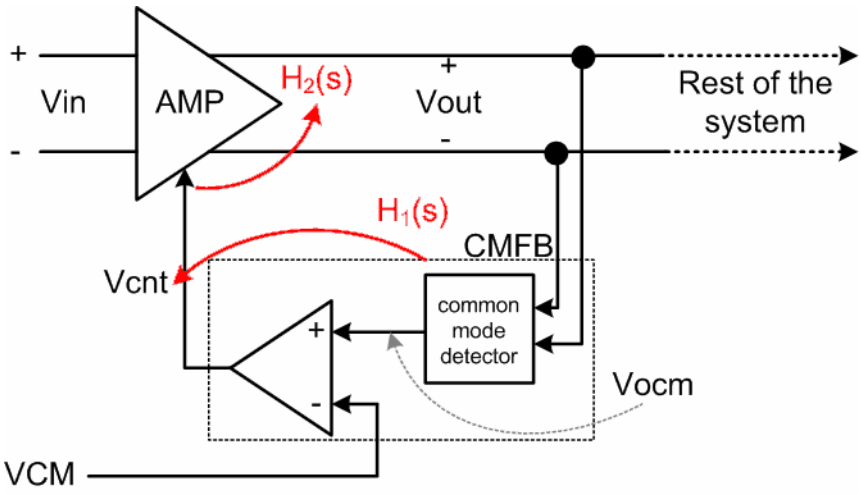

Figure 7. CMFB Block Diagram

The output common mode of the circuit can be is given as

$$Vout,cm = \frac{Vout(+) + Vout(-)}{2} = Vocm \tag{15}$$

The CMFB circuit forces the common mode voltage to be equal to *VCM*. The feedback equation can be written as follows:

$$\frac{Vocm}{Vcnt} = \frac{H_2(s)}{1 + H_1(s)H_2(s)} \tag{16}$$

Figure 8 shows the circuitry we used to implement the CMFB system.

The circuit operates like this: as the common mode voltage at the amplifier output rises, drain current at M_3 and M_4 increases. The sum of these currents is equal to the drain current of M_1. This current mirrors to M_2 . As the drain current, I_d, of M_2 increases, V_{cnt} increases.

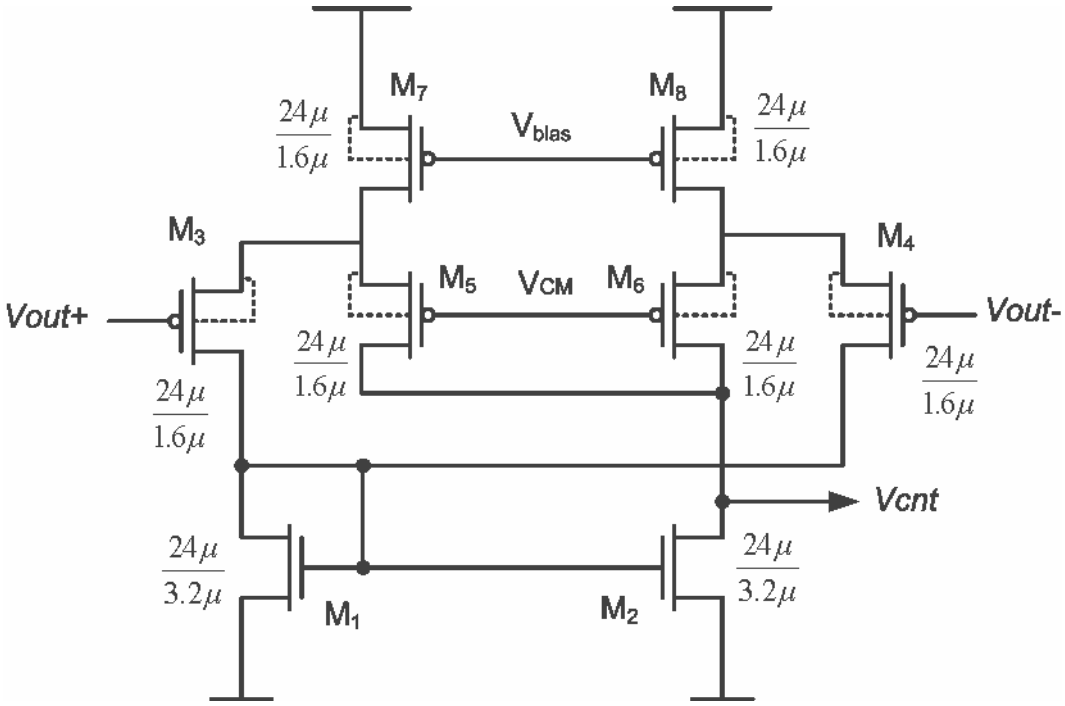

Figure 8. Common Mode Feedback circuit

Stability Analysis

For stability analysis, we turn to the Figure 9 which is a depiction of a block diagram of the amplifier-CMFB loop.

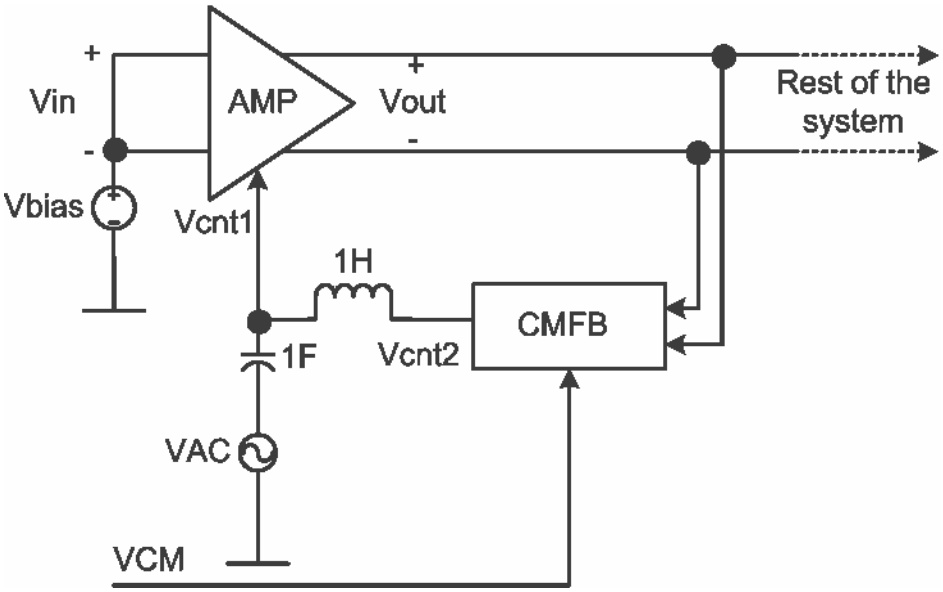

Figure 9. Stability analysis of the CMFB loop

Assuming:

$$V_{cm} = \frac{V_{o+} + V_{o-}}{2} \tag{17}$$

The transfer function of the CMFB circuit is given as:

$$H_1(s) = \frac{V_{cnt}}{V_{cm}}(s) \tag{18}$$

And the loop completes with the second stage:

$$H_2(s) = \frac{V_{cm}}{V_{cnt}}(s) \tag{19}$$

In order to determine the stability of the system following method was used. The system was modified as shown in Figure 9. An AC sweep was conducted using the Spectre simulator. The loop gain and phase margin (PM) can be found using

$$\frac{V_{cnt2}(s)}{V_{cnt1}(s)} = H_1(s)H_2(s) \tag{20}$$

The simulation results showed that the PM of the system is 40 degrees and the gain is 120 (41 dB).

3.3.6 Offset Correction Circuit

This system is also provided with a manual offset-cancellation circuit in case the chopper technique does not completely eliminate the offset. The block diagram of the offset-cancellation circuit and its connection to the amplifier is shown in Figure 10.

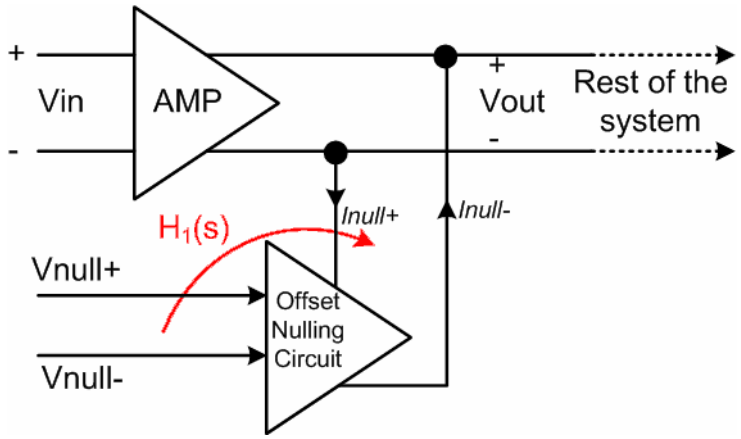

Figure 10. Offset-cancellation circuit block diagram

This block introduces a current mismatch at the output of the amplifier, which in turn creates a voltage offset at the output of the system, which allows any offset to be nullified.

The output offset can be reduced by the gain of the nulling circuit, which is found to be equal to 24 at low frequencies. So,

$$V_{offset(nulling)} = \frac{V_{offset(no-nulling)}}{24} \tag{21}$$

This device can be turned off by connecting its inputs to ground.

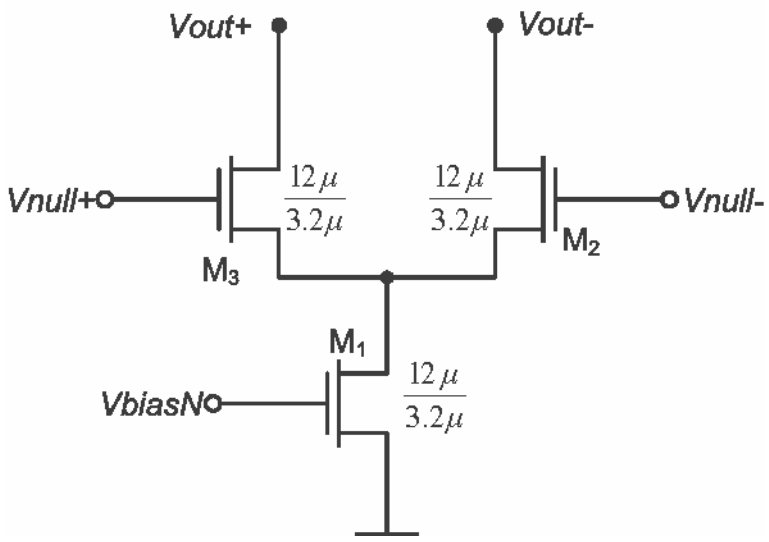

Figure 11. Offset correction circuit

3.3.7 Low pass filter

The chopper demodulator's output will have the neural signal at the baseband and modulated flicker noise at higher frequencies. After that, a data-acquisition unit may be used to capture and analyze the signal. The modulated noise can be removed later with software. This

approach requires the sampling rate of the analog-to-digital converter to be at least twice the bandwidth of the previous stages. In order to reduce the required bandwidth, an analog low-pass filter is added to remove the noise beyond the desired signal range. This reduces the sampling rate requirement to a very low value. We chose a second order GM-C filter to filter out the noise.

The design of this filter involves several steps. The transfer function of a generalized 2nd order filter is given in (22) [6].

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + (\frac{\omega_0}{Q})s + \omega^2{}_0} \tag{22}$$

The block diagram of this function can be seen in Figure12.

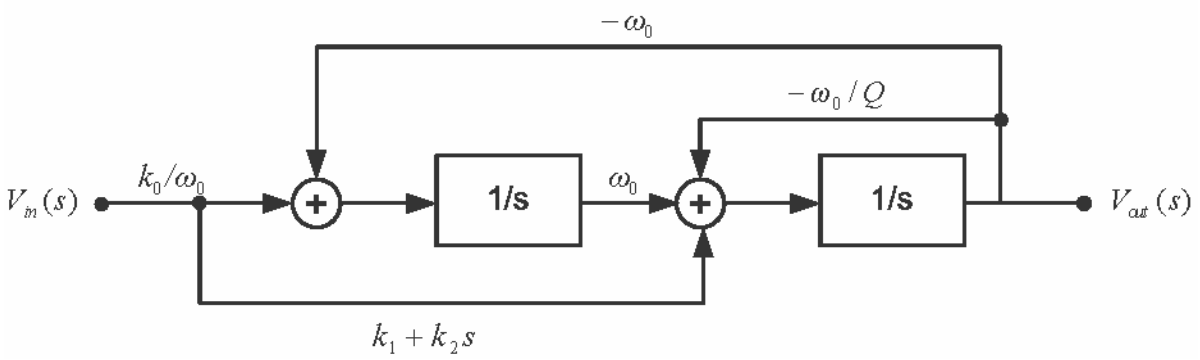

Figure 12. 2nd degree filter block diagram

For a low pass filter, the values of k_2 and k_1 will be zero. Using transconductance cells, a low-pass circuit can be designed as seen in Figure 13. Equation (17) shows the transfer function.

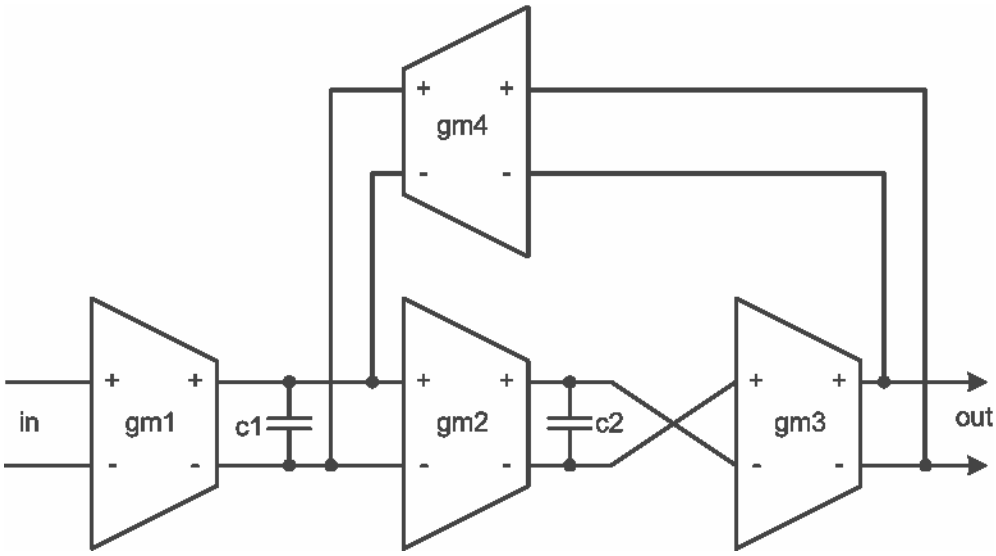

Figure 13. Low Pass Filter

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s\frac{G_{m3}}{C_2} + \frac{G_{m2}G_{m4}}{C_1C_2}} \tag{23}$$

Linearized transconductance circuits have been used to implement g_m stages [6, 7], as shown in Figure 14. The transconductance of such a cell is given in (24). G_m depends on bias current I_d and sizes of the transistors are M_1 and M_2. Equation (25) defines k_3 and k_1. In this circuit, M_1 and M_2 operate in the triode region, which improves the linearity of the circuit. Linearity is rather important in our system, because the input to the low-pass filter has a large signal swing. The common-mode voltages of the transconductance circuits are set by the common-mode feedback circuit shown in Figure 8.

$$G_m = \frac{4k_3\sqrt{k_1 I_d}}{4k_3 + k_1} \tag{24}$$

$$k_k = \frac{\mu_k C_{ox}}{2} \frac{W_k}{L_k} \tag{25}$$

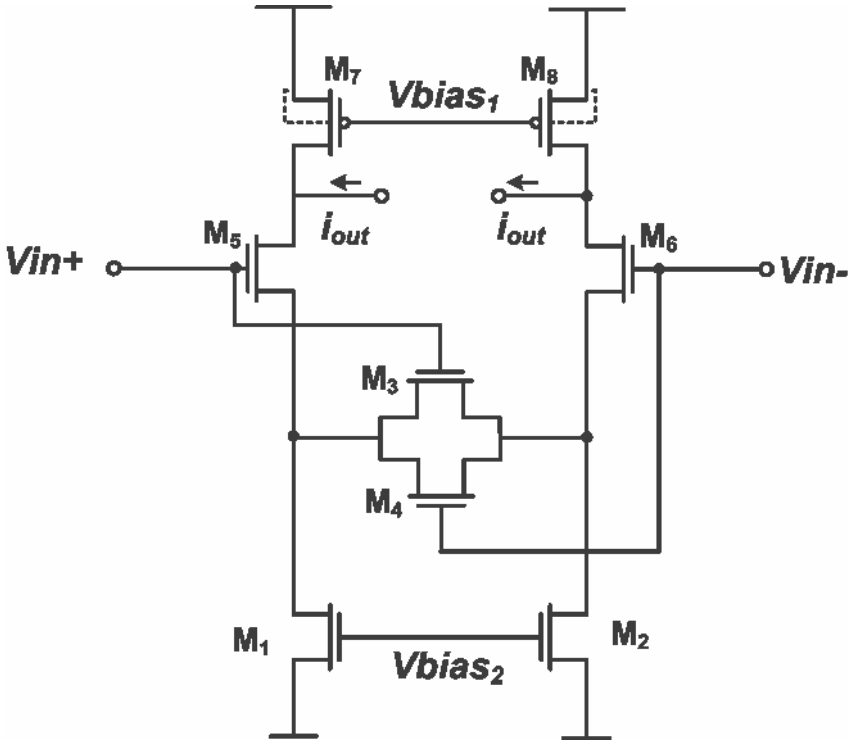

Figure 14. Linearized transconductance circuit

To better understand the g_m circuit, first we consider that it does not have any source degeneration at all. The output current, then, will be a function of V_{gs}^2:

$$I_{out} \propto k \times V_{gs}{}^2 \tag{26}$$

This is not a good setup because it has a non-linear association. In order to increase linearity, we can use resistors across the sources of the input transistors. In this case, most of the output current will be a function of the voltage across the resistors, reducing the effect of the squared input voltage.

$$I_{out} \propto R \times V_{in} + k \times V_{in}^{\,2} \tag{27}$$

Let's further assume that, instead of resistors, MOSFETs operating in triode region are used. These MOSFETs can be tied to a fixed voltage. The problem with that approach is that as the input signal gets bigger, so do the Vds values of the degeneration MOSFETs, making them less linear. To compensate for this, the gates of these can be tied to input pins, which will assure that they operate in the triode region [7].

In this design, the cut-off frequency of the filter is chosen as 5 kHz because most neural signals have less than 5 kHz bandwidth, and DC gain is desired to be unity, because the inputs to the low-pass filter are already amplified. The g_m and capacitance values that satisfy these specifications are listed in Table 1.

Table 1: Characteristics of the low-pass filter

Gm1	753 nS
Gm2	1.179 uS
Gm3	787 nS
Gm4	674 nS
C1=C2	30 pF

3.4 Simulation Results

A transient simulation of one channel of the system is shown in Figure 15. The curves at left represent the voltages shown in Figure 1 and the curves at right represent the Discrete Fourier Transform (DFT) of the transients. The input signal has 500 μV amplitude and 1 kHz frequency. In order to simulate flicker noise, a sinusoidal voltage source, which has 200μV amplitude and 500 Hz frequency, is inserted between chopper modulator and the amplifier.

This is, in fact, an overestimation of the flicker noise. The chopper frequency has been set to 20 kHz. The output signal shows that most of the noise has been low-pass filtered. In reality, flicker noise at 500 Hz would be much smaller, on the order of microvolts, which can be derived from the formula given in Chapter II, Equation (2) using typical values.

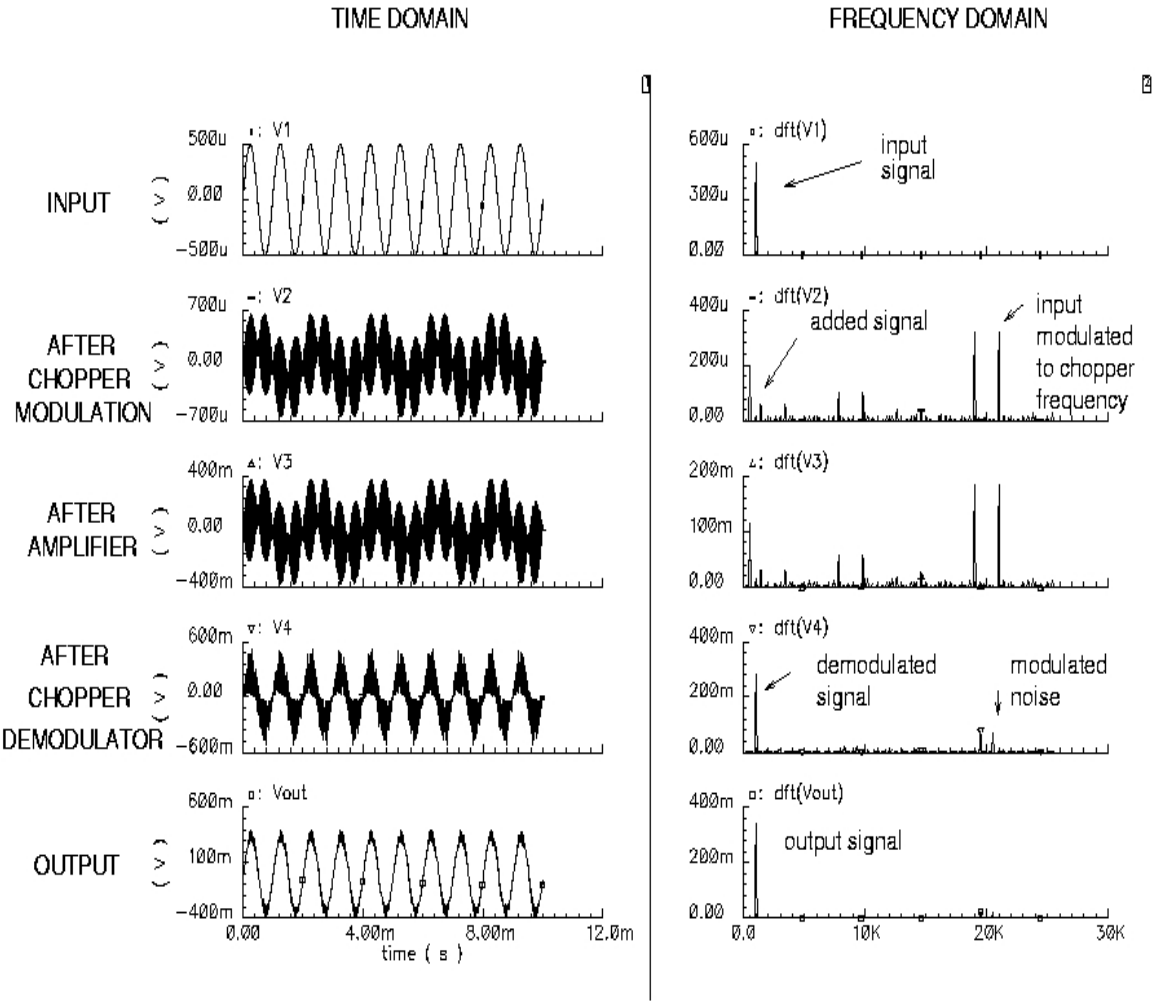

Figure 15. Simulation results

The summary of the simulation results is given Table 2.

Table 2: Summary of the results

Supply Voltage	5V
Power Consumption	<750 uW
DC Gain	650
Amplifier Bandwidth	115 kHz
CMRR	<80 dB
Input referred noise	<16 nV/rt(Hz)

3.5 Amplifier System

The circuit discussed previously has been used in a system designed for neural recording applications. A chip was manufactured in the MOSIS AMI ABN 1.5 micron technology process. A block diagram of the designed chip can be seen in Figure 16.

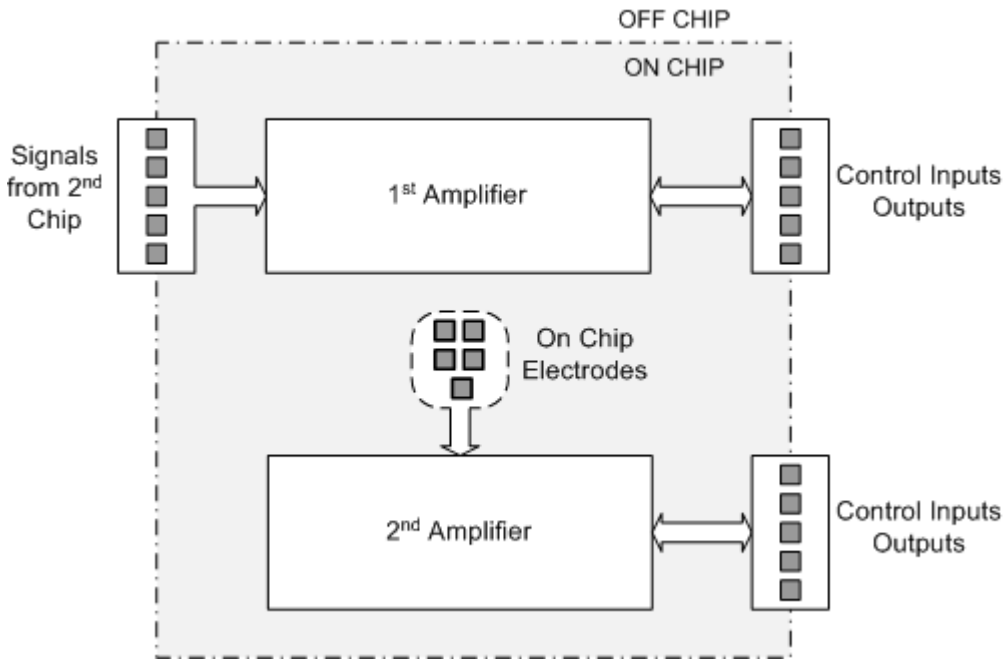

Figure 16. Diagram of the manufactured "NeuroChip"

Two identical amplifiers were used in this process. The first one, labeled "1st Amplifier" in the figure, is designed to work with an external recording environment. An electrode array or a neuro-transistor array [3] can be used as inputs to this amplifier.

In the case of using a neuro-transistor, for each of the four channels, PMOS-based load transistors were inserted at the front end to shift the input voltage to the amplifier's operating DC voltage. The front-end diagram is shown in Figure 17.

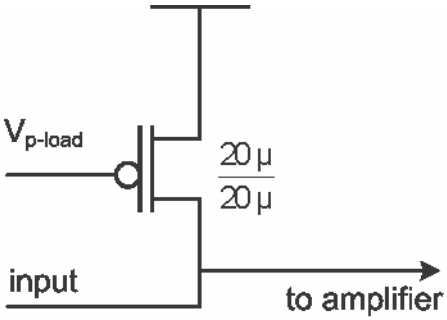

Figure 17. Front end

3.6 Metal recording sites on MOSIS chips

The second amplifier in this system accepts inputs from an internal 4-site recording array. For on-site recording arrays, it is important that they can be manufactured via a commercial process. The most feasible option was to use probe pads as the recording interface. Probe pads are basically exposed metal contact points which are created by etching holes in the last passivation layer. There was a complication in this approach. Because we wanted to create a stimulation and recording site very close to each other, we needed to put two probe pads very close to each other so that the neuron could touch both of these pads, while providing enough insulation between them. The design rules did not allow us to put two probe pads closer than 30 µm. A study of the process revealed that we could ignore one of these design rules and put two metal contacts as close as 5 µm to each other and create a single glass-cut to cover them

both. Even though this did not strictly pass the design rule check, we determined that it was safe to assume that the circuit would be manufacturable.

A layout picture of this can be seen in Figure 18.

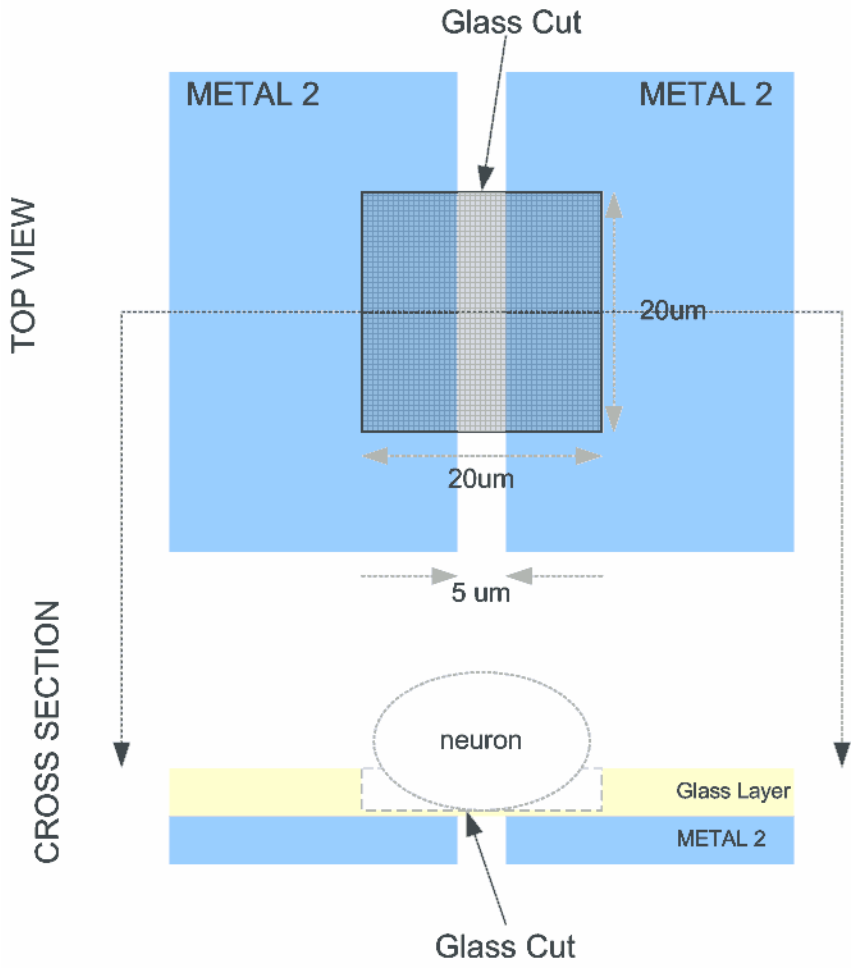

Figure 18. Internal Electrode

The close-up picture of the electrodes can be seen in Figure 19.

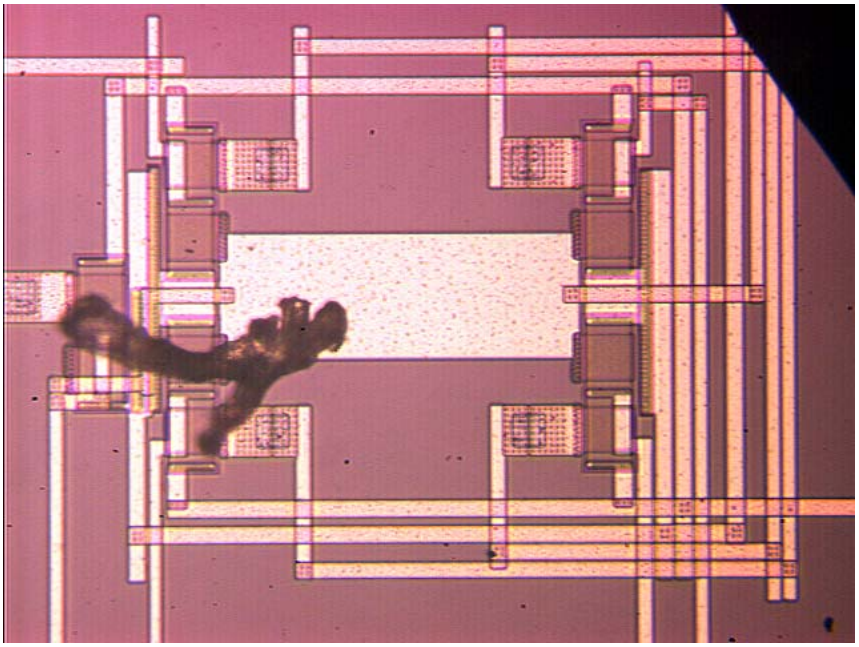

Figure 19. Electrode Array on MOSIS chip

In order to bias the neural signals with the DC operating voltage of the amplifier, a PMOS-based level shifter circuit is used. Figure 20 shows this circuit. The DC bias voltage of the PMOS load can be changed to bring the amplifier's input signal to the right bias voltage of the amplifier input.

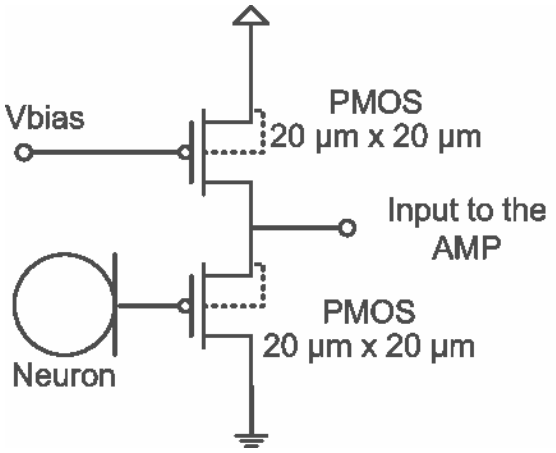

Figure 20. PMOS source follower

Unfortunately, the internal-electrode-based circuit did not work. The reason for this might be that the calculations for DC operating point were off because of the mismatches that were caused by the manufacturing process. The rest of the circuit was identical to the first circuit.

Some of the packaged chips were encapsulated with epoxy glue and Petri dishes to create a chamber for neurons. The final product can be seen in Figure 21.

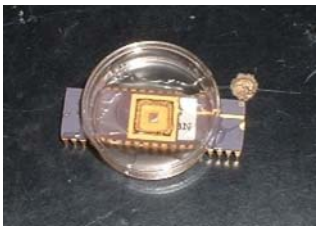

Figure 21. Encapsulated chip

3.7 Neural input pads

In order to protect the chip from static electricity, most of the pins used an electrostatic discharge (ESD) protection circuit. In order to avoid any additional noise being injected into the weak neural signals, the input pins to the first amplifier were not equipped with ESD protection circuitry. A picture of the pad can be seen in Figure 22.

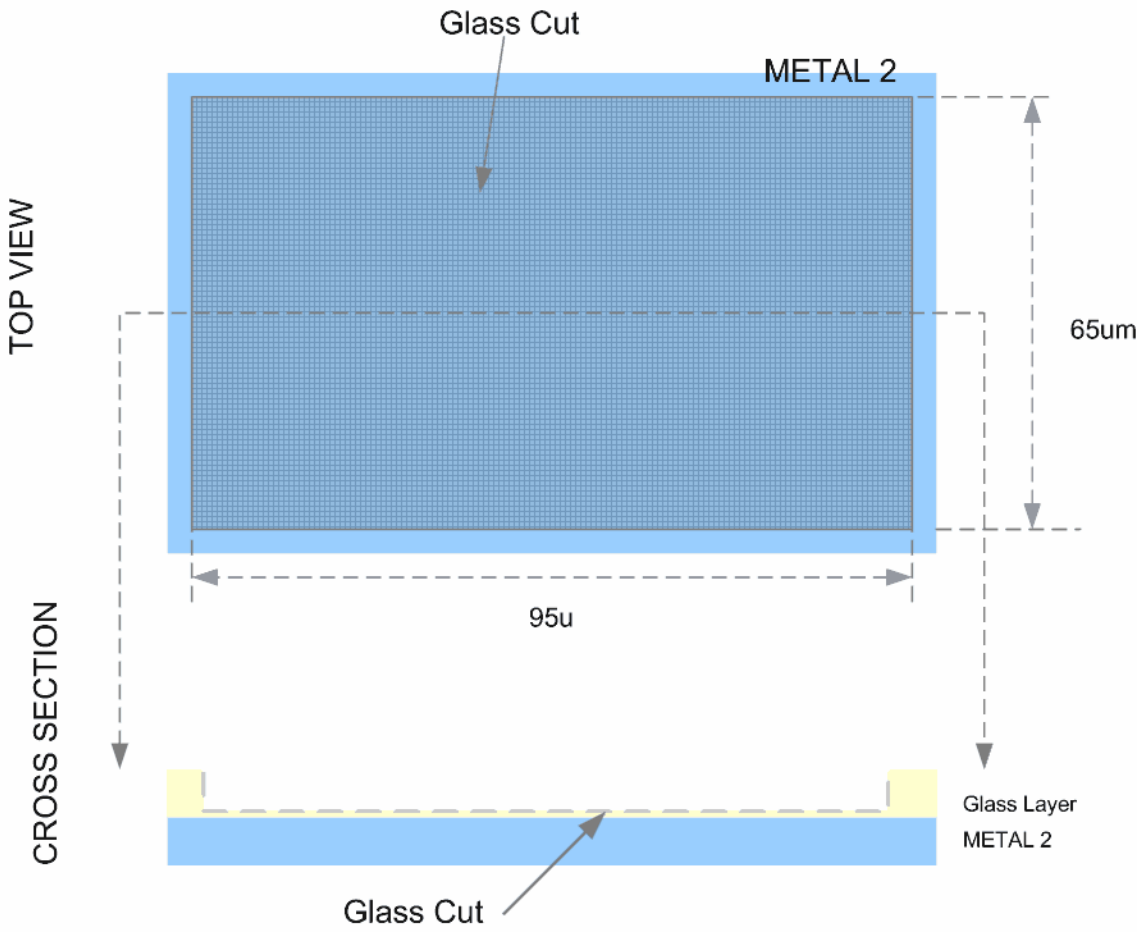

Figure 22. Neural Input Pads

3.8 Chip overall

A picture of the MOSIS chip can be seen in Figure 23. It was manufactured at MOSIS using their AMI ABN 1.5 um technology. The chip was 2.2 mm x 2.2 mm in size and packaged in a 40 pin DIP package. All tests were performed on packaged parts.

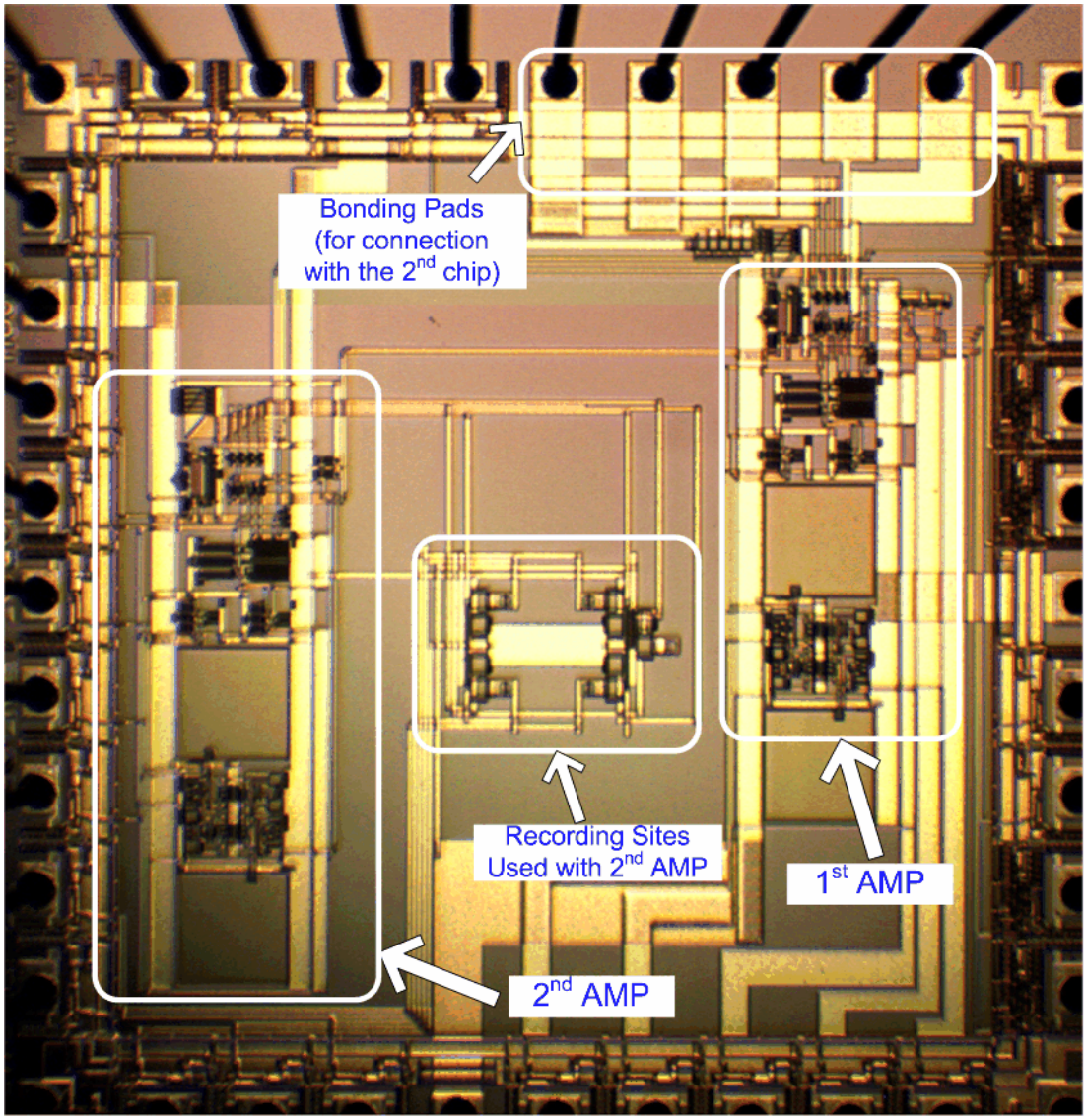

Figure 23. Picture of the MOSIS chip

The pin assignment diagram is shown in Figure 24.

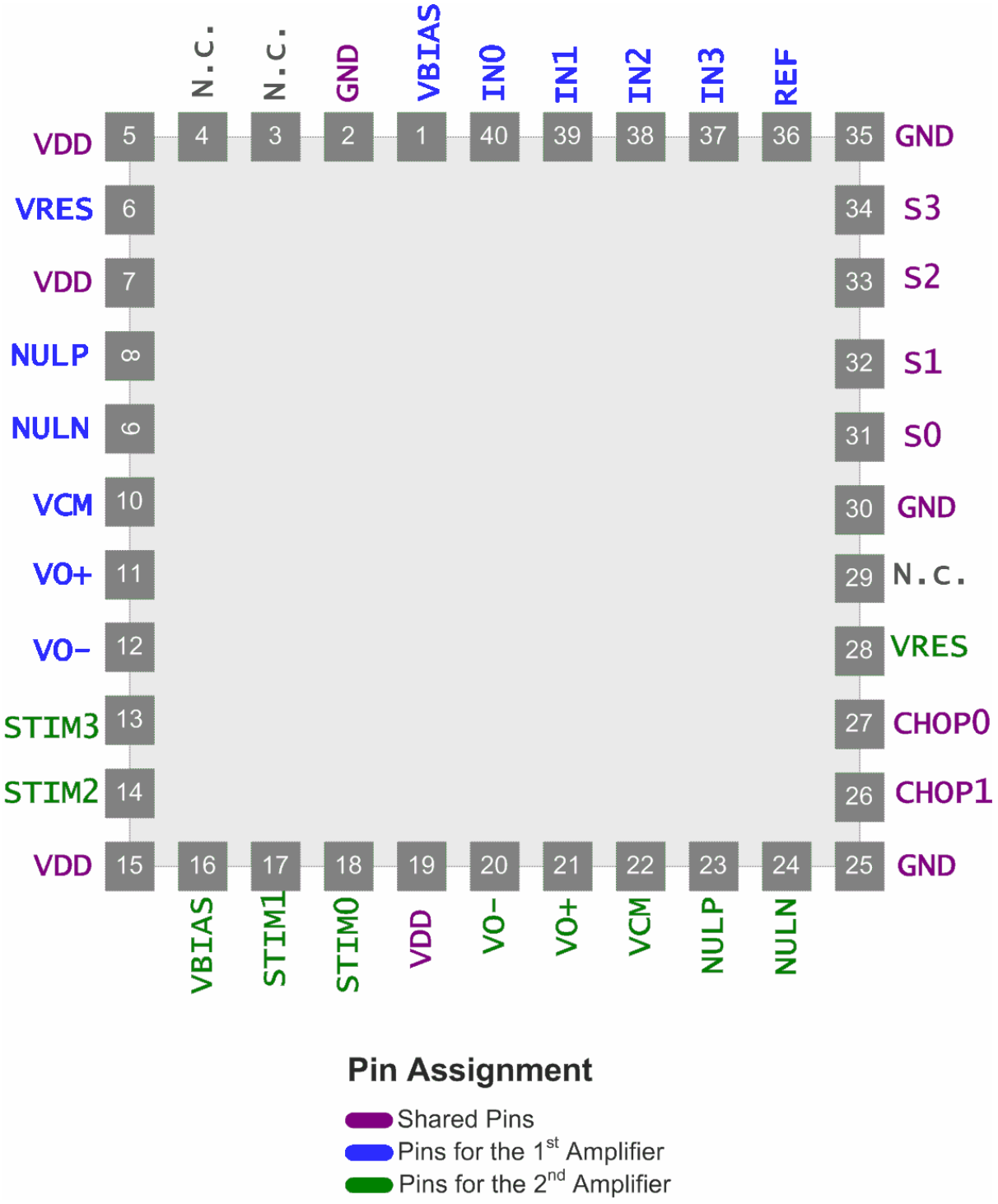

Figure 24. Pin assignment for the MOSIS chip

3.9 Neuron Transistors

Another way of interfacing neurons with the amplifier system was pursued. Creating FETs without gate metal to interface the neurons was successfully demonstrated by the German group led by Dr. Fromherz [3].

3.9.1 Process Steps

The main process steps are as follows [8]

- An approximately 400 nm thick field oxide is grown over a p- substrate.
- A pattern of silicon dioxide is grown all over the chip.
- Using photolithography, the active areas for source and drain are defined.
- SiO_2 is etched to expose sources and drains of the transistors, as well as the stimulation areas.
- The junctions are created (n+ for a p- substrate); this is mostly done by diffusion but sometimes ion implantation is used.
- The metal contacts are deposited. (Either Al or W).
- The whole chip is covered with low temperature oxide (instead of silicon nitride).
- The gate areas are etched with HF to leave a 10-15 nm thin oxide.

Figure 6 shows the cross-section of the device after the process. The process is similar for P-type transistors, except the wafers are N type and the diffusion is replaced with a boron implant.

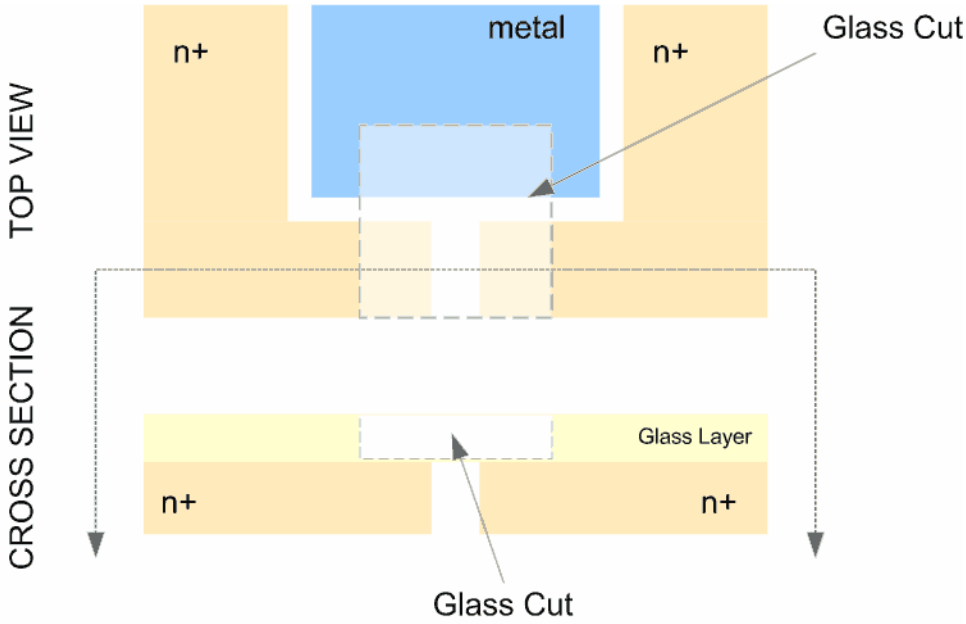

Figure 25. Neuro-Fet with metal stimulation spots

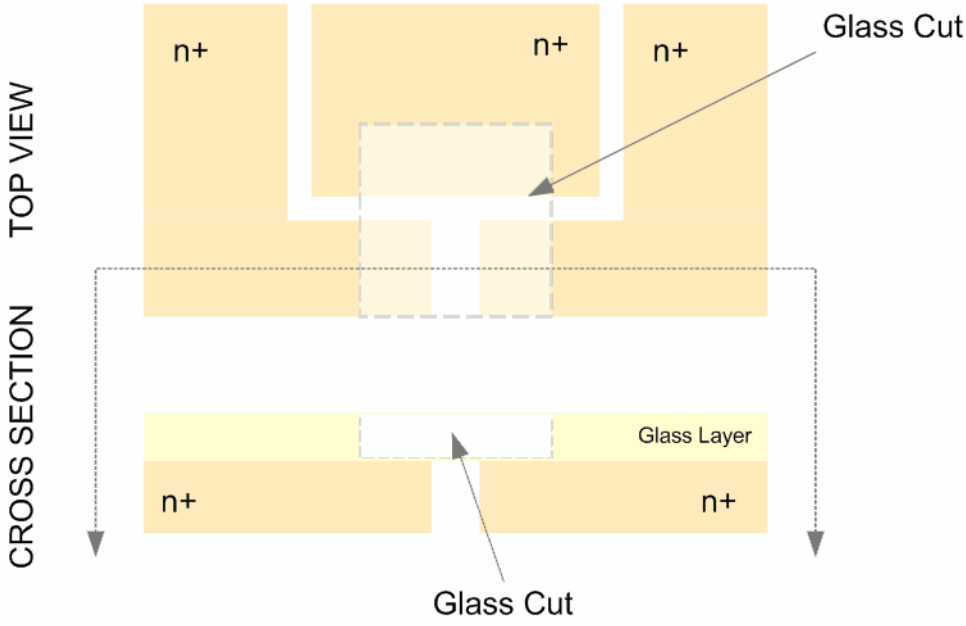

Figure 26. Neuro-fet with n+ stimulation spots

Each chip was manufactured with 4 transistors, 2 of each stimulation spot given in Figure 25 and Figure 26. The overall picture is given in Figure 27.

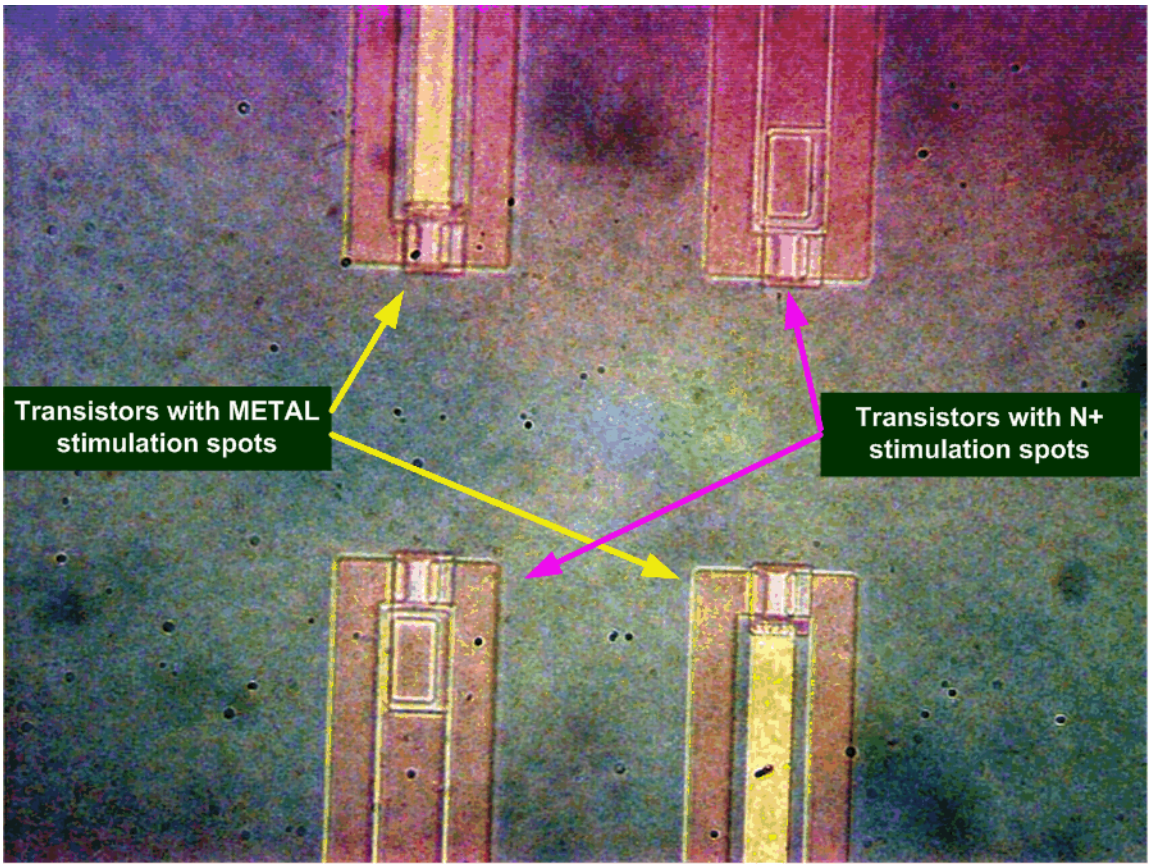

Figure 27. Picture of the Neuron-Fet Devices

3.9.2 Packaging and Bonding Problems

These chips were glued to a 68-pin DIP chip-carrier. In order to be able to use them with other chips, we needed to bond the pins and enclose the chip with a chamber. The final product was as seen in Figure 27.

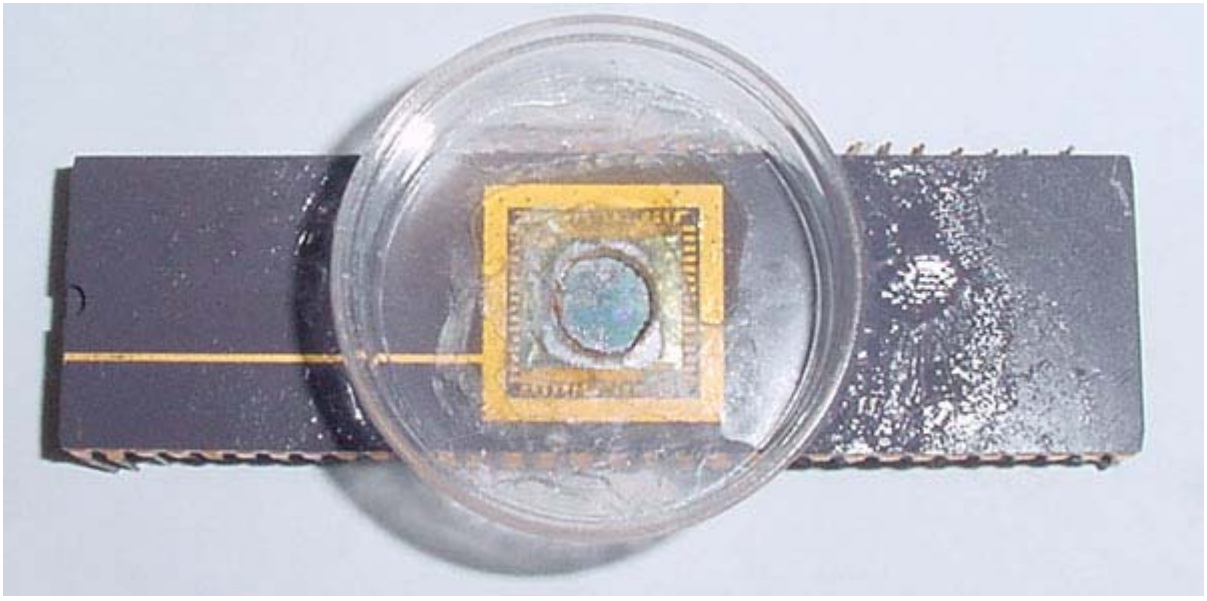

Figure 28. Picture of the bonded N-Chip

We encountered problems with bonding the pads to the contacts on the chip carrier. We think the following facts prevented a successful bond:

- The pad material used was aluminum for some chips and tungsten for others. Tungsten pads were just too rigid to accept a successful bond.
- There was a significant amount of oxide left on the pads which made it difficult to create strong bonds.

Although several kinds of workarounds were attempted, no success was achieved with the bonding so this method was abandoned.

3.10 Using Commercial Electrode Arrays

Another way of recording electrical activity from neurons is using commercial electrode arrays. One example is an 8x8 array of electrodes made by Panasonic [9]. We also tried to

record from one of these with a commercial amplifier system. Initial attempts were unsuccessful. Figure 29 shows the chromaffin cells plated on MEA dish.

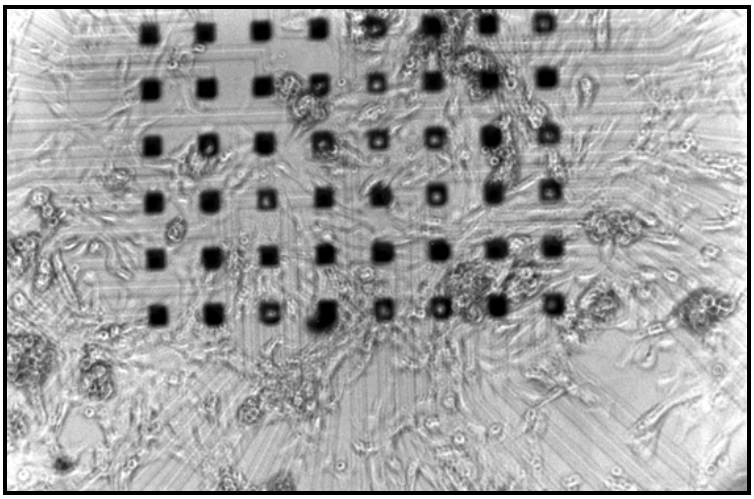

Figure 29. Chromaffin cells plated on MEA dish

3.11 Test boards and test results

Several test configurations have been implemented.

3.11.1 Testing the chopper-modulated amplifier

In order to verify the chip's operability, we used static signals fed into the 1st amplifier. The first set of tests was performed using an sinewave input signal with 1.6mV amplitude operating at 1 kHz. In order to get this low amplitude we used an attenuator to divide a 240 mV signal from a commercial signal generator by a factor of 150. The chopper clock operates at 50 kHz and was also created by a signal generator.

The setup block diagram is shown in Figure 30.

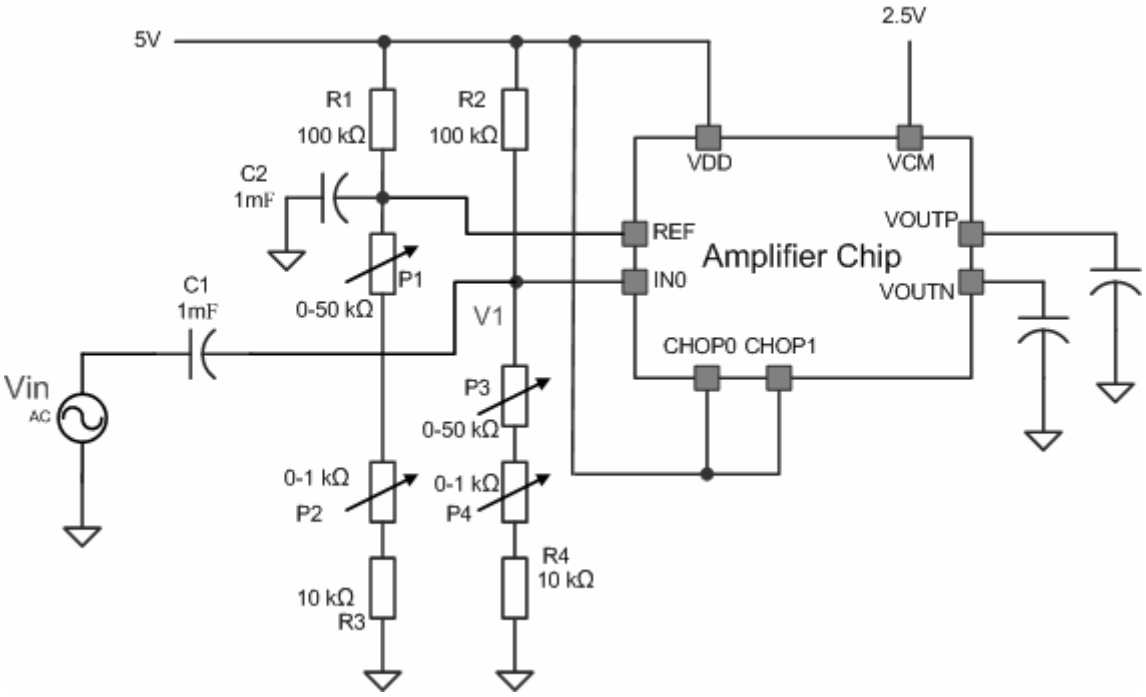

Figure 30. Test Setup

The output results are shown in Figure 31.

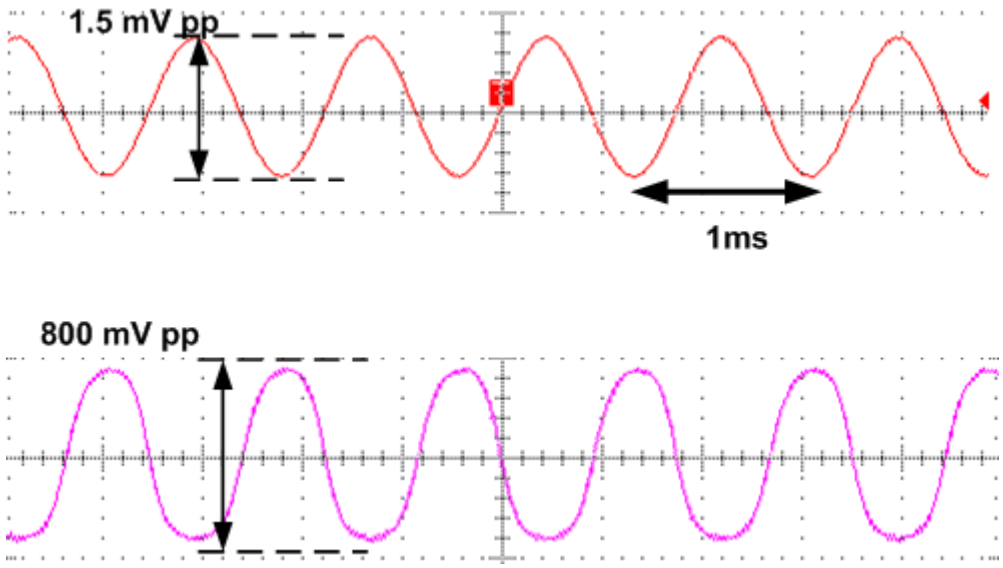

Figure 31. Amp input & output

The output amplitude was approximately 800 mV.

3.11.2 Flicker noise measurements

For flicker noise measurements, no input signal was required. The output of the amplifier was fed into a National Instruments data acquisition card and the output spectrum was measured with and without chopper modulation. In Figure 32, The output noise at 263 Hz is shown to be around -60 dB. In Figure 33, the output spectrum is shown for a chopper modulation at 50 kHz. We can clearly see a -20 dB reduction in noise at 263 Hz. The high frequency noise has increased but this can be remedied by using another low pass filter, or it can be removed with software.

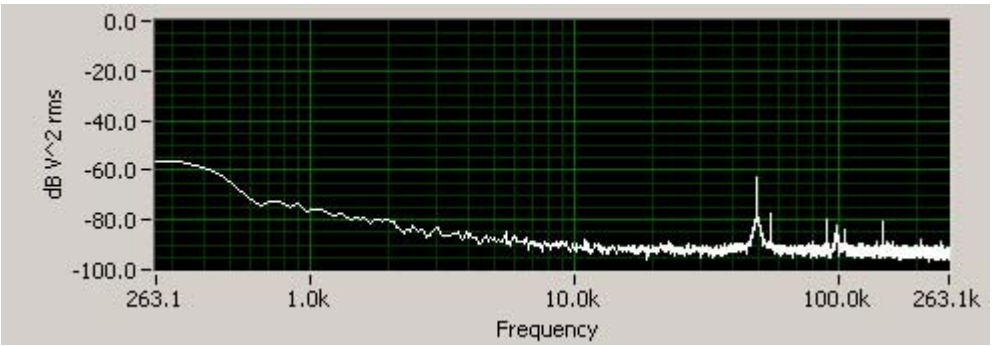

Figure 32. Spectral analysis of the Neurochip's outputs **without** chopper modulation. The signal is averaged over 8 samples to reduce the effects of the random noise on the graph. Output noise and offset is around -60 dB at 263 Hz. The noise corner is around 10 kHz.

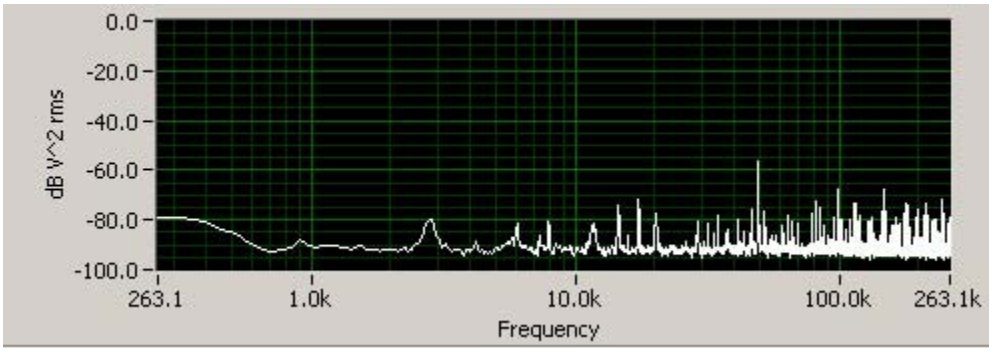

Figure 33. Spectral analysis of the Neurochip's outputs **with** chopper modulation. This test also utilized averaging over 8 samples. The low frequency output noise is reduced to -80 dB at 263 Hz.

3.11.3 Testing of Neuron-FETs

In order to test the chips, a PDMS mold was created on top the transistor recording sites and as for the electrolyte, a 1 mM solution of tetrabutylammonium hexafluorophosphate in propylene carbonate was used. A silver wire was used as the contacting electrode to the electrolyte. The V_{gs}-I_d curve for one of the first transistors is shown in Figure 34.

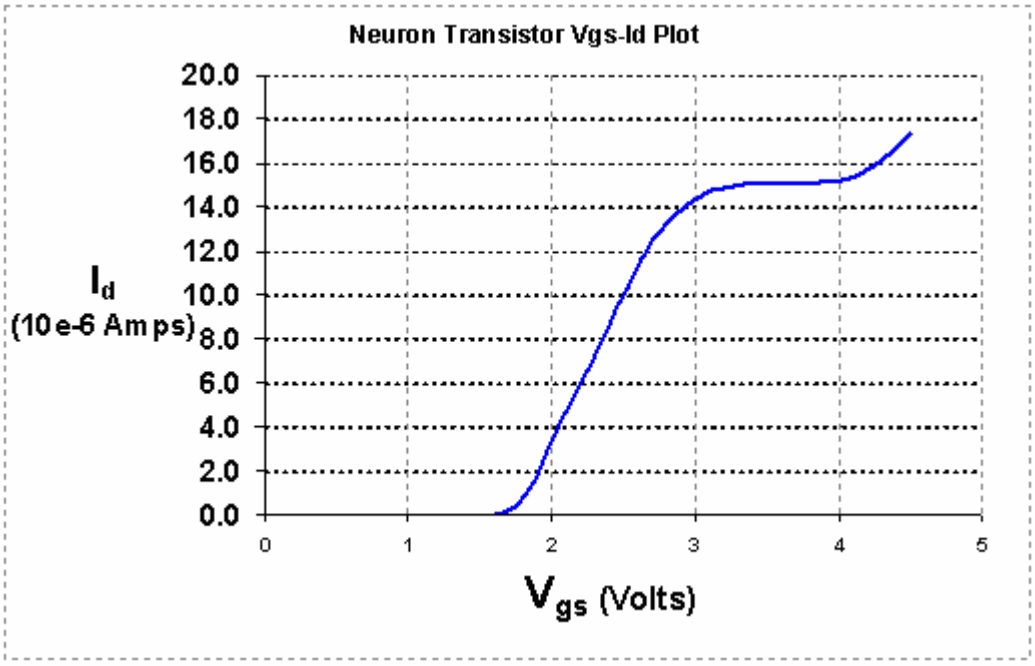

Figure 34. Neuron transistor VGS - ID curve (VDS=2.5 V)

3.11.4 Test setups for in-vitro testing

Two circuit boards were designed to make in-vitro recordings and test our amplifier in an actual neural-recording environment. The first setup is shown in Figure 35.

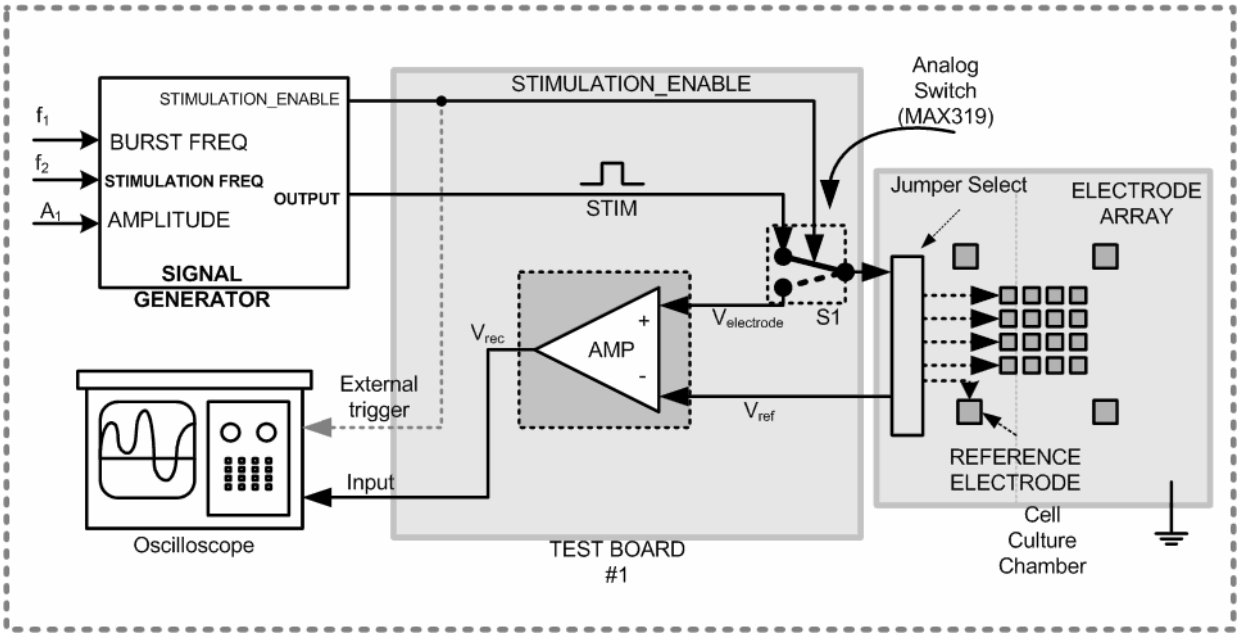

Figure 35. Test Board # 1

In this setup, a stimulator is created using a signal generator and a buffer. This setup is used to create voltage pulses required for stimulating the cells. F1 represents the *burst frequency*, which is the duration of stimulation. F2, is the *stimulus frequency,* and is used to set the duration of each pulse. The detailed information for the signals is shown in Figure 36.

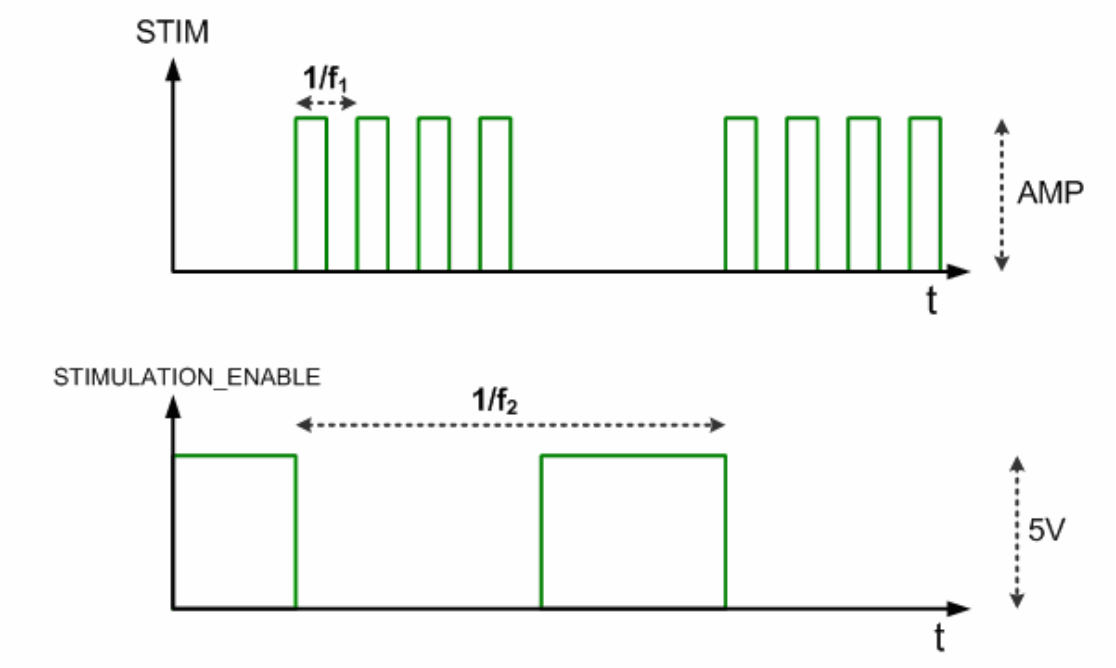

Figure 36. Signals for the Test Board # 1

In this setup, a site that has a number of cells is selected by setting one of the jumpers on the cell culture chamber board. During stimulation the recording path is disconnected from the stimulator path via a commercial analog multiplexer (Maxim MAX319). A `STIMULATION_ENABLE` signal is used to control the multiplexer. After the stimulation period ends, the stimulation path is disconnected and the recording path is connected.

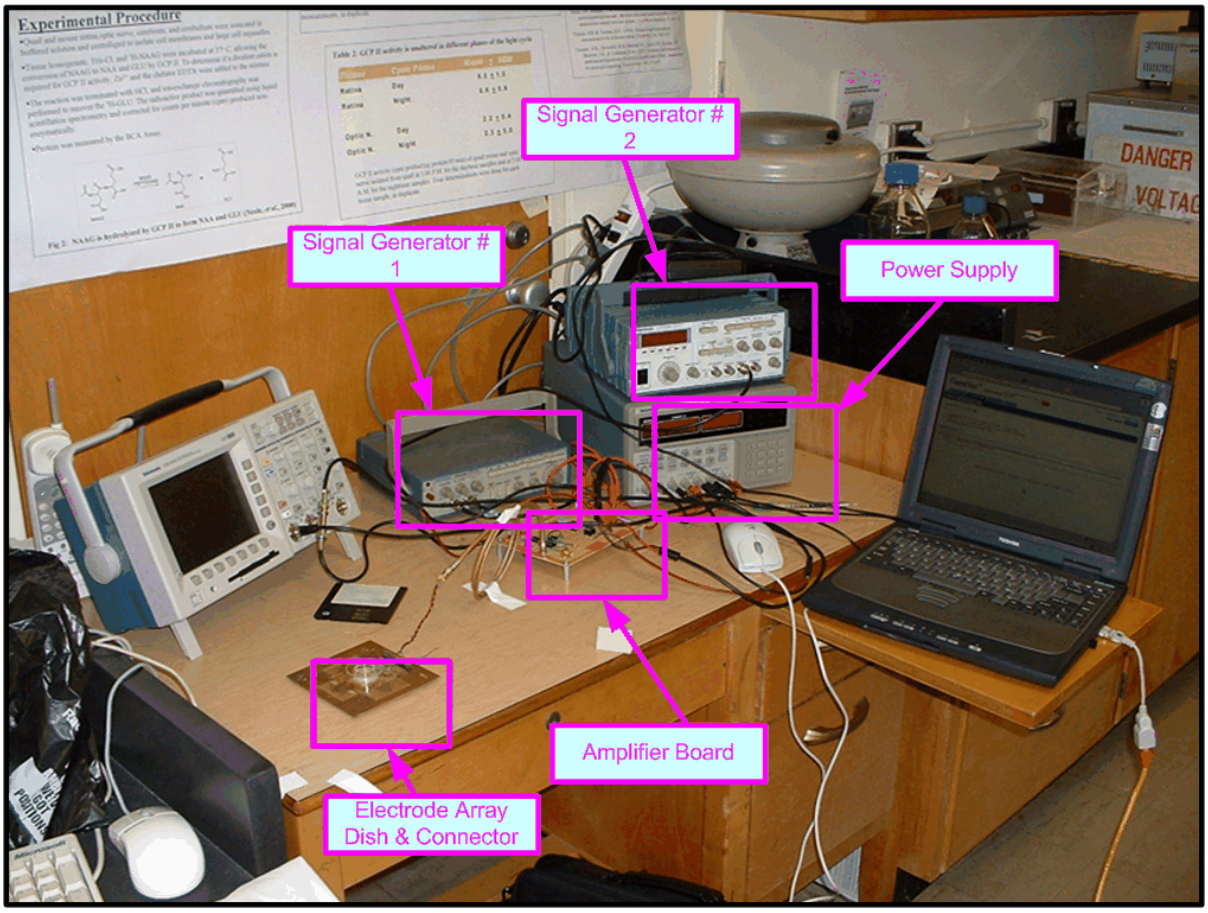

Figure 37. Setup for Test Board # 1

The second testboard is shown in Figure 38.

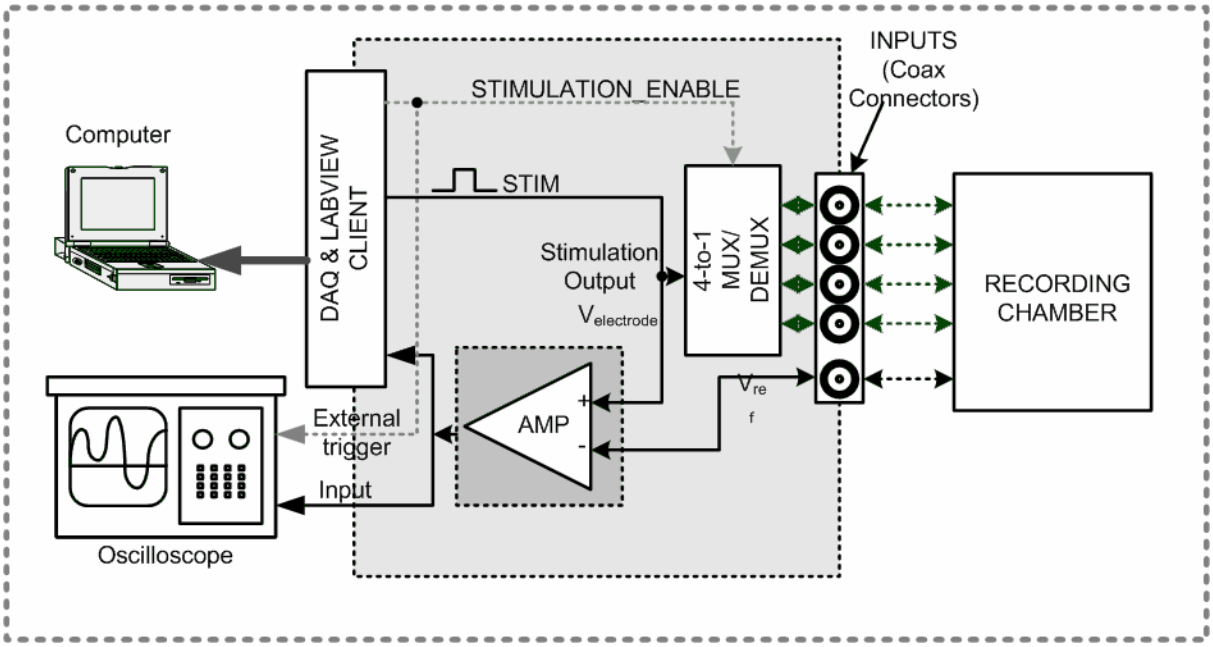

Figure 38. Test Board # 2

On the second test board low-noise RF connectors were used as the inputs from the recording source to the board. Also, stimulation source was also replaced with a computer based DAQ system. The DAQ is also used to record the signal activity.

3.12 Neurochip Testing Problems

3.12.1 Introduction

The purpose of this subchapter is to explain the circumstances which led my chip to fail in an actual neural recording environment while it worked as designed with synthetic signals. I will also offer solutions to these problems.

The chip was designed to work as an open-loop amplifier and provides very high gain with a single stage amplifier. The problem with this approach was that it was necessary to set the

DC level of the inputs to a very specific voltage in order to set the amplifier at its optimum operating conditions because of the biasing scheme used in the design.

The solution to this problem was to use a resistor divider to set the DC level and add the signal to this bias point. It was necessary to adjust the bias voltage with potentiometers because the bias point has to be at a precise voltage within about 10 mV.

This biasing stage reduced the effective input impedance of the amplifier to 28 kΩ. The system was tested in the lab with synthetic signals generated by using a signal generator. This source has low (50 Ω) output impedance so the 28 kΩ load did not attenuate the signal at all. Once the bias potentiometers were properly adjusted, a 1 mV signal input was properly processed by the system.

In the lab experiments, however, the reduced impedance of the input stage created a problem. The output impedance of the probing system used to measure actual signals in tissues is significantly higher -- roughly 3 to 5 orders of the magnitude -- which means the combined system gain turns out to be less than unity. This fact was verified by simulations which show that the impedance of the metal-amplifier interface combined with impedance of the modified input biasing circuitry never allows for sufficient total system gain. The high impedances cause the input stage to become a high pass filter with a passband that starts well beyond the frequencies of the neural signals.

The above considerations show that the main novel contribution of the thesis - that adding chopper modulation to reduce flicker noise in this type of system is useful - is valid and can be made to work. All of the circuit elements work individually but the total system did not work properly due to the biasing issue in the amplifier. But this problem is merely an implementation issue that can be resolved by redesigning the bias circuits in the amplifier. Since this can obviously be done there doesn't seem to be much point in actually doing it.

3.12.2 Analysis of the problem

The amplifier was designed to work in an open loop configuration and create a very high gain. The drawback of this approach was that the input signal's DC level must be at a very precise voltage level with about 10 mV error margin.

The solution to this problem was to use a resistor divider network which set the bias voltage for the input stage. Figure 30 shows the diagram of the setup. Potentiometers P1 and P3 are used for coarse adjustment, while potentiometers P2 and P4 are used for fine adjustment of the bias voltage.

The consequence of using this method was that when the correct bias points were adjusted the effective input impedance was dominated by parallel combination of these potentiometers, which worked out to roughly 28 kΩ at the frequencies of interest.

The output impedance of the source and the input impedance of the amplifier play a major role in transferring the signal. An ideal voltage source has zero output impedance and an ideal amplifier would have infinite input impedance. This would allow the transfer of the signal without any loss.

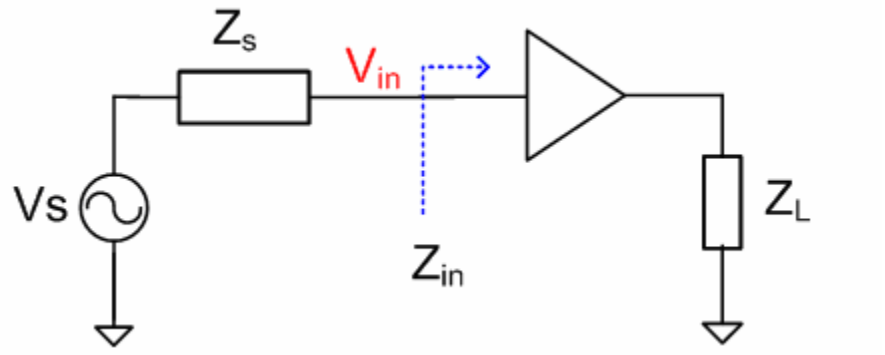

Figure 39: Model of a voltage source and an amplifier

From Figure 39, we can say the voltage labeled as Vin will be the following:

$$Vin(s) = \frac{Zin(s)}{Zin(s) + Zs(s)} \times Vs(s) \tag{28}$$

So, when |Zs| << |Zin| , |Vin| ≈ |Vs|.

To test the chip for functionality a signal generator was used as an input source. The output impedance of the signal generator was reported to be 50Ω. Compared to the 28kΩ effective input impedance, the output impedance of the source was therefore relatively small; in fact 98% of the signal was transferred, so the chips were functional under these conditions. The gain was verified to be about 55 dB and at least 20dB flicker noise reduction was observed at low frequencies. Figure 31 shows an input/output waveform of the amplifier at 50 kHz chopper frequency. Figure 32 shows the noise measurement without chopping and Figure 33 shows the noise spectrum when a 50 kHz chopper frequency is used. A 20 dB reduction was achieved at 263 Hz with chopper modulation.

The problem was that in the actual neural recording tests, using both metal electrode arrays and extracellular recording electrodes, the output impedance is large. In the case of using commercial metal electrode arrays this output impedance can be reduced to a very low and acceptable amount by means such as depositing platinum black on the recording electrode. In fact, the specification of the electrodes used reported that they would have an effective 22 kΩ measured at 1 kHz. But this impedance is not guaranteed. First of all, the impedance significantly increases after each use and this increase also depends of the way the electrode arrays were cleaned, maintained and stored. It is not possible to estimate quantitatively which actions will change these parameters. The only way to know for sure is to actually measure the impedance characteristics before each use, which I did not do. However, some empirical studies have been presented [10], which only show the how the impedance increases after each use. The other factors, such as byproducts of the cells, changing acidity, length of incubation, etc., would only worsen the situation. There are some cleaning

techniques recommended by the manufacturer, but they also state that these electrodes are intended for disposable use. They do not recommend using an electrode more than ten times.

Before I attempted any recordings, I used the array chamber for culturing cells many times. The process of learning the culturing methods required that I reuse the array many times. By the time I did start to perform recordings, the properties of these electrodes had probably changed drastically which almost certainly resulted in electrodes with very high output impedance. I also observed that the metal was being stripped away, as can be seen at Figure 40 and Figure 41, from most of these sites and the ITO underneath the Platinum Black is known to have very high impedance. (That's why the platinization is done in the first place. If ITO could be used, Platinum Black would not be necessary). It is probably safe to say that as a result of all these factors, the impedance got extremely high and most of the signal was attenuated before it is even passed on to the amplifier in any recording experiments.

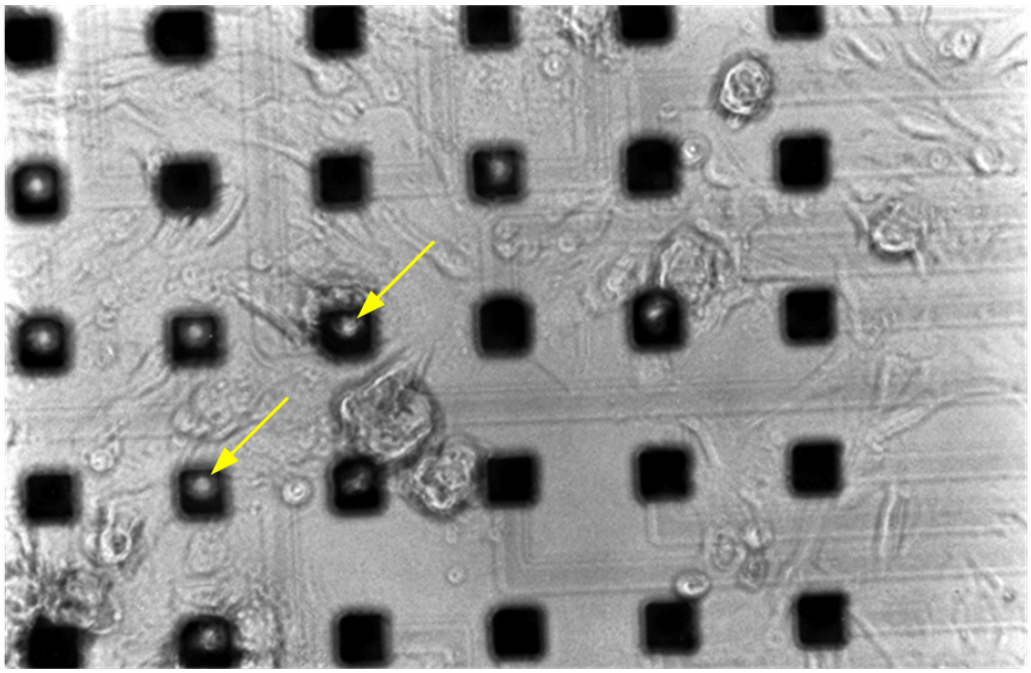

Figure 40: White spots on the recording electrodes show the stripped metal

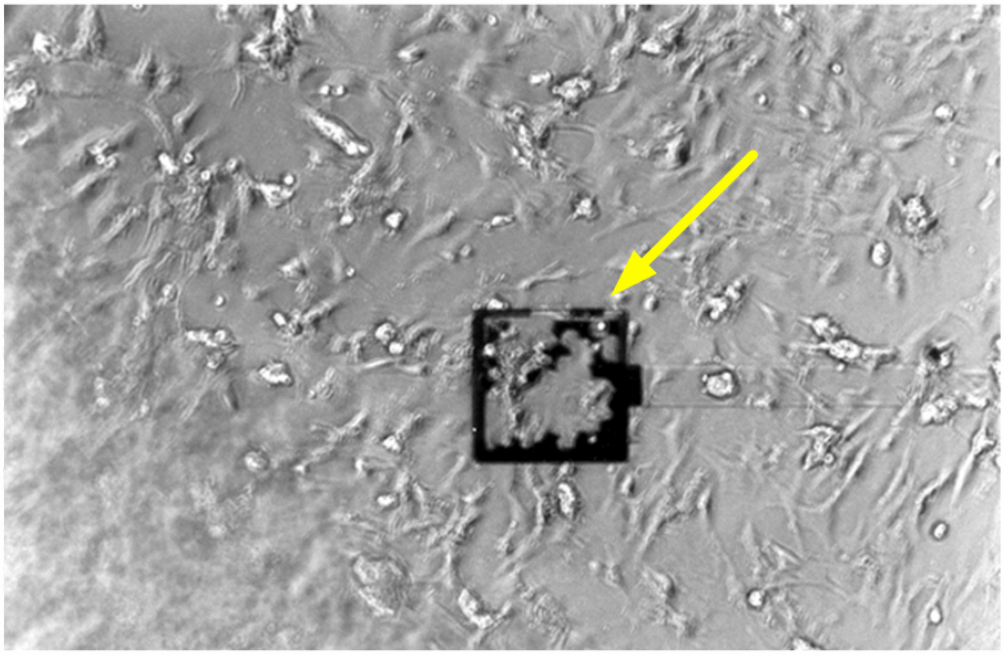

Figure 41: A reference electrode almost completely stripped off of its metal

In order to better understand the interface between the metal and the electrolyte we will try to use the published models for such an interface and determine if the system could have worked theoretically. Since the actual tests we have done involved metal electrodes, we will first investigate a model of the metal-electrolyte interface. A generic model has been given by Borkholder et al. [11] which is shown in Figure 42.

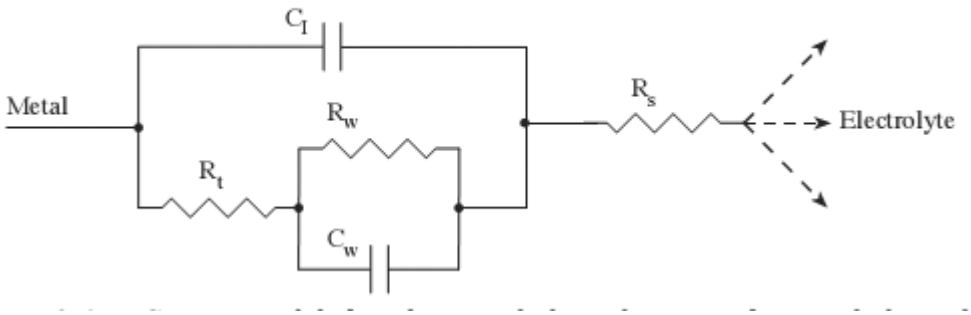

Figure 42: Metal-Electrolyte Interface [11]

If we add this interface to the setup shown in Figure 42., we will have a model as seen in Fig 43. (In this figure, some of the resistors and potentiometers are combined and shown connected in series for simplicity, but the circuit is the same…)

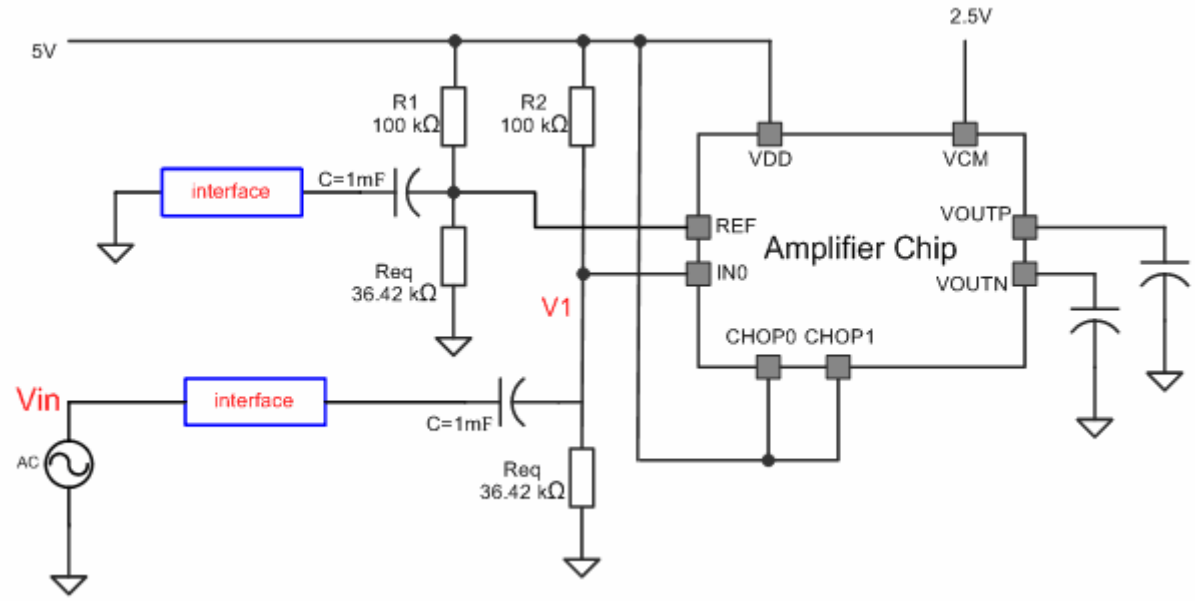

Fig 43: Setup with interface

The block labeled as “interface” is the model shown in Figure 42.

For this interface model, the most common values for the model parameters are the following [11]:

Table 3: Metal-electrolyte interface common values

Parameter	Worst Case	Best Case
CI	10 pF	326pF
Rt	214 MΩ	6.8 MΩ
Rw//Cw	2.4 nF // 65 kΩ	80 nF // 2 kΩ
Rs	82 kΩ	15 kΩ
Cp	1 pF	1 pF

In the "Best Case" values, the interface should have a small resistive and large capacitive path. The "Worst Case", is the complement of this.

Figure 44 and Figure 45 show the impact of the interface to the signal. As expected, the high-pass nature of the interface attenuates the signal significantly at low frequencies. So, using published values to the metal-amplifier interface, these simulations show that the bias circuit workaround does indeed cause the overall system to fail.

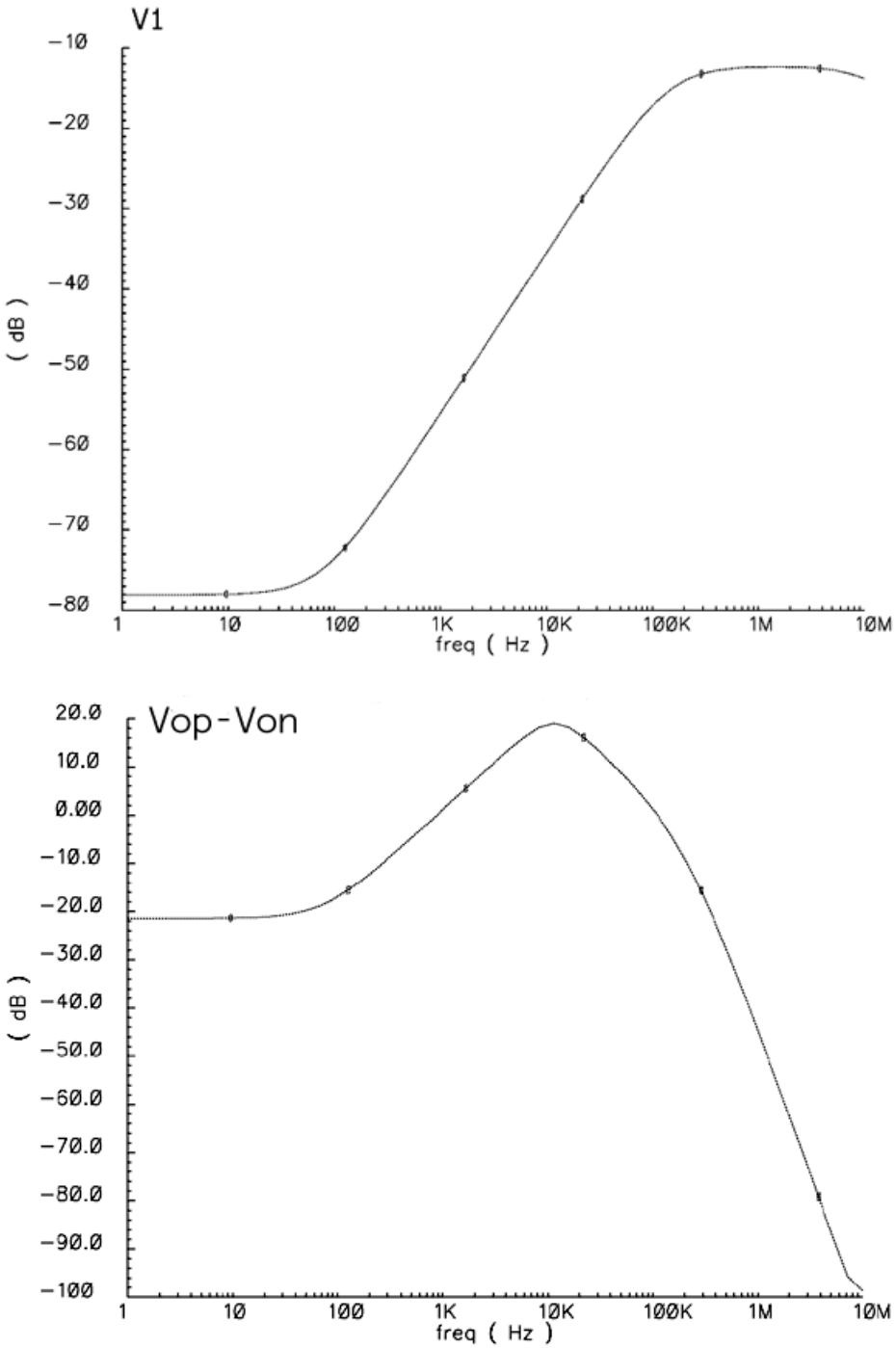

Figure 44: Output transfer function for V1 and Vout for “worst case” parameters

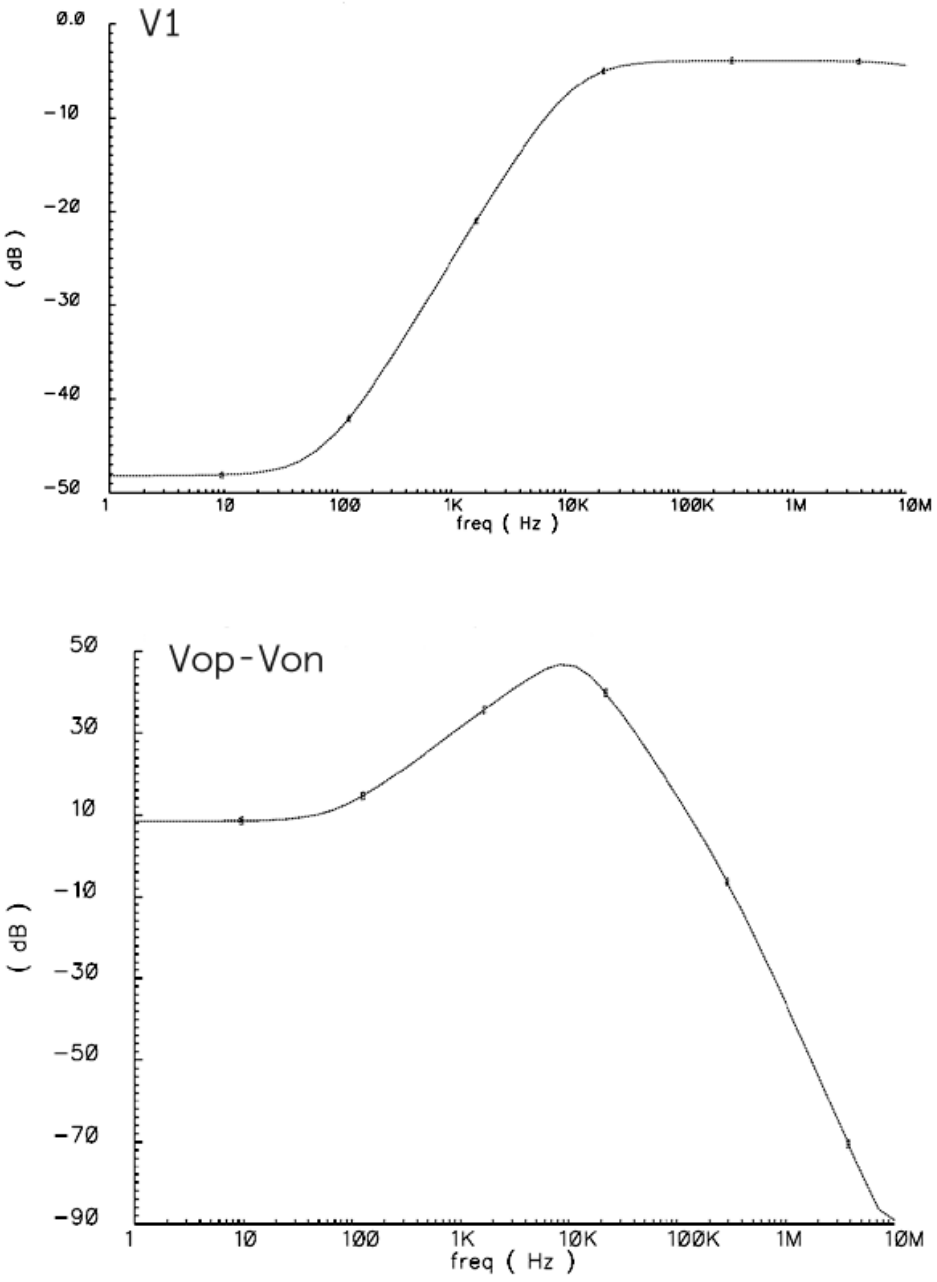

Figure 45: Output transfer function for V1 and Vout for “best case” parameters

3.13 Conclusions

From the modeling, simulations and lab results of the tests previously performed, we see that this system worked as intended using a low output impedance signal generator. The implementation of chopper modulation has been shown to remove the effects of the flicker noise in this environment. The actual neural recording tests did not work because of a minor design flaw in the biasing scheme of the Neurochip's input stage. The necessity of biasing the input signal forced me to use resistor dividers, which created the most important problem of impedance mismatching. The best way to remedy this is to redesign the input stage of the amplifier to allow DC level of the input signals to be at ground voltage.

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Chapter IV. Conclusions and Future Work

4.1 Flicker Noise Reduction – Does it matter?

In this dissertation we proposed and designed circuitry that will reduce the flicker noise and DC offset in a neural recording system. We have claimed that since both flicker noise and neural signals lay in frequencies of interest, there is a good chance it will affect the accuracy of our recordings. However, some may still ask whether or not this is in fact a big issue. One way to make this determination is to investigate the effect of the flicker noise quantitatively, perhaps using neural recording data obtained from a neuroscience group. This data will include recordings and the results of spike detection software. We can then add flicker noise using different parameters to this data and analyze the spike detection result for the manipulated data. We can then compare the results and have a good idea as to whether we have a significant improvement or not. While the neural recording data that we use as a baseline will include some flicker noise due to the amplification used in recording it, we can safely treat this as part of the signal because we are adding our own flicker noise contribution and we simply need to find out if the technique results in the same spike detection as in the original signal. The main question we need to answer is: Are flicker noise reduction techniques beneficial in some cases?

A second way to do this would be to create completely synthetic neural data, using available models for the cell–>amplifier interface to produce controlled action potentials. We can then artificially add flicker noise and analyze the detection rate.

Either technique will show us whether or not chopper modulation provides a useful improvement to a neural recording system.

4.2 Circuit Enhancements

The weakest point in this research was the input circuitry to the amplifier. While we were able to demonstrate that the approach works, this imperfection in the implementation made it

impossible for us to test it in an actual neural recording environment. The most important thing that needs to be addressed is the issue of input bias sensitivity. This must be corrected in the future.

4.3 Multi-chip / single-package solution

Another important problem with neural recording systems is the difficulty in packaging amplifier chips with the recording arrays. Normally, recording electrodes and amplifier circuitry are packaged separately and connections are made using a printed circuit board. One of our initial goals was to package the recording chip and amplifier chip in the same package. Unfortunately, bonding problems prevented us from succeeding in doing that. Meanwhile, other research groups {{35 Fromherz,P. 2002; }} have been able to implement this idea. We still think that a better system can be designed. Using a commercial process, such as MOSIS ABN 1.5 technology, chips can be manufactured relatively cheaply. But there is a limit to the number of amplifiers we can put on a single chip. By designing scalable amplifier chips, we could put several amplifier chips in the same package and increase the number of recording sites that can be monitored significantly. Figure 1 shows a possible configuration of such a system.

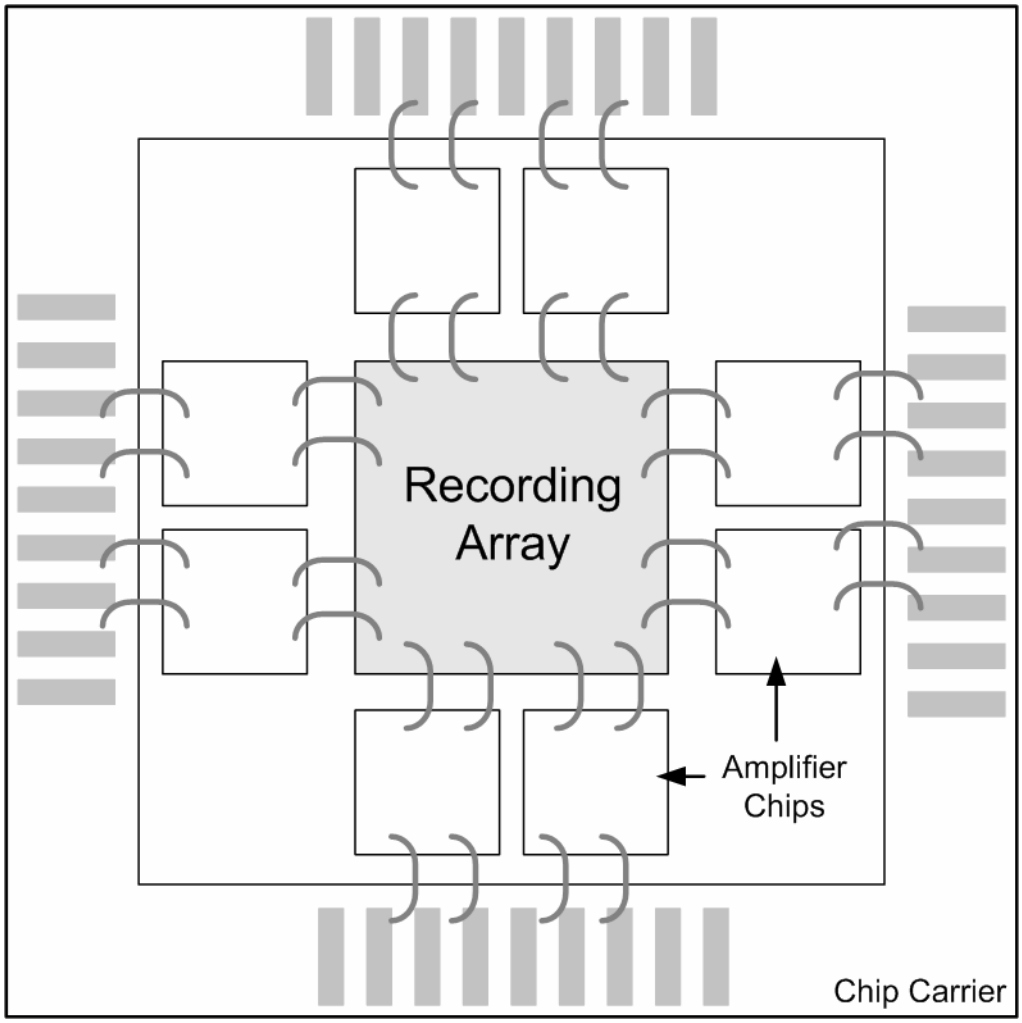

Figure 1. Multi-chip neural recording package

Of course, afterwards, this package can be encapsulated using a bio-compatible epoxy glue to expose only the recording electrodes.

Another possible improvement would be to bond chips directly to a PC board.

4.4 Neuron Transistor

The superiority of using gate-metal free transistors over metal electrodes was demonstrated by Fromherz et. al. [1] and later using the modeling work by Grattarola et al [2]. Of course,

these systems are much harder and expensive to manufacture because a custom process must be used to produce the transistor arrays. Therefore, a neuron-transistor-based commercial system has not yet been produced, but this is a path that may still be worth pursuing. Innovations may be found which significantly reduce the cost problem.

4.5 MOSIS-based microelectrode arrays

MOSIS is a very cheap way to manufacture low frequency semiconductor circuits. Our attempt to utilize this process to create recording arrays could not be completely tested because of the problems in our circuitry, it may still be possible to use the commercial process to our advantage and create electrode arrays and amplifier circuitry on the same chip.

4.6 Conclusions

In this research, we have implemented a neural recording system which incorporates the well-known chopper modulation technique to remove low-frequency noise added by the amplifier system. We manufactured a chip using the MOSIS AMI ABN 1.5um process. We worked on the manufacturing of neuron-transistors and on-chip recording electrodes. We also used commercial microelectrode arrays and incorporated them in a package with our amplifier. We have attempted experiments using crayfish and snail neurons and bovine chromaffin cells.

We showed that our chip works perfectly using synthetic signals created via signal generators. While we were unable to demonstrate the same level of performance in actual neural recording experiments, we have shown that this was due to a minor implementation issue and that the system is fundamentally sound.

It is our conclusion that with proper modification of the input stage of the amplifier, this system can be made to work as predicted in actual neural recording experiments.

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